Development of a Technique for Characterizing Bias Temperature Instability-Induced Device-to-Device Variation at SRAM-Relevant Conditions

Meng Duan, Jian Fu Zhang, Zhigang Ji, Wei Dong Zhang, Ben Kaczer, Tom Schram, Romain Ritzenthaler, Guido Groeseneken, and Asen Asenov

***Abstract*— SRAM is vulnerable to device-to-device variation (DDV), since it uses minimum-sized devices and requires device matching. In addition to the as-fabricated DDV at time-zero, aging induces a time-dependent DDV (TDDV). Bias temperature instability (BTI) is a dominant aging process. A number of techniques have been developed to characterize the BTI, including the conventional pulse-I–V, random telegraph noises, time-dependent defect spectroscopy, and TDDV accounting for the within-device fluctuation. These techniques, however, cannot be directly applied to SRAM, because their test conditions do not comply with typical SRAM operation. The central objective of this paper is to develop a technique suitable for characterizing both the negative BTI (NBTI) and positive BTI (PBTI) in SRAM. The key issues addressed include the SRAM relevant sensing Vg, measurement delay, capturing the upper envelope of degradation, sampling rate, and measurement time window. The differences between NBTI and PBTI are highlighted. The impact of NBTI and PBTI on the cell-level performance is assessed by simulation, based on experimental results obtained from individual devices. The simulation results show that, for a given static noise margin, test conditions have a significant effect on the minimum operation bias.**

***Index Terms*— Aging-induced variation, charge fluctuation, degradation, device variability, device-to-device variation, lifetime, negative bias temperature instabilities, statistical variation, time-dependent variation.**

I. Introduction

SRAM can occupy over 50% of the space for system-on-a-chip products, forcing it to use the minimum-sized devices. The device-to-device variability (DDV) increases as their size reduces [1]–[15]. The SRAM is especially vulnerable to DDV, since it has a high packing density and requires device match for its two cross-coupled inverters in Fig. 1. Apart from the as-fabricated DDV at time-zero [1]–[6], aging introduces a time-dependent DDV (TDDV) [7]–[15]. Aging originates from a number of sources: 1) negative bias temperature instability (NBTI) [16]–[19]; 2) hot carriers [20]; and 3) oxide breakdown [21]. For high-k/SiON gate dielectric stack, positive bias temperature instability (PBTI) can also be important [22]–[24]. Both NBTI for pMOSFETs and PBTI for nMOSFETs are investigated in this paper.

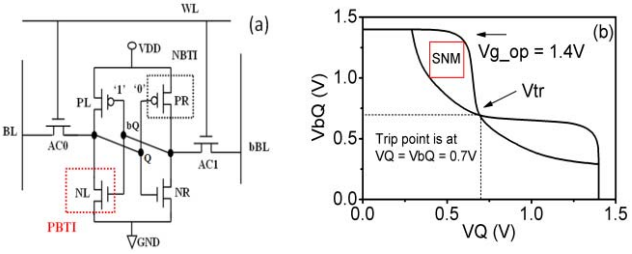

Fig. 1. (a) Standard symmetric six-transistor SRAM bitcell with PR, but not PL under NBTI stress. NL, but not NR, under PBTI stress when node Q is 0 and bQ is 1. If the bitcell does not flip, the stress is dc. (b) Butterfly characteristics during read. Vtr is the trip point.

The BTI can induce TDDV in two ways. On one hand, different devices in a circuit can suffer from different BTIs. For example, the pMOSFET PR in Fig. 1 suffers from NBTI stress, while PL does not, so that TDDV between PR and PL increases with time. On the other hand, even if two devices were stressed under the same conditions, the stochastic nature of charging-discharging the as-grown defects [8], [11] and generating new defects [14], [15] will result in TDDV.

A number of techniques have been developed to characterize the BTI and the TDDV, including the conventional pulse-I–V (PIV) [25], [26], random telegraph noises (RTN) [11]–[13], [27]–[29], time-dependent defect spectroscopy (TDDS) [8], and TDDV accounting for the within-a-device fluctuation (WDF) (TVF) [14], [15]. Although these techniques have provided valuable information on the defects, they cannot be directly applied to SRAM, because their test conditions do not comply with the SRAM operation, as analyzed in Section III.

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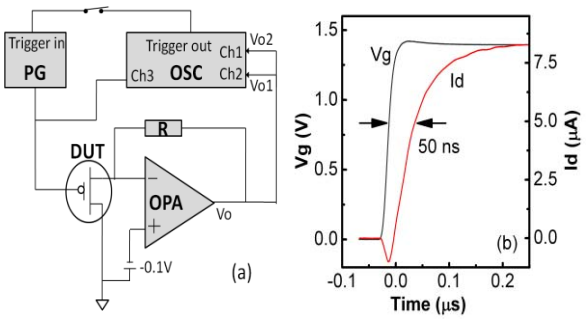

Fig. 2. (a) Test circuit. (b) Characteristic response time of the system. Vg was stepped with an edge time of 10 ns and Id = (Vo−Vd)/R rises to 63% of its peak in 50 ns.

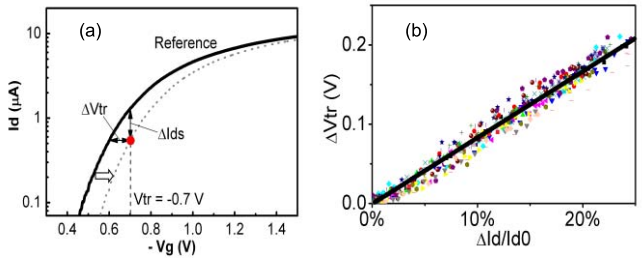

Fig. 3. (a) ΔVtr evaluation. The reference I–V was taken from a fresh device. After stress, Id at the trip point, Vg = Vtr, was measured and ΔVtr was taken from the Vg shift from the reference I–V at this Id. (b) Linear relation between ΔId/Id measured under Vg = −1.4 V and ΔVtr. The data were obtained from 21 devices.

The objective of this paper is to develop a technique suitable for characterizing both the NBTI and PBTI in SRAM. The key issues addressed include the sensing Vg, measurement delay, capturing the upper envelope (UE) of degradation, sampling rate, and measurement time window. The impact of BTI-induced TDDV on the static noise margin (SNM) and the minimum operation voltage of SRAM will be simulated and their sensitivity to test conditions will be highlighted.

II. Devices and Experiments

Both pMOSFETs and nMOSFETs have a channel length of 50 nm and a width of 90 nm. The gate dielectric stack is HfO_2 with an Al_2O_3 cap layer and the equivalent oxide thickness is 1.45 nm. The gate is TiN.

The experimental setup is given in Fig. 2(a) and Id was measured at |Vd| = 0.1 V through a fast operational amplifier [30]. To find the response time of the setup, a step Vg was applied to the input and Fig. 2(b) shows that the output Id can response in 50 ns. Before aging, a reference Id–Vg was taken in 3 μs and is shown in Fig. 3. The degradation during this short measurement time is negligible [14], [26].

The test follows a stress-then-sense procedure [25], [26] and the technique developed in this paper requires the device being stressed under use voltage. The stress was carried out at Vg = +1.4 V for PBTI of nMOSFETs and Vg = −1.4 V for NBTI of pMOSFETs. During stress, Id was continuously monitored on-the-fly against time. To assess the aging on the SRAM trip voltage, |Vg| was ramped down from 1.4 V to the trip point of the inverter, |Vtr| = 0.7 V, in 3 μs to minimize the recovery [26] and Id was measured. Fig. 3(a) shows that the stress lowered Id by ΔIds at |Vtr| = 0.7 V. The shift of trip voltage, ΔVtr, was taken against the reference IV. Fig. 3(b) plots the ΔVtr against the ΔId/Id measured at Vg = −1.4 V for 21 devices. They have a linear relation for all tested devices, which is used to convert ΔId/Id to ΔVtr.

All tests and measurements were carried out at 125 °C. Two channels of the oscilloscope were used for Id to obtain two different resolutions for the stress and measurement phases, respectively [15].

III. Shortcomings of Existing Techniques

The BTI tests were generally carried out on individual devices [7]–[16] and care must be excised when using these test data for assessing the impact on SRAM. In principle, the aging of a device in a circuit is the same as that for an individual device, provided the same voltage is applied during both stress and the measurement. To apply the test data obtained from individual devices to SRAM, it is crucial to align the measurement condition with the SRAM operation. In this section, the typical operation conditions of SRAM will be briefly reviewed first and the misalignment between the existing measurement techniques and SRAM operation will then be pointed out.

A. Typical Operation Conditions of SRAM

The SRAM has three basic operation modes: 1) read; 2) write; and 3) hold. The BTI mainly occurs in hold-mode and Fig. 1(a) shows that, when $Q = 0$ and bQ = 1, NL and PR suffers PBTI and NBTI, respectively, but NR and PL does not. This weakens NL and PR and maximizes the mismatch of the two inverters. In another word, the effects of PBTI and NBTI are adding, rather than canceling, for SRAM. If a bitcell's content does not change, NL and PR will be under the worst BTI stress: dc stress without recovery.

The SNM for a standard six-transistor SRAM is smaller during read than hold, because the precharged BL in Fig. 1(a) will partially pull-up Q through voltage dividing between AC0 and NL. The BTI weakens NL and PR by reducing their overdrive voltage |Vg − Vth| and in turn, the SNM. In contrast, this reduction of |Vg − Vth| does not reduce the write noise margin, since a weakened NL and PR will make the bitcell easier to flip. As a result, SRAM is most vulnerable to BTI during read. The typical read time is in the order of tens of nanoseconds, during which Q and bQ can approach Vtr in Fig. 1(b) and flip the bitcell erroneously. The SRAM-relevant BTI should use the operation bias for hold, Vg_op, as the stress voltage and the degradation should be sensed at Vg = Vtr.

B. Shortcomings of Existing Techniques

1) Conventional p-I–V: The p-I–V allows measuring threshold voltage shift at a preset stress time in ∼μs that minimizes recovery during measurement [25], [26]. It worked well for large devices where Id has little fluctuation, as

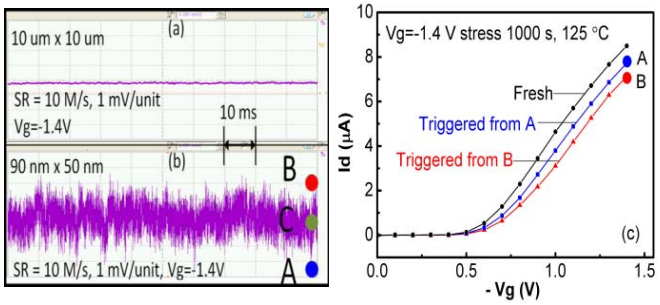

Fig. 4. (a) and (b) After a 1000-s stress, Id under Vg $= -1.4$ V fluctuates little for a 10-μm $\times$ 10-μm device, but substantially for a 90-nm $\times$ 50-nm device. Time window in (a) and (b) is 0.1 s. Note the output signal Vo in Fig. 2(a) is negative, so that Id at B is smaller than Id at A. The point C represents a typical dc measurement at a speed of 10 ms per point. When triggering Vg-switch from the point A and B, the recorded degradation is significantly different (c).

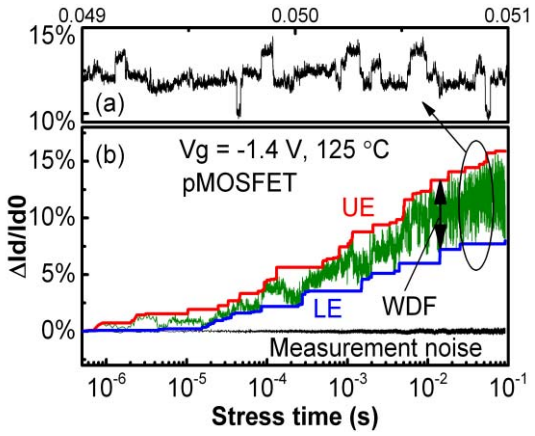

Fig. 5. (a) For a given defect number, the RTN signal by enlarging the circled region of (b) Defects, however, increase with time. The UE and LE represent the UE and LE of raw data and their difference is caused by the WDF under a given Vg. The system measurement noise is negligible.

shown in Fig. 4(a). For nm-size devices, however, Id fluctuates substantially [Fig. 4(b)] due to the discrete nature of charging-discharging. Fig. 4(c) shows that for the same stress, the degradation varies substantially, depending on the charging level immediately before triggering the measurement. The conventional p-I–V makes one measurement and gives only one ΔVth at a preset time [25], [26]. It does not take this within-a-device-fluctuation (WDF) into account and does not give the range of threshold voltage shift for a given stress time. The dc measurement of conventional parameter analyzer typically uses the average value within a measurement time window of, say 10 ms, as represented by the point C in Fig. 4(b). It does not capture the fluctuation well.

2) Random Telegraph Noises: Unlike the conventional p-I–V, the RTN captures the WDF by monitoring Id against time [11]–[13], [27]–[29]. The problem with the standard RTN technique is that it requires both charging and discharging a defect to produce a telegraph-noise, as shown in Fig. 5(a). However, there are substantial amount of defects that do not discharge under Vg_op $= -1.4$ V, as marked by the LE for the lower envelope (LE) of ΔId/Id in Fig. 5(b) and they are not probed by RTN.

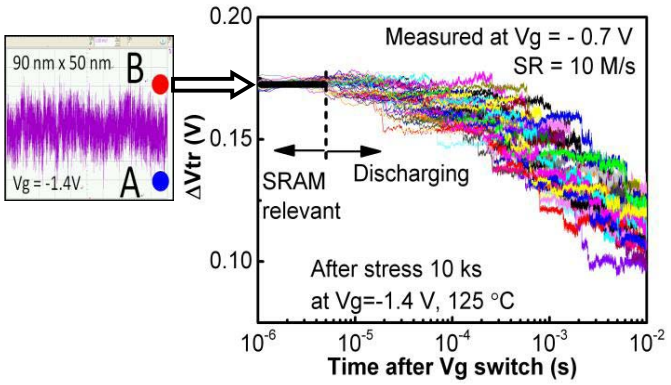

Fig. 6. Vg-switch from -1.4 to -0.7 V was triggered from the point B and ΔVtr is monitored for 10^{-2} s under Vtr $= -0.7$ V. Vg $= -1.4$ V was then reapplied until the Id reached the point B and the Vg-switch triggered again. This sequence was repeated 50 times. The discharge is absent for < 5 μs. The stochastic discharge at longer time induces considerable variation, which is irrelevant to SRAM during read operation.

To reduce the discharge time and observe it within the measurement time window, tw, the RTN is typically monitored at a |Vg| lower than the operation |Vg_op| [27], [28]. As analyzed in the Section III-A, for SRAM, Vg_op can be applied indefinitely during the hold of a bitcell, but Vg may approach Vtr during read for a typical time of only $\sim$10 ns. As a result, for SRAM, the charge fluctuation should be monitored at Vg_op, rather than at |Vg| $<$ |Vg_op| [27], [28]. Fig. 6 presents the transient ΔVtr when |Vg| was stepped down from |Vg_op| to |Vtr|. The ΔVtr is flat in $\sim\mu$s range [11], [26], although discharge happened at longer time. It should be pointed out that the flat $\sim\mu$s region in Fig. 6 is not caused by system limitation, since its response time is 50 ns [Fig. 2(b)]. As a result, there is no RTN signal in the time domain relevant to SRAM operation at Vtr, so that RTN cannot be used to measure ΔVtr in a time-domain relevant to reading an SRAM cell. In addition, RTN is difficult to analyze when there are more than four traps [29].

3) Time-Dependent Defect Spectroscopy: The TDDS [8] probes individual defects by monitoring their discharge after Vg switching from Vg_op to a low level close to Vth, as illustrated in Fig. 6. When triggered from the same point B repeatedly, the same SRAM-relevant charge level in $\sim\mu$s was observed. The subsequent discharge, however, introduces a considerable variation due to the stochastic nature of discharge. As a result, there is no TDDS signal at Vtr for SRAM operation condition and there is no unique relation between the ΔVtr at $\sim\mu$s and the amount of discharge measured within a limited time window. To further explore this point, Fig. 7 compares two cases triggered from A and B. As expected, ΔVtr(B) $>$ ΔVtr(A) in $\sim\mu$s, but the two curves actually cross over later, confirming that there is no unique relation between ΔVtr at $\sim\mu$s and ΔVtr at longer time.

Another difficulty with the TDDS is that discharge does not always complete within a practical time window, especially after a relatively long stress (e.g., $>$1000 s), because of the permanent component [16], [18] originating from the generated anti-neutralization positive charges [31]–[33]. In addition,

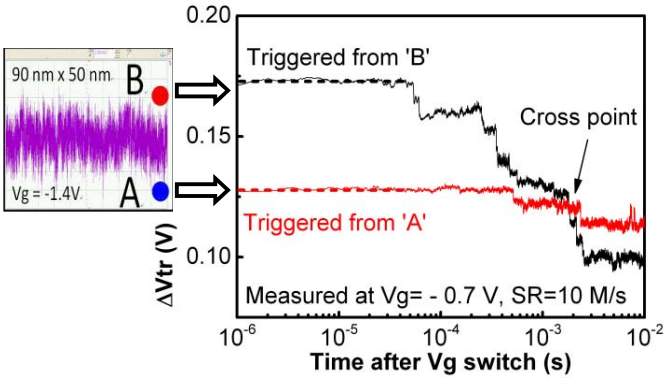

Fig. 7. After triggering from the points A and B in Fig. 4(b), respectively, ΔVtr('A')< ΔVtr('B') in ∼μs, but ΔVtr('A')> ΔVtr('B') at 10 ms, indicating the ΔVtr measured at typical dc speed is not a reliable representation of the SRAM-relevant ΔVtr in ∼μs.

TDDS does not directly give the WDF at Vg_op, which plays an important role in the BTI-induced TDDV, as to be shown in the Sections IV-B and IV-D.

4) TDDV Accounting for the WDF: The TVF [14], [15] is based on the measurement in Fig. 5(b), where the UE was divided into two components: a WDF and the defect that does not discharge under Vg_op, i.e., the LE. To capture the UE and LE, ΔId/Id was monitored continuously under Vg_ op $= -1.4$ V. By comparing the WDF, LE, and UE of different devices, TVF allows separating DDV from WDF.

The TVF proposed in our early work [14] monitors the degradation by ΔId/Id under Vg_op, but SRAM is most vulnerable to BTI during read when Vg approaching Vtr. The SRAM-aging should be characterized by ΔVtr, therefore. In addition the sampling rate (SR) used in [14] was only 100 point per second, which substantially underestimated the WDF, as to be shown in the Section IV-A. The applicability of TVF to PBTI of nMOSFETs is not tested, either.

IV. Characterize BTIs-Induced TDDV for SRAM

The TVF technique [14], [15] will be revised and extended to nMOSFETs to probe the BTIs-induced TDDV for SRAM by addressing a number of key issues, including the sensing Vg, measurement delay, capturing the UE of degradation, SR, and measurement time window. We will first study how to measure the SRAM-relevant BTI for one device reliably and then investigate the DDV.

A. Measuring a Single Device

1) AC or DC Stress: Digital circuits are typically under ac stress with a reduced degradation when compared with dc stress. An SRAM bitcell, however, can hold its content indefinitely and the dc stress is used here, therefore.

2) Sensing Vg and Measurement Delay: As analyzed in the Section III-A, the SRAM is most vulnerable to BTI during read, when Vg can approach Vtr in ∼ns. A degradation of Vtr can cause a flip, so that BTI should be assessed by measuring ΔVtr at a sensing Vg∼Vtr [26], as shown in Fig. 3. Ideally, the measurement delay should be only ∼ns, but this cannot be achieved for wafer level measurements. Fig. 7 shows that a measurement delay of ∼μs is adequate to minimize the recovery during measurement.

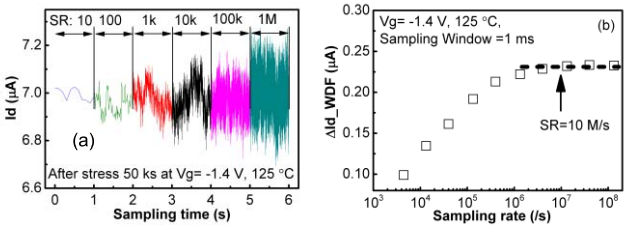

Fig. 8. Dependence of WDF on the SR for pMOSFETs. Id fluctuation increases with SR when (a) SR < 1 M/s , but saturates after (b) SR > 1 M/s. The device was stressed for 50 ks to ensure that further degradation during the measurement itself is negligible.

3) Capturing the UE of ΔVtr: When a bitcell's content does not change, WDF occurs under Vg_op. A bitcell can be read many times and there can be millions of bitcells in an SRAM. It is inevitable that some bitcells will be read when the charging reaches its UE, i.e., the point B in Fig.4(b) and (c). It is important to capture the UE of ΔVtr during test, therefore. This requires monitoring Id under Vg_op, rather than under a |Vg|< |Vg_op|.

It has been reported that defects can have a wide range of charging and discharging time [8], [11]–[13]. To capture the fast trap, the SR, must be sufficiently high. To capture the slow trap, the measurement time window must be sufficiently wide.

4) Sampling Rate: To investigate the dependence of WDF on SR, it is desirable to fix the number of defects during the measurement. This can be achieved by first stressing a device heavily, so that further defect generation is negligible during the subsequent measurement. After a stress time of 1000 s or longer, tests show that further increase in defect number in the subsequent 40 s is <0.27 mV, which is within the test resolution. Fig. 8(a) gives the WDF measured within a time window of tw $= 1$ s at different SR after 50-ks stress. The WDF increased substantially with SR, but Fig. 8(b) shows that a saturation is reached around SR $= 1$ M/s. This indicates that the defects responsible for WDF have a charging/discharging time larger than ∼μs, in agreement with the lack of fluctuation in the ∼μs region in Fig. 7. We will use SR $= 10$ M/s for the on-the-fly measurement of ΔId/Id hereafter and emphasize that it is enough to capture the fast traps for NBTI.

5) Measurement Window: Fig. 9(a) indicates that the WDF is approximately constant as the measurement time window, tw, increases. This is, however, an artifact. Once the tw is plotted in logarithmic scale, Fig. 9(b) shows that WDF increases with tw. As a result, tw should be made as long as possible. Since Id is monitored on-the-fly, the longest possible tw is tw $=$ stress time and this is achieved by recording Id continuously during test. The time window here is for measuring ΔId/Id under Vg_op $= -1.4$ V and it increases with stress time.

After examining the WDF caused by the NBTI of pMOSFETs, we turn our attention to the PBTI of nMOSFETs. As illustrated in Fig. 1, when the pMOSFET (PR) is suffering

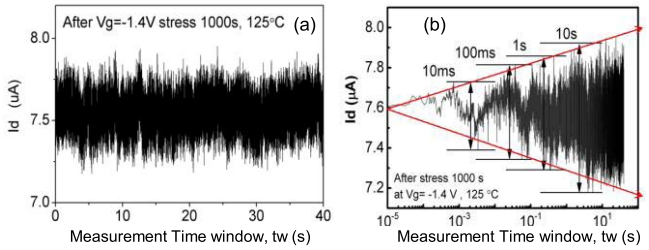

Fig. 9. Dependence of WDF on the measurement time window for pMOSFETs. Although the Id fluctuation appears insensitive to time in a linear scale in (a), it clearly increases with time when plotted in a logarithmic scale in (b) for a pMOSFET.

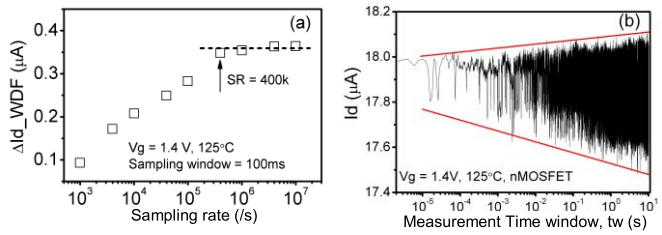

Fig. 10. WDF of PBTI in an nMOSFET. The nMOSFET was prestressed for 1 ks under Vg $= +1.4$ V to ensure negligible new defect creation during the measurement itself. (a) Dependence on SR. Id fluctuation increase with SR, but saturates after SR $>$ 400 k/s. (b) Dependence on the measurement time window.

NBTI, the nMOSFET (NL) is suffering PBTI at the same time. Fig. 10(a) shows that the PBTI-induced WDF increases by a factor over 3 with SR, and then saturates for SR $\geq$ 400 k/s. Similar to the NBTI-induced WDF, the PBTI-induced WDF also increases with measurement time window in Fig. 10(b). The revised TVF proposed for NBTI can be used to probe the PBTI of nMOSFETs.

In short, the TVF monitors ΔId/Id on-the-fly and then convert it to ΔVtr at the trip point based on the p-I–V. It is different from the conventional on-the-fly method that measures ΔVth at the stress Vg, rather than at the trip point. It is also different from the conventional p-I–V that did not monitor the ΔId/Id on-the-fly and did not capture the UE of ΔId/Id.

B. NBTI-Induced TDDV

After studying how to characterize the SRAM-relevant BTI for a single device by the improved TVF, the same test like Fig. 5 was repeated for 56 different pMOSFETs to study the NBTI-induced TDDV. The ΔId/Id0_UE measured in Fig. 5 is converted to ΔVtr_UE by using Fig. 3(b) for each device and the DDVs are given in Fig. 11. It increases in steps and the gap between two steps varies due to the discreteness and stochastics of charges. The thick line represents the devices of the largest UE at a stress time of 1000 s. Their positions relative to other devices change with time. For example, the device of largest UE at 1000 s had one of the lowest UE at short time. As a result, it is essential to measure the NBTI in all devices at all time.

The distributions of UE are given in Fig. 12 and they can be fitted reasonably with the Gaussian distribution. The

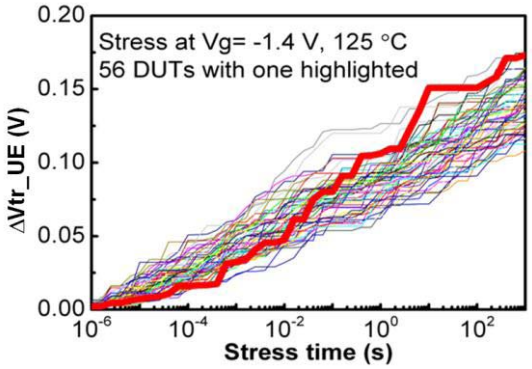

Fig. 11. ΔVtr_UE against stress time, recorded for 56 90-nm $\times$ 50-nm pMOSFETs. For each device, ΔId/Id0 was continuously monitored under Vg $= -1.4$ V and its UE was extracted, as shown in Fig. 5(b). This ΔId/Id0_UE was then converted to ΔVtr_UE by using their relation in Fig. 3(b). The thick line highlights the device with the highest degradation at 1000 s, although it is close to the bottom at short time. The step-like change is caused by the discreteness of charges.

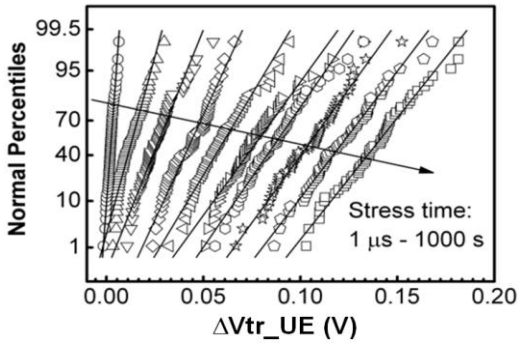

Fig. 12. Statistical distribution of ΔVtr_UE for NBTI of pMOSFETs. An increase of stress time raised not only the average, but also the variation. The solid lines were fitted with the Gaussian distribution.

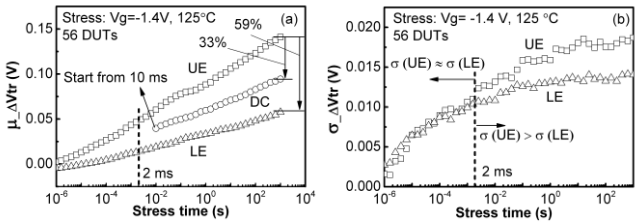

Fig. 13. NBTI of pMOSFETs. (a) Kinetics of the average, μ. (b) Standard deviation, σ. μ_UE$>$ 2 $\times$ μ_LE, due to the contribution of WDF under a given Vg. The dc represents the typical results measured by a quasi-dc parameter analyzer. σ_UE $\approx$ σ_LE within 2 ms, but σ_UE $>$ σ_LE afterward.

kinetics of the average (μ) and standard deviation (σ) is given in Fig. 13(a) and (b), respectively. As time increases, both μ and σ increase. μ_UE more than doubles μ_LE and the typical dc measurement also substantially underestimates μ_UE. Although μ_LE $<$ μ_UE/2 in Fig. 13(a), σ_LE $\approx$ σ_UE initially (i.e., $<$ 2 ms) in Fig. 13(b), indicating the WDF contributes little to DDV initially. For longer stress, however, σ_UE is clearly above σ_LE and the WDF does vary for different devices.

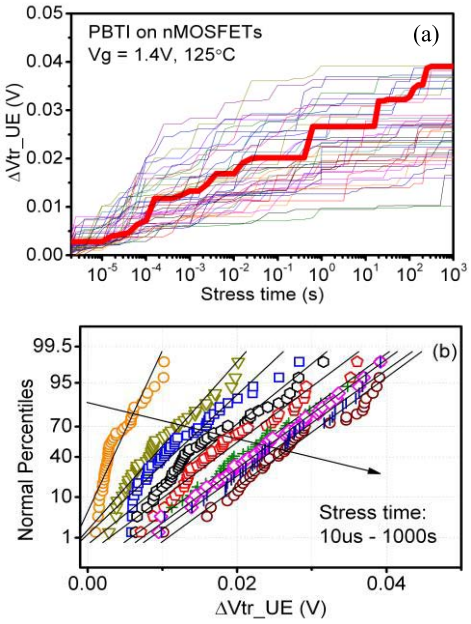

Fig. 14. PBTI of 45 nMOSFETs. Stress conditions were Vg = +1.4 V under 125 °C. The thick line in (a) highlights the device with the highest degradation at 1000 s, although it was close to the bottom at short stress time. (b) Statistical distribution of ΔVth_UE, solid lines were fitted with the Gaussian distribution.

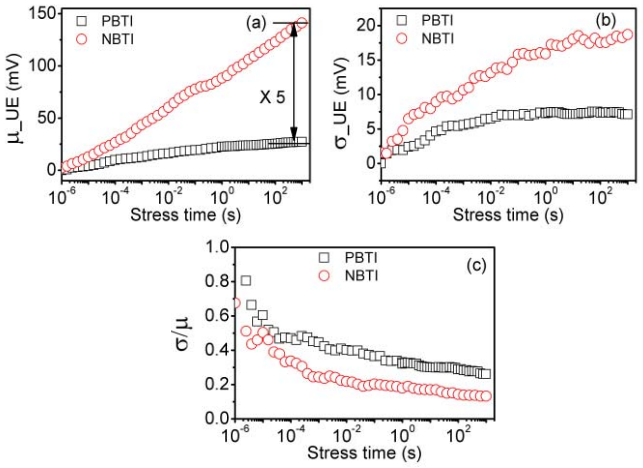

Fig. 15. Comparison of the kinetics: PBTI versus NBTI under |Vg| = 1.4 V at 125 °C. (a) Average, μ. (b) Standard deviation, σ. (c) σ/μ. NBTI is substantially higher than PBTI, but PBTI has higher σ/μ, indicating a higher relative variation.

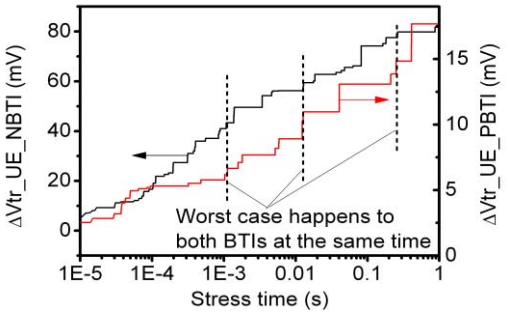

Fig. 16. UE of NBTI and PBTI. The worst TDDV occurs when NBTI and PBTI reach their UE simultaneously, as marked by the vertical dotted lines.

C. PBTI-Induced TDDV

Similar results were obtained for PBTI in nMOSFETs, as shown in Fig. 14(a) and (b). Fig. 15(a)–(c) compares the UE of NBTI and PBTI when stressed under |Vg| = 1.4 V. After 1000-s stress, the average of NBTI is five times of that of PBTI. The difference in their standard deviation, however, is smaller. This leads to a higher σ/μ for PBTI [Fig. 15(c)], indicating the DDV is relatively larger for PBTI of nMOSFETs.

D. Impact on SRAM

Ideally, to assess the impact of BTI on SRAM performance, one would like to insert the aged devices into an SRAM cell and measure it directly [34]. Such test structure, however, is not available to this paper, so that we simulate the impact. The design and optimization of SRAM must meet multiple constraints, such as static and dynamic margins and power consumptions. In this paper, we focus only on one key parameter, the static read noise margin (SNM).

1) Worst Case BTIs for SRAM: To illustrate the potential impact of BTI on SRAM, we use simulation based on a 45-nm technology. The SNM was simulated with both access transistors, AC0 and AC1 in Fig. 1(a) switched ON. The bias at Q, VQ, is swept from zero to 1.4 V and the VbQ is recorded to obtain the voltage transfer characteristics (VTC) for the inverter on the right-hand side (PR-NR). We then sweep VbQ and record VQ to obtain the VTC for the inverter on the left-hand side (PL-NL). These two VTCs form the butterfly in Fig. 1(b).

We will first consider the NBTI and PBTI separately and then combine them. When reading a bitcell, the worst case is that both NBTI and PBTI reach their UE, which maximizes the mismatch between the two inverters. As an example, Fig. 16 shows that this occurred three times for two devices. Given that there are often multimillion bitcells in an SRAM, one should consider the combined impact of UE_NBTI and UE_PBTI.

2) BTIs Impact on SNM: One of the most important parameters for SRAM read stability is the SNM [35]. The SNM is typically measured from the size of the square that can be fitted into the two VTCs for the butterfly [Fig. 1(b)]. To simulate the impact of NBTI, we assume that PR is aged by ΔVtr(NBTI) and simulate the VTC for the PR-NR inverter. Fig. 17(a) shows the VTC(PR-NR) is shifted toward left, reducing SNM. The impact of UE_NBTI is significantly higher than that of LE_NBTI, so that it is important to capture the UE.

Similarly, to simulate the impact of PBTI, we assume that NL is aged by ΔVtr(PBTI) and simulate the VTC for the PL-NL inverter and Fig. 17(b) shows the VTC(PL-NL) is shifted toward right. Since the two VTCs were shifted in the opposite direction by NBTI and PBTI, respectively, their effect on the SNM reduction is adding.

Fig. 17(c) shows that reduction of SNM caused by UE_NBTI and UE_PBTI separately and by combining them. Although NBTI has a larger impact, the contribution of PBTI is around one-fourth of the combined and must be taken into

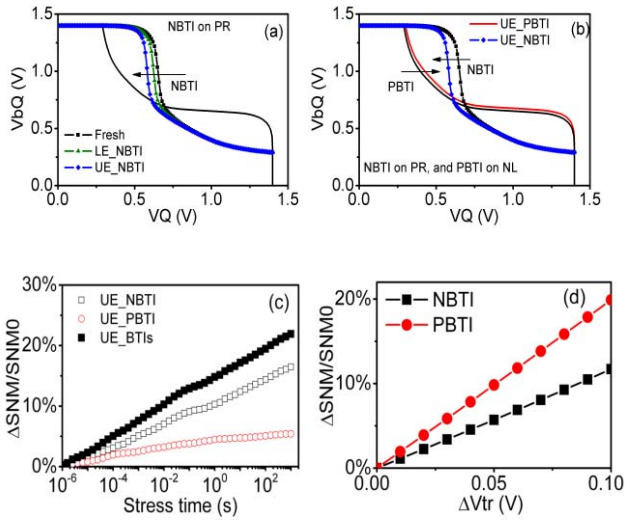

Fig. 17. Simulation of the BTI impact on SRAM for a 45-nm technology. (a) NBTI impact on SRAM. The degradation is much larger for the UE_NBTI than the LE_NBTI. (b) Degradation by both NBTI and PBTI. (c) SNM degradation caused by UE_NBTI, UE_PBTI, and their combination. (d) For the same $|\Delta \text{Vtr}|$, PBTI results in a larger ΔSNM/SNM.

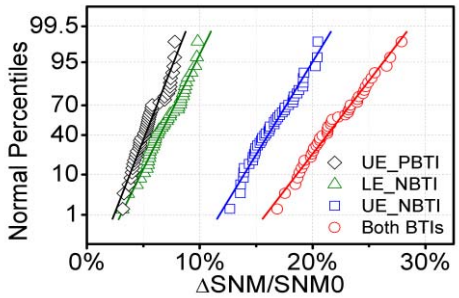

Fig. 18. Statistical distributions of ΔSNM/SNM caused by NBTI, PBTI, and NBTI+PBTI. The devices were stressed under $|\text{Vg}| = 1.4$ V for 1000 s at 125 °C. The SNM was simulated based on the experimental UE_NBTI and UE_PBTI.

account. Early works [23] and [36] show that PBTI of high-k/SiON stack is sensitive to processing conditions and the smaller PBTI in Fig. 17(c) could be achieved through process optimization. For the same $|\Delta \text{Vtr}|$, however, Fig. 17(d) shows that PBTI has a larger effect on SNM degradation. This is because during read, VQ in Fig. 1(a) and (b) is not at zero, due to the voltage dividing between AC0 and NL [37].

Fig. 18 gives the distribution of by ΔSNM/SNM. A combination of NBTI and PBTI increases not only its average, but also its variation.

3) BTIs Impact on the Minimum V_{DD}: To reduce power consumption, lowering V_{DD} is desirable. A lower V_{DD}, however, reduces SNM, as shown in Fig. 19. For a given SNM, the required V_{DD} can be substantially increased by the BTI-induced TDDVs. For example, for a 45-nm CMOS technology, to keep an SNM = 180 mV, V_{DD} is about 0.9 V before BTI. It increases to 1.2 V when considering the UE_NBTI and rises further to 1.38 V after combining UE_NBTI and UE_PBTI.

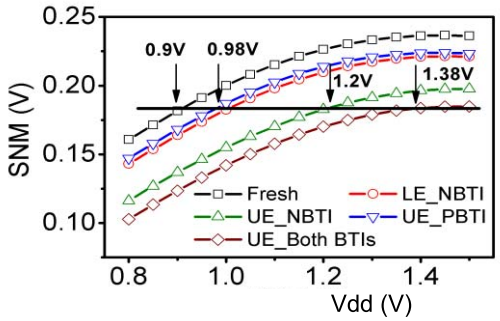

Fig. 19. SNM versus V_{DD} with NBTI, PBTI, and NBTI+PBTI. For a required SNM, BTIs increase the minimum V_{DD} substantially. The SNM was simulated based on the experimental UE_NBTI and UE_PBTI.

V. Conclusion

The existing techniques are not suitable for probing the BTI-induced TDDV for SRAM and a technique suitable for this task has been developed by improving the TVF. The key issues addressed include the sensing Vg, measurement delay, capturing the UE of degradation, SR, and measurement time window. The TVF allows capturing both the fast and slow traps, minimizing the missing of a defect during measurement. The results show that the WDF is significant and it should be captured at the operation bias, rather than at a Vg close to threshold level. Both NBTI for pMOSFETs and PBTI for nMOSFETs were investigated and compared. The NBTI is substantially higher than the PBTI, but PBTI also makes considerable contribution to TDDV for the high-k/SiON stack. For the same average ΔVtr, PBTI has a large variation and also a large effect on the SNM.

References

[1] A. Asenov *et al.*, "Modeling and simulation of transistor and circuit variability and reliability," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2010, pp. 1–8.

[2] K. J. Kuhn, "Reducing variation in advanced logic technologies: Approaches to process and design for manufacturability of nanoscale CMOS," in *Proc. IEEE IEDM*, Dec. 2007, pp. 471–474.

[3] P. A. Stolk and D. B. M. Klaassen, "The effect of statistical dopant fluctuations on MOS device performance," in *Proc. IEDM*, Dec. 1996, pp. 627–630.

[4] T. Mizuno, J. Okamura, and A. Toriumi, "Experimental study of threshold voltage fluctuation due to statistical variation of channel dopant number in MOSFET's," *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 2216–2221, Nov. 1994.

[5] J. T. Horstmann, U. Hilleringmann, and K. F. Goser, "Matching analysis of deposition defined 50-nm MOSFET's," *IEEE Trans. Electron Devices*, vol. 45, no. 1, pp. 299–306, Jan. 1997.

[6] K. R. Lakshmikumar, R. A. Hadaway, and M. A. Copeland, "Characterisation and modeling of mismatch in MOS transistors for precision analog design," *IEEE J. Solid-State Circuits*, vol. 21, no. 6, pp. 1057–1066, Dec. 1986.

[7] Y. Mitani, "Experimental study on origin of VTH variability under NBT stress," in *Proc. IEEE Int. Rel. Phys. Symp.*, Apr. 2011, pp. 857–862.

[8] T. Grasser, H. Reisinger, P.-J. Wagner, and B. Kaczer, "Time-dependent defect spectroscopy for characterization of border traps in metal–oxide–semiconductor transistors," *Phys. Rev. B*, vol. 82, p. 245318, Dec. 2010.

[9] S. Pae, J. Maiz, C. Prasad, and B. Woolery, "Effect of BTI degradation on transistor variability in advanced semiconductor technologies," *IEEE Trans. Device Mater. Rel.*, vol. 8, no. 3, pp. 519–525, Sep. 2008.

[10] S. E. Rauch, "Review and reexamination of reliability effects related to NBTI-induced statistical variations," *IEEE Trans. Device Mater. Rel.*, vol. 7, no. 4, pp. 524–530, Dec. 2007.

[11] C. Liu *et al.*, "Towards the systematic study of aging induced dynamic variability in nano-MOSFETs: Adding the missing cycle-to-cycle variation effects into device-to-device variation," in *IEDM Tech. Dig.*, Dec. 2011, pp. 571–574.
[12] J. Zou *et al.*, "New insights into AC RTN in scaled high-κ/metal-gate MOSFETs under digital circuit operations," in *Proc. Symp. Very Large Scale Integr. (VLSI) Technol.*, Jun. 2012, pp. 139–140.
[13] P. Ren *et al.*, "New observations on complex RTN in scaled high-κ/metal-gate MOSFETs—The role of defect coupling under DC/AC condition," in *IEDM Tech. Dig.*, Dec. 2013, pp. 778–781.
[14] M. Duan *et al.*, "New analysis method for time-dependent device-to-device variation accounting for within-device fluctuation," *IEEE Trans. Electron Devices*, vol. 60, no. 8, pp. 2505–2511, Aug. 2013.
[15] M. Duan *et al.*, "Key issues and techniques for characterizing time-dependent device-to-device variation of SRAM," in *IEDM Tech. Dig.*, Dec. 2013, pp. 774–777.
[16] T. Grasser *et al.*, "The 'permanent' component of NBTI: Composition and annealing," in *Proc. Int. Rel. Phys. Symp.*, Apr. 2011, pp. 605-613.
[17] M. H. Chang and J. F. Zhang, "On positive charge formed under negative bias temperature stress," *J. Appl. Phys.*, vol. 101, no. 2, p. 024516, 2007.
[18] M. Duan *et al.*, "New insights into defect loss, slowdown, and device lifetime enhancement," *IEEE Trans. Electron Devices*, vol. 60, no. 1, pp. 413–419, Jan. 2013.
[19] J. F. Zhang *et al.*, "Dominant layer for stress-induced positive charges in Hf-based gate stacks," *IEEE Electron Device Lett.*, vol. 29, no. 12, pp. 1360–1363, Dec. 2008.
[20] J. F. Zhang and W. Eccleston, "Effects of high field injection on the hot carrier induced degradation of submicrometer pMOSFET's," *IEEE Trans. Electron Devices*, vol. 42, no. 7, pp. 1269–1276, Jul. 1995.
[21] W. D. Zhang, J. F. Zhang, C. Z. Zhao, M. H. Chang, G. Groeseneken, and R. Degraeve, "Electrical signature of the defect associated with gate oxide breakdown," *IEEE Electron Device Lett.*, vol. 27, no. 5, pp. 393–395, May 2006.
[22] J. F. Zhang, "Defects and instabilities in Hf-dielectric/SiON stacks (invited paper)," *Microelectron. Eng.*, vol. 86, nos. 7–9, pp. 1883–1887, Jul./Sep. 2009.
[23] C. Z. Zhao, J. F. Zhang, M. B. Zahid, B. Govoreanu, G. Groeseneken, and S. D. Gendt, "Determination of capture cross sections for as-grown electron traps in HfO_2/HfSiO stacks," *J. Appl. Phys.*, vol. 100, no. 9, pp. 093716-1–093716-10, Nov. 2006.
[24] C. Z. Zhao, M. B. Zahid, J. F. Zhang, G. Groeseneken, R. Degraeve, and S. D. Gendt, "Properties and dynamic behavior of electron traps in HfO_2/SiO_2 stacks," *Microelectron. Eng.*, vol. 80, pp. 366–369, Jun. 2005.
[25] T. Yang *et al.*, "Fast and slow dynamic NBTI components in p-MOSFET with SiON dielectric and their impact on device life-time and circuit application," in *Symp. Very Large Scale Integr. (VLSI) Technol. Dig. Tech. Papers*, Jun. 2005, pp. 92–93.
[26] Z. Ji, J. F. Zhang, M. H. Chang, B. Kaczer, and G. Groeseneken, "An analysis of the NBTI-induced threshold voltage shift evaluated by different techniques," *IEEE Trans. Electron Devices*, vol. 56, no. 5, pp. 1086–1093, May 2009.
[27] T. Nagumo, K. Takeuchi, T. Hase, and Y. Hayashi, "Statistical characterization of trap position, energy, amplitude and time constants by RTN measurement of multiple individual traps," in *IEDM Tech. Dig.*, Dec. 2010, pp. 628–631.
[28] N. Tega *et al.*, "Increasing threshold voltage variation due to random telegraph noise in FETs as gate lengths scale to 20 nm," in *Proc. Symp. Very Large Scale Integr. (VLSI) Technol.*, Jun. 2009, pp. 50–51.
[29] H. Kurata *et al.*, "Anomalously large threshold voltage fluctuation by complex random telegraph signal in floating gate flash memory," in *IEDM Tech. Dig.*, Dec. 2006, pp. 218-221.
[30] Z. Ji, J. F. Zhang, and W. Zhang, "A new mobility extraction technique based on simultaneous ultrafast I_d–V_g and C_{cg}–V_g measurements in MOSFETs," *IEEE Trans. Electron Devices*, vol. 59, no. 7, pp. 1906–1914, Jul. 2012.
[31] C. Z. Zhao and J. F. Zhang, "Effects of hydrogen on positive charges in gate oxides," *J. Appl. Phys.*, vol. 97, no. 7, pp. 073703-1–073703-8, Apr. 2005.
[32] C. Z. Zhao *et al.*, "Stress-induced positive charge in Hf-based gate dielectrics: Impact on device performance and a framework for the defect," *IEEE Trans. Electron Devices*, vol. 55, no. 7, pp. 1647–1656, Jul. 2008.
[33] J. F. Zhang, M. H. Chang, and G. Groeseneken, "Effects of measurement temperature on NBTI," *IEEE Electron Device Lett.*, vol. 28, no. 4, pp. 298–300, Apr. 2007.
[34] A. T. Krishnan *et al.*, "SRAM cell static noise margin and VMIN sensitivity to transistor degradation," in *IEDM Tech. Dig.*, Dec. 2006, pp. 77–80.
[35] E. Seevinck, F. J. List, and J. Lohstroh, "Static-noise margin analysis of MOS SRAM cells," *IEEE J. Solid-State Circuits*, vol. 22, no. 5, pp. 748–754, Oct. 1987.
[36] M. B. Zahid, R. Degraeve, J. F. Zhang, and G. Groeseneken, "Impact of process conditions on interface and high-κ trap density studied by variable T_{charge}–$T_{discharge}$ charge pumping (VT^2CP)," *Microelectron. Eng.*, vol. 84, nos. 9–10, pp. 1951–1955, 2007.
[37] A. Bansal, R. Rao, J.-J. Kim, S. Zafar, J. H. Stathis, and C.-T. Chuang, "Impact of NBTI and PBTI in SRAM bit-cells: Relative sensitivities and guidelines for application-specific target stability/performance," in *Proc. IEEE Int. Rel. Phys. Symp.*, Apr. 2009, pp. 745–749.

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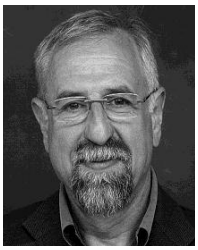

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