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# Statistical Variability in Implant-Free Quantum-Well MOSFETs with InGaAs and Ge: A comparative 3D simulation study

Ewan Towie<sup>1</sup>, Kah Hou Chan<sup>1</sup>, Brahim Benbakhti<sup>3</sup>, Craig Riddet<sup>1</sup>, Asen Asenov<sup>1,2</sup>

<sup>1</sup> Device Modelling Group, School of Engineering, University of Glasgow, G12 8LT Glasgow, U.K

<sup>2</sup> Gold Standard Simulations Ltd., G12 8LT Glasgow, U.K

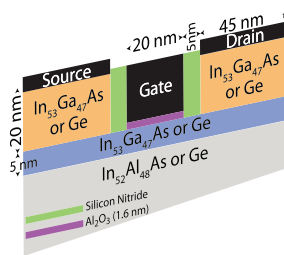
<sup>3</sup> School of Engineering, Liverpool John Moores University, L3 3AF Liverpool, U.K.

Ewan.Towie@glasgow.ac.uk

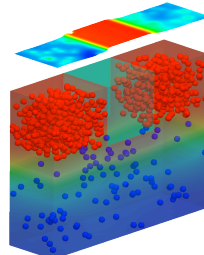
## Summary

Introduction of high mobility channel materials including III-Vs and Ge into future CMOS generations offer the potential for enhanced transport properties compared to Si. The Implant Free Quantum Well (IFQW) architecture offers an attractive design to introduce these materials, providing excellent electrostatic integrity. Statistical variability introduced by the discreteness of charge and granularity of matter has become a key factor for current and future generations of MOSFETs and in this work numerical simulations are used to critically assess the statistical variability in IFQW transistors and compare results with equivalent conventional Si ‘bulk’ MOSFETs.

The 20nm gate length IFQW device architecture considered in this paper is depicted in Fig. 1 [1-4], with the n-type device (nIFQW) using InGaAs/InAlAs III-V materials and the p-type device utilising Ge. Both devices have a relatively lowly doped channel ( $1 \times 10^{17} \text{cm}^{-3}$ ). The 3D Glasgow atomistic drift-diffusion simulator GARAND [5] has been calibrated to Monte Carlo (MC) simulations of the IFQW devices (Fig. 2) and then used to simulate the impact of Random Discrete Dopants (RDD), Line Edge Roughness (LER) and Metal Gate Granularity (MGG) on threshold voltage ( $V_T$ ) variability in ensembles of 1000 devices and compared to an equivalent Si device.



**Fig 1. Cross section of the IFQW device.**



**Fig 2. Example layout of dopants.**

Here, RDD variability simulations account for the random dopants in the source/drain, channel and substrate (see Fig. 2). LER induced modulation of the gate length has also been simulated with a reduction in gate length leading to a decrease in  $V_T$ . The effect of LER is significantly smaller than the RDD induced variability due to the excellent electrostatic integrity of the IFQW transistors. The final source of variability studied in respect of these devices is MGG where a TiN metal gate is considered. A range of grain sizes

from 5nm to 30nm has been simulated and the spread in  $V_T$  distribution increases with the grain size.

Combined variability simulations have been completed for both the IFQW and bulk Si devices and include a combination of LER and MGG grain sizes of 5nm and 20nm (always in conjunction with RDD). The Si MOSFETs have a metal gate of 20nm length and a typical halo doping profile. Table 1 compares the  $\Delta V_T$  for both architectures and highlights that the IFQW devices have better immunity to  $V_T$  variability. This illustrates the benefit of the low doped channel, reducing the RDD induced variability.

	nIFQW	pIFQW	nSi	pSi
$\sigma V_T$ [mV] (RDD + LER + MGG)				
<b>MGG 5nm</b>				
LER 2nm	44	42	94	79
LER 4nm	44	44	94	91
<b>MGG 10nm</b>				
LER 2nm	74	76	110	96
LER 4nm	77	75	110	10

**Table 1. Comparison of the IFQW device combined  $V_T$  variability with a bulk Si MOSFET.**

In conclusion, variability simulations have shown that high-mobility IFQW devices have excellent immunity to  $V_T$  fluctuation compared to equivalent bulk Si FETs and are suitable for potential inclusion in future CMOS technology generations.

## Publications

- [1] B. Benbakhti *et al. Sol.-St. Elec.* **63** p14 (2011)
- [2] B. Benbakhti *et al. Microel. Eng.* **88** p358 (2011)
- [3] K.H. Chan *et al, Proc. ULIS* (2011)
- [4] DualLogic FP7  
www.ims.demokritos.gr/DUALLOGIC/
- [5] A. Asenov *J Comp. Elec.* **8** p349 (2009)