A Wideband CPW Ring Power Combiner with Low Insertion Loss and High Port Isolation

Chong Li, Ata Khalid, Vasileios Papageorgiou, Lai Bun Lok, and David R. S. Cumming

***Abstract*— In this paper we present a coplanar waveguide (CPW)-based ring power combiner that exhibits less than 0.8 dB insertion loss, better than 15 dB port match and higher than 22 dB isolation loss over the frequency range from 50 GHz to 100 GHz. Compared with the conventional 2-way Wilkinson combiner, the proposed ring power combiner replaces the resistor between the two input ports with two quasi quarter-wave CPWs, a 180º CPW phase inverter, and two resistors that lead to frequency-insensitive port isolation and wideband port match. The power combiner is realized using an electron beam-based GaAs MMIC process along with simple electron beam airbridge technology. These results agree well with 3D full-wave simulations.**

***Index Terms*—Power divider/combiner, coplanar waveguides, phase inverter, MMICs.**

I. Introduction

POWER dividers/combiners are widely used for power dividing and (or) combining, balancing and transforming circuits in RF and microwave systems. One of the most widely used dividers/combiners is the Wilkinson divider [1]. A 2-way conventional Wilkinson divider has a lumped resistor between two output ports that provides good port matching and port-to-port isolation near the centre design frequency; however, the operating bandwidth is narrow. Several modified versions of the Wilkinson divider have been demonstrated to achieve wider bandwidth using different technologies [2]-[8]. Among them, Chiu and Xue used parallel–striplines and a swap to achieve 96.5% -10 dB impedance bandwidth, 25 dB isolation, and less than 0.7 dB insertion loss at a centre frequency of 2 GHz [2]. The problem with this design is it is difficult to adapt it to standard GaAs monolithic microwave integrated circuits (MMICs). In addition, it becomes lossy at higher microwave frequencies due to the use of via holes. Simpler designs using uniplanar technologies such as coplanar striplines and slotlines were demonstrated later with similar performance [3]. However, the radial lines used for frequency independent swaps in their designs enlarge the component size that consequently increases cost and reduces efficiency. Although others have shown a similar bandwidth with miniaturized structures, such as multiple layers [4], [5] and metamaterials [6], they still showed either higher loss or complicated design and fabrication processes.

Manuscript received 13 June 2012, revised on 4 Sepember 2012.

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We have recently demonstrated a hybrid uniplanar -combination of CPWs, coplanar striplines (CPSs) and airbridges- ring power divider operating at K-band [9] that had ultra wideband operation but a much simpler design and realization process and smaller size compared to prior art [2]-[8]. However, this type of divider suffers from high insertion loss because of the transitions between CPW and CPS at the input and output ports. The excessive loss may lead to low efficiency when used as a power combiner. In this letter, we present a new power combiner design that has an even simpler design and fabrication process, wide operating bandwidth and improved efficiency. Thus, multiple such components may be cascaded to combine more signal sources and amplifiers to meet the demand for high power sources in the millimeter-wave frequency range.

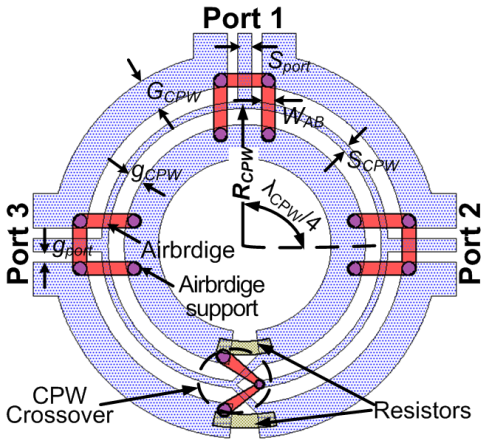


Fig. 1. Design of the proposed CPW ring power combiner for V-band and W-band operation.

II. Design and Simulation

A design layout of the proposed power combiner is shown in Fig. 1. It consists of two upper quarter-wave CPWs and two lower quasi quarter-wave CPWs, having characteristic impedance, Z_{CPW}, of $\sqrt{2}Z_0$, where Z_0 is the system impedance, configured in a ring structure. Port 1 is the output port and Port 2 and Port 3 are the input ports of the combiner. Between the two lower quasi quarter-wave CPWs is a 180º CPW phase inverter. The phase inverter has negligible phase deviation from 180º provided the ground planes are discontinuous [10]. Two parallel resistors having a resistance of $2Z_0$ are inserted between

the grounds in order to achieve good matching at Port 2 and 3. The combination of a frequency-insensitive phase inverter and resistors ensures wideband port matching and high isolation.

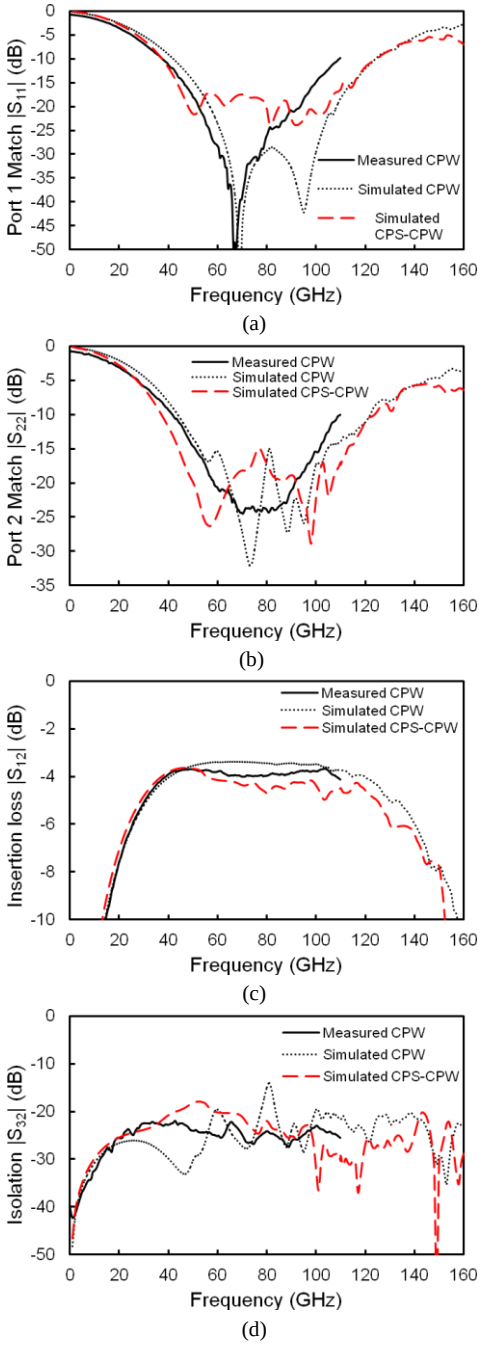


Fig. 2. Measured and simulated frequency response of the ring power combiner: (a) Port 1 return loss, (b) Port 2 return loss, (c) insertion loss ($|S_{12}|$), and (d) output isolation ($|S_{32}|$).

The design rule for this combiner is straightforward. For Z_0=50 Ω at the centre design frequency of 90 GHz, the quarter-wave length of CPWs on a semi-insulating GaAs substrate that has a relative dielectric constant of 12.9 is 320 µm [11]. The central conductor width, S_{CPW}, and the gap between the central conductor and the ground conductor, g_{CPW}, are chosen to be 10 µm and 23.5 µm, respectively, to obtain $Z_{CPW} = \sqrt{2}Z_0$, which is 70.7 Ω. For the CPW feed ports, the central conductor width, S_{port}, and the gap between the central conductor and the ground conductor, g_{port}, of the port feed are 20 µm and 15 µm, respectively, to have a characteristic impedance of 50 Ω. Other parameters are defined in Table I.

TABLE I
DIMENSIONS FOR THE PROPOSED RING COMBINER DESIGN

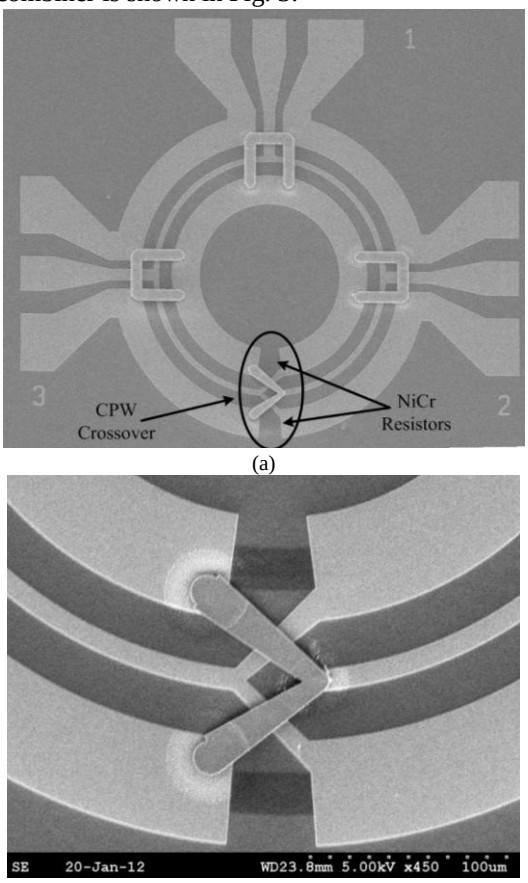
Parameter	Description of the parameter	Value
S_{CPW}	Central conductor width of CPW	10 µm
g_{CPW}	Gap between central and ground conductor	23.5 µm
G_{CPW}	Ground conductor width of CPW	50 µm
R_{CPW}	Center ring radius	205 µm
$\lambda_{CPW}/4$	Quarter wave length at centre design frequency	320 µm
H_{AB}	Height of airbridges and crossover	4 µm
W_{AB}	Width of airbridges and crossover	10 µm
t	Conductor thickness	0.4 µm

The combiner design was optimized using the full-wave electromagnetic modeling tool, Ansoft HFSS™, whose accuracy has been valid and verified up-to 220 GHz [12]. Several parameters, such as width, length, and height of the swap, size and shape of the resistors have been tuned to achieve the best overall performance of the combiner. It is found that without airbridges significant loss is generated at all ports of the combiner. Physical dimensions of the final design are given in Table I. The simulated magnitudes of S-parameters (dB) of the proposed power divider between 10 MHz and 160 GHz are plotted in Fig. 2. One can see that the combiner has an insertion loss of less than 0.5 dB from 50 GHz to 102 GHz and the port isolation ($|S_{32}|$) is better than 15 dB across the entire simulated frequency band. The port return losses are better than 15 dB over the frequency range from 52 GHz to 106 GHz for input ports ($|S_{22}|$ and $|S_{33}|$), which are slightly different due to the asymmetrical structure of the swap, and greater than 15 dB from 50 GHz to 115 GHz for Port 1 ($|S_{11}|$), respectively. Simulated S-parameters of a power combiner using hybrid CPS-CPW [9] operating in the similar bandwidth are also plotted and compared in Fig.2. It is clearly seen that with the new design, the transmission loss has improved significantly. The improved design increases the combining efficiency of the component when used as a combiner.

III. Realization and Characterization

The power combiner was fabricated on a 620 µm thick semi-insulating GaAs substrate that has a tangent loss of 0.006. All patterns were defined using electron beam lithography (EBL). The resistors were first formed using 33 nm thick nichrome (NiCr) that gave an approximate resistivity of 50 Ω/Square. For a 100 Ω resistance, the active region of the resistor had dimensions of 20 µm × 10 µm (length×width). However, another 15 µm length of NiCr extended on either side of the resistor for better contact with the subsequent deposited conductors. A 0.4 µm thick gold layer was then electron beam evaporated in order to form the CPW structures. The airbridges connecting the ground planes of the CPW and the CPW crossover were formed by EBL and a dry etch process [13]. This airbridge development process provides a high degree of

flexibility, simplicity, reliability and compatibility to the GaAs MMIC process. A scanning electron microscopy (SEM) image of the combiner is shown in Fig. 3.



(a)

(b)

Fig. 3. Scanning electron microscopy images of the fabricated CPW ring combiner (a) and the detailed CPW crossover and NiCr resistors (b). CPW transitions from 20 μm/15μm to 60 μm/40 μm in (a) were applied to compromise the 100 μm-pitch testing GSG probes.

The components were tested using a pair of DC-110 GHz probes with pitch separation of 100 μm from GGB Industries and an Agilent PNA N5250C (10 MHz-110 GHz) on a Cascade semi-automated probe station. In order to be compatible with the geometry of the test probes, CPW transitions from 20 μm/15 μm to 60 μm/40 μm were deployed at three ports. Since the input ports are orthogonal to the output port, three separate calibrations and the corresponding measurements were carried out and reconstructed to obtain the scattering parameters of the combiner. A Short-Open-Load-Reciprocal Thru (SOLR) calibration method [14] was used to calibrate the VNA system for Port 1-Port 2 and Port 1-Port 3 transmission measurements and a Line-Reflect-Reflect-Match (LRRM) calibration method was used for Port 2-Port 3 isolation measurement. The calibration substrate used was CS-5 from GGB Industries.

The measured results are plotted in Fig. 2. It can be seen that the experimental results have reasonable agreement with the simulation data. The slightly higher insertion loss, which is approximately 0.3 dB at most, is due to the CPW transitions at three ports. Minor discrepancies are visible in port match and return losses. These may result from the difference between fabricated and modeled airbridges, crossover and resistors as similarly discussed in [9]. In general, the demonstrated CPW combiner has very good performance in terms of isolation, port match, and insertion loss in a wide bandwidth.

IV. Conclusions

A new CPW ring power combiner operating in V and W bands has been demonstrated. The combiner has a uniplanar geometry which was realized using a standard GaAs MMIC process and EBL airbridge process. The overall size of the combiner is 580 μm×570 μm. Experimental results indicated less than 0.8 dB transmission loss (less than 0.5 dB from simulation), greater than 15 dB port return loss and better than 22 dB output isolation in the frequency range of 50 GHz and 100 GHz. In addition, the component has a simple design procedure and small features. This leads to wide range applications and easy integration with MMICs for efficient power dividing and combining.

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