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Titania/alumina bilayer gate insulators for InGaAs metal-oxide-semiconductor devices

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We describe the electrical properties of atomic layer deposited TiO_2/Al_2O_3 bilayer gate oxides which simultaneously achieve high gate capacitance density and low gate leakage current density. Crystallization of the initially amorphous TiO_2 film contributes to a significant accumulation capacitance increase (~33%) observed after a forming gas anneal at 400 °C. The bilayer dielectrics reduce gate leakage current density by approximately one order of magnitude at flatband compared to Al_2O_3 single layer of comparable capacitance equivalent thickness. The conduction band offset of TiO_2 relative to InGaAs is 0.6 eV, contributing to the ability of the stacked dielectric to suppress gate leakage conduction. © *2011 American Institute of Physics*. [doi:10.1063/1.3662966]

Because silicon semiconductor channels are reaching their scaling limits, III-V compound semiconductor channels coated by deposited high-k dielectrics are the subject of intense interest for high performance metal-oxide-semiconductor (MOS) devices beyond the 22 nm technology node.[1] Unlike SiO_2/Si technology, however, one of the main challenges in developing III-V based semiconductors is the difficulty of preparing high quality gate oxides with low interface defect densities.[2] Atomic-layer-deposited (ALD) Al_2O_3 is known to provide a relatively low interface defect density and an unpinned Fermi level on InGaAs (100) substrates.[3,4] A particularly interesting approach is to use (1) an InGaAs channel surface that is initially capped with an As_2 layer that can be thermally desorbed prior to gate oxide deposition[3] and (2) forming gas anneals after gate electrode deposition in order to passivate interface traps and border traps in the ALD-Al_2O_3 layer.[5] However, Al_2O_3 is a moderate-k dielectric compared to other higher-k oxides which have been studied as SiO_2 replacements,[6] and this hinders further scaling of the gate oxide capacitance density. Oxide materials with high dielectric constant such as TiO_2 have a low conduction band offset relative to a Si substrate;[7] therefore, they are not as effective in reducing leakage current as are SiO_2 and Al_2O_3. It is difficult to find a single oxide which satisfies all requirements for end-of-roadmap MOS gate dielectrics (high dielectric constant, low interface trap density, high thermal stability, etc.), making bilayer gate dielectrics an interesting option.[8] In this letter, we report electrical properties of ALD-TiO_2/Al_2O_3 bilayer dielectrics with comparison to ALD-Al_2O_3 single layer dielectrics. We also discuss structural changes in the TiO_2 layer after forming gas anneal and the spectroscopic measurement of the band alignment of TiO_2 and Al_2O_3 relative to n-$In_{0.53}Ga_{0.47}As$.

Epitaxial n-type $In_{0.53}Ga_{0.47}As(100)$ channel layers of 500 nm thickness and Si doping concentration of $2.0 \times 10^{16}\,cm^{-3}$ were grown on heavily doped n-type InP substrates by molecular beam epitaxy (MBE). The epilayers were covered *in-situ* with an approximately 80 nm thick amorphous As_2 capping layer to protect the channel surface from uncontrolled oxidation and contamination during wafer transfer from the MBE chamber to the ALD reactor. The As_2 capping layer was thermally desorbed at 380 °C under high vacuum in the ALD reactor prior to gate oxide deposition. ALD-Al_2O_3 layers were deposited at a substrate temperature of 270 °C, using trimethylaluminum (TMA) and water vapor, with a TMA pulsing first in the sequence. To fabricate the bilayer structure, ALD-TiO_2 deposition was performed at 150 °C with a H_2O/tetrakis(dimethylamino) titanium process immediately after Al_2O_3 deposition, without a vacuum break. Platinum gate electrodes of 50 nm thickness were e-beam evaporated through a shadow mask, and wafer back side contacts of 50 nm Au/20 nm Ti were deposited to reduce the contact resistance. Post-metallization forming gas (5% H_2/95% N_2) anneal (FGA) was done for 30 min at 400 °C.

Multi-frequency (1 kHz to 1 MHz) capacitance-voltage (C-V) measurements in the dark were performed on ~7 nm TiO_2/~2 nm Al_2O_3 bilayer MOS capacitors. The C-V characteristic of the as-deposited TiO_2/Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ bilayer dielectric (Fig. 1(a)) exhibits large frequency dispersion

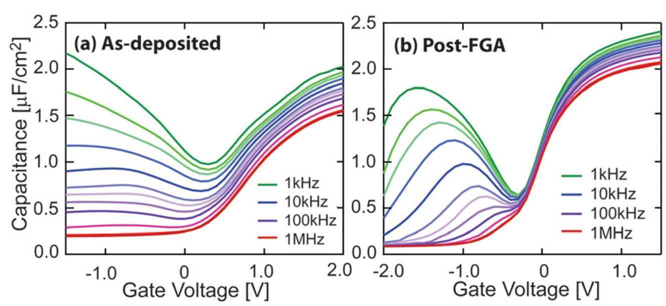

FIG. 1. (Color online) Multi-frequency (1 kHz–1 MHz) C-V curves from (a) as-deposited and (b) forming gas annealed Pt/~7 nm TiO_2/~2 nm Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ MOSCAPs.

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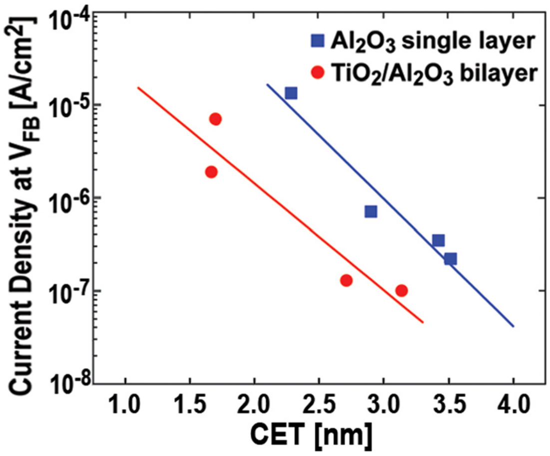

FIG. 2. (Color online) Plot of leakage current density versus CET for the Al_2O_3 single layers (●) and TiO_2/Al_2O_3 bilayers (■). The leakage currents were measured at the flatband voltage.

throughout the applied bias range and the C-V curves stretch out through depletion, which shows that as-grown oxides contain a large density of border traps and interface defects. Post-metallization FGA effectively removes and/or passivates most of the interface defect states present at the oxide/semiconductor interface, which, as a result, reduces C-V stretch-out and frequency dispersion as shown in Fig. 1(b). In addition, the flatband voltage was shifted close to the ideal value (~0.5 eV, given by the work function difference between gate metal and semiconductor), which is indicative of reduction of the oxide trapped charges. The post-metallization FGA effect on passivating defect sites has previously been reported to occur in Al_2O_3 single layer capacitors.[5,9] The key feature of the bilayer capacitors, which is different from single layer dielectrics, is that the maximum accumulation capacitance density of bilayer gate oxide increases from 1.5 μF/cm^2 to 2.0 μF/cm^2 after FGA, whereas no such effect of FGA has been observed for the single layer Al_2O_3 MOSCAPs investigated.[10]

The leakage current density across the bilayer gate dielectrics was also compared to that of Al_2O_3 single layers. Figure 2 plots the gate leakage current density measured at flatband voltage as a function of the capacitance-derived equivalent SiO_2 thickness (CET). The plot clearly shows that the addition of the TiO_2 layer gives about one order of magnitude reduction of the gate leakage current at a given CET. The addition of a physically thicker but higher-*k* TiO_2 layer creates little change in gate capacitance density but greatly suppresses gate leakage current. An electrostatic dipole formed at the TiO_2/Al_2O_3 interface can also inhibit leakage current. In Al_2O_3/TiO_2/n-GaAs devices, a dipole created between the TiO_2 and Al_2O_3 layers has been reported to enhance the leakage current compared to TiO_2/n-GaAs by reducing the effective metal/semiconductor barrier height.[11] It can be inferred that the reverse oxide stack order (TiO_2/Al_2O_3) should generate an opposite dipole, and this can increase the barrier height and as a result lower the leakage current density.

Microstructural changes were investigated in a Tecnai G2 transmission electron microscope (TEM). Figure 3(a) shows a cross-sectional TEM micrograph of the Pt/TiO_2/Al_2O_3/$In_{0.53}Ga_{0.47}As$ stack after the FGA at 400 °C for 30 min. It is difficult to resolve the interface between the two dielectrics, because both have an amorphous structure, with similar densities and average atomic numbers. After the FGA, areas with lattice fringes are observed in the TiO_2 films in both cross-sectional TEM (Fig. 3(a)) and the plan-view TEM (Fig. 3(b)), indicating full or partial crystallization of the TiO_2 layer. Analysis of selected area electron diffraction (SAED) patterns reveals that the crystalline TiO_2 is predominantly in the anatase phase (Fig. 3(c)). *In-situ* TEM analyses of the same bilayer dielectric combination on a Ge substrate show that the crystalline anatase phase TiO_2 becomes evident at an annealing temperature of 300 °C and the crystalline rutile phase starts to form at 400 °C.

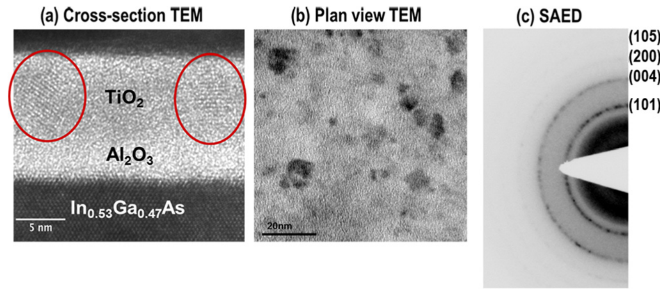

FIG. 3. (Color online) (a) Cross-sectional TEM image and (b) plan-view TEM image of TiO_2/Al_2O_3 bilayer stack. (c) Selected area electron diffraction pattern showing anatase phase predominant.

The total accumulation capacitance density, C_{acc}, is determined by several different capacitance factors, as expressed in

$$\frac{1}{C_{acc}} = \frac{1}{C_{Al_2O_3}} + \frac{1}{C_{TiO_2}} + \frac{1}{C_S + C_{it}}. \tag{1}$$

Here, $C_{Al_2O_3}$ and C_{TiO_2} are the capacitances of the Al_2O_3 and TiO_2 layers, respectively, C_S is the substrate capacitance, and C_{it} is the interface trap capacitance. The dielectric constant of anatase phase TiO_2 is reported to be as high as 78,[12] and the rutile phase TiO_2 can have a dielectric constant of up to 170 depending on crystalline orientation,[13] while the k-value of the ALD-grown amorphous TiO_2 was previously found to be approximately 32.[14] Crystallization of the TiO_2 film is expected to contribute to the accumulation capacitance increase after FGA, which was observed only in the TiO_2-containing samples. Another factor that can increase the accumulation capacitance is densification of the oxide layers during FGA, which makes the oxide layers physically thinner. Fast interface traps can also affect the measured accumulation capacitance through the interface trap capacitance, C_{it}. Quantification of these various effects of FGA on C_{acc} remains a topic of future work. The CET extracted for the bilayer MOSCAP is <1.7 nm after FGA, which includes the contributions of both the InGaAs substrate and of the capacitance of interface traps and near-interface border traps on C_{acc}. However, both bilayer and single-layer MOSCAPs have an ALD-Al_2O_3/InGaAs interface with very similar thermal history and, therefore, we may assume that the trap contributions are similar for each. We attribute most of the FGA effect on C_{acc} seen in Fig. 1 to TiO_2 microstructural changes, including crystallization.

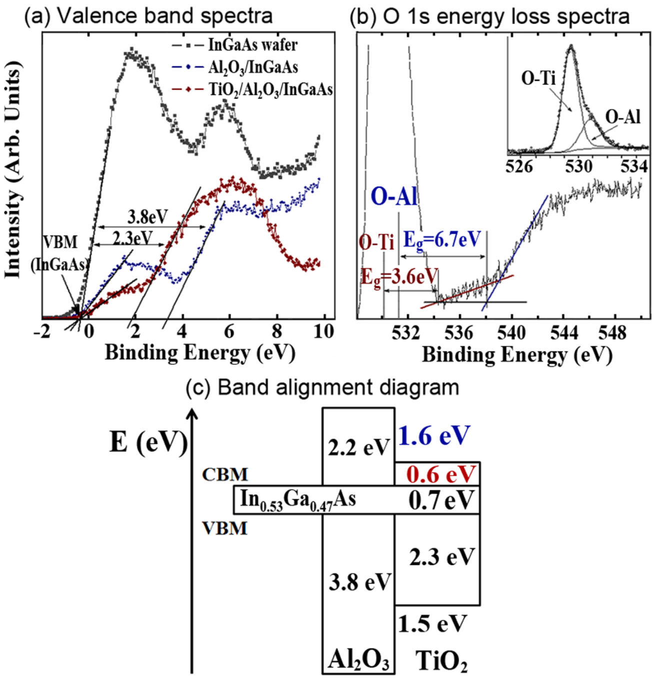

FIG. 4. (Color online) (a) Valence band spectra obtained from the InGaAs wafer, Al_2O_3/InGaAs, and TiO_2/Al_2O_3/InGaAs samples. (b) Oxygen 1s energy loss spectra for the TiO_2/Al_2O_3/InGaAs sample. The inset is a deconvoluted O 1s core-level spectrum of this sample. (c) Band alignment diagram of TiO_2/Al_2O_3/InGaAs system.

In order to investigate the effects of interface energy barriers in the bilayer structure to suppress gate leakage conduction, the band alignment of the $TiO_2/Al_2O_3/In_{0.53}Ga_{0.47}As$ system was determined by x-ray photoelectron spectroscopy measurements. The valence band offsets of the Al_2O_3 and TiO_2 films to InGaAs estimated by measuring the energy difference between the valence electrons ejected from the Al_2O_3 and TiO_2 films (second slope in Fig. 4(a)) and from the InGaAs wafer are 3.8 ± 0.2 eV and 2.3 ± 0.2 eV, respectively. The valence band offsets measured in our experiments are smaller than those calculated in a recent report,[15] but in agreement with experimental results from other researchers for individual Al_2O_3 and TiO_2 layers on InGaAs substrate.[16] Next, the bandgaps of the Al_2O_3 and TiO_2 films were determined by the O 1 s core level spectrum, as shown in Fig. 4(b). The bandgap is the energy difference between the O-Al or O-Ti peak and the beginning of the each energy loss region (the region with higher binding energies). The extracted band gap values are 3.6 ± 0.2 eV for TiO_2 and 6.7 ± 0.2 eV for Al_2O_3, which are in good agreement with literature for amorphous phase Al_2O_3 and TiO_2.[17] Based on these findings, we can plot the band alignment diagram of the TiO_2/Al_2O_3/InGaAs system (Fig. 4(c)), where the conduction band offset was calculated by the equation $\Delta E_C = E_{G,oxide} - E_{G,InGaAs} - \Delta E_V$. The conduction band offsets of the TiO_2 and Al_2O_3 with respect to InGaAs are 0.6 ± 0.2 and 2.2 ± 0.2 eV, respectively. This result indicates the ability of the physically thicker bilayer dielectric to reduce gate leakage conduction when TiO_2 is stacked on the Al_2O_3/InGaAs MOS structure.

In conclusion, we have demonstrated 1.7 nm CET with 1.9×10^{-6} A/cm^2 leakage current density at the flatband voltage with TiO_2/Al_2O_3 bilayer dielectrics. Adding a TiO_2 layer on Al_2O_3/InGaAs MOSCAPs can lower the gate leakage current by one order of magnitude, which is attributable in part to the 0.6 eV conduction band offset of TiO_2 relative to InGaAs, as well as possible oxide/oxide dipole effects. The bilayer dielectrics show a significant increase of accumulation capacitance density after FGA, and the crystallization of the TiO_2 layer appears to be responsible for the capacitance increase.

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