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Fabrication of 30nm T-gate High Electron Mobility Transistors Using a Bi-layer of PMMA and UVIII

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Abstract—**This work reports on the development and fabrication of High Electron Mobility Transistors with a gate length of less than 30nm. The T-shaped gates were realized using a two-stage "bi-lithography" process that creates a T-shaped image in a bi-layer of PMMA and UVIII. This is then transferred into SiO_2 gate support layer by a low damage dry-etch process. This method enables the fabrication of mechanically robust, ultra short T-gates to be realised.**

Keywords- HEMT; T-gate; Bi-layer; UVIII; Lithography;

I. INTRODUCTION

Due to their unparalleled high speed and low noise performance High Electron Mobility Transistors (HEMTs) based on InP substrates are of great interest as active devices in the next generation of ultra-high speed electronics operating in excess of 100GHz. Applications for these technologies include 160Gbit/s data communications [1], environmental monitoring from space in the G-band (140-220GHz) [2] and passive imaging systems enabling pilots to see through fog or finding concealed weapons [3].

In order to develop circuits for these applications a process must be developed that is capable realizing transistors capable of operating in excess of 300GHz. In addition to the required high-frequency performance many of the proposed applications require a technology that will simultaneously provide high gain and a low noise.

This combination of performance can be achieved using lattice matched HEMTs grown on an InP substrate. The use of an indium phosphide substrate allows layers with a high indium content (53%) to be grown without strain. The high indium concentration provides high electron, the lack of strain in the layer structure allows very smooth interfaces to be grown. Rough surfaces at the interfaces of the channel degrade the mobility of the electrons within the channel. Scaling the gate length gate while maintaining a low gate resistance greatly improves the high-frequency performance in two ways, better modulation of the current modulation by the gate resulting in a higher transconductance and reducing the gate capacitance. Both of these enhance the key RF figures of merit such as the cut-off frequency, f_t, and maximum frequency of oscillation, f_{max}.

In this work we report on the work carried out at the University of Glasgow developing and fabricating lattice matches HEMTs grown on InP substrates. This work complements the existing 120nm and 50nm T-gate InP based process flows previously developed at Glasgow.

II. DEVELOPMENT

There are a number of factors to be considered when developing a sub-50nm T-gate process. These include lithographically producing the T-gate of this gate length, the scaling of the layer structure to minimize short channel effects and maximize performance. The physical stability must also be addressed. In this section, these areas will be considered and the design decisions that each problem introduces will be discussed.

A. *Vertical Scaling of the Layer structure.*

As the gate length of a HEMT is reduced the ability of the gate electrode to modify the electron density within the channel is also reduced. In order to maintain control of the channel current by the gate the gate-channel separation must be reduced as the gate length is scaled. It has been suggested that a ratio of gate length to gate-channel separation of approximately 3:1 gives efficient gate control. However it has also been suggested that lowering the ratio to 2:1 leads to higher carrier velocities, this has the side effect of reducing the carriers in the within the channel and the gate recess offset must be carefully controlled.

Considering this the layer structure shown in Figure 1 was used. This comprises of a 20nm $In_{0.53}Ga_{0.47}$ As cap, this layer is highly doped to allow the formation of low resistance ohmic contact. The next layer is the un-doped $In_{0.52}Al_{0.48}As$ barrier layer with a thickness of 7.5nm. At the interface at the barrier layer and the 4nm thick un-doped $In_{0.52}Al_{0.48}As$ spacer layer is a layer of delta doping with a concentration of the order of 10^{12} cm^{-2} to provide doping for the channel.

Layer	
20nm n^+ $In_{0.53}Ga_{0.47}As$ Cap Layer	Si Doped ~10^{19} cm^{-3}
7.5 nm $In_{0.52}Al_{0.48}As$ Etch Stop Layer	Si δ-Doping (~10^{12} cm^{-2})
4nm $In_{0.52}Al_{0.48}As$ Spacer	
12nm $In_{0.53}Ga_{0.47}As$ Channel	
400nm $In_{0.52}Al_{0.48}As$ Buffer	
SI InP Substrate	

Figure 1. Layer Structure of Lattice Matched 30nm HEMT Wafer

This layer structure has a gate-channel separation of 11.5nm giving a gate length to gate-channel separation ratio of around 2.5. This makes the layer structure well scaled for a gate length of 30nm.

B. *Gate Stability Issues*

As the gate length is a reduced to achieve greater performance the gate resistance must be kept constant in order to prevent degradation of the maximum frequency of oscillation, f_{max}. This requires that the cross sectional area of the gate be maintained as the gate-length is reduced. This leads to T-shaped gates with have very large heads (typically 300nm) supported by a very small footprint making the gate unstable leading to problems during fabrication when the gate is formed by lift-off.

This has lead to the use of dielectric gate support layers such as the Si_xN_y dielectric layer used by Suemitsu et al.[4] A thin layer of dielectric material is deposited and the gate foot pattern is transferred into this layer. The dielectric layer can be used as a high definition shadow mask for the evaporation of the gate metal as well as providing support for the foot of the gate. In this work a 25nm layer of SiO_2 is used with the pattern transferred by a low damage dry etch process. This thickness has been be found to provide good support with little deformation during metallization.

C. *Electron Beam Lithography*

The T-shaped gates were defined using electron beam lithography, the tool used was a Leica EBPG-5HR beamwriter. This was operated at an accelerating voltage of 50keV and 100keV.

In order to achieve the high resolution possible a process was developed to minimize the effective beam broadening caused by forward scattering of electrons through the resist. This can done in two ways, increasing the accelerating voltage, and reducing the thickness of resist that the electrons must pass scatter through. This lead to the writing of the gate foot at 100keV and the development of a two stage-lithography process based on the PMMA/UVIII process developed at Glasgow for the fabrication of 70nm T-gates.[5] This process used a PMMA base layer to define the gate foot and a UVIII layer to define the gate head. A separation layer of Lift-Off Resist (LOR) from Microchem was included to prevent cross-linking of the PMMA and UVIII. This process is an excellent basis for a two-stage process because of the high sensitivity ratio of the two resists and the use of two separate developers . This allows the gate head and gate foot to be written separately., the gate head is written with a low dose using an accelerating voltage of 50keV and then developed. The gate foot is then written using a very high dose with an accelerating voltage of 100keV. The gate foot pattern is then transferred into the dielectric layer by a low damage dry etch process. The gate lithography process is summarized in Figure 2.

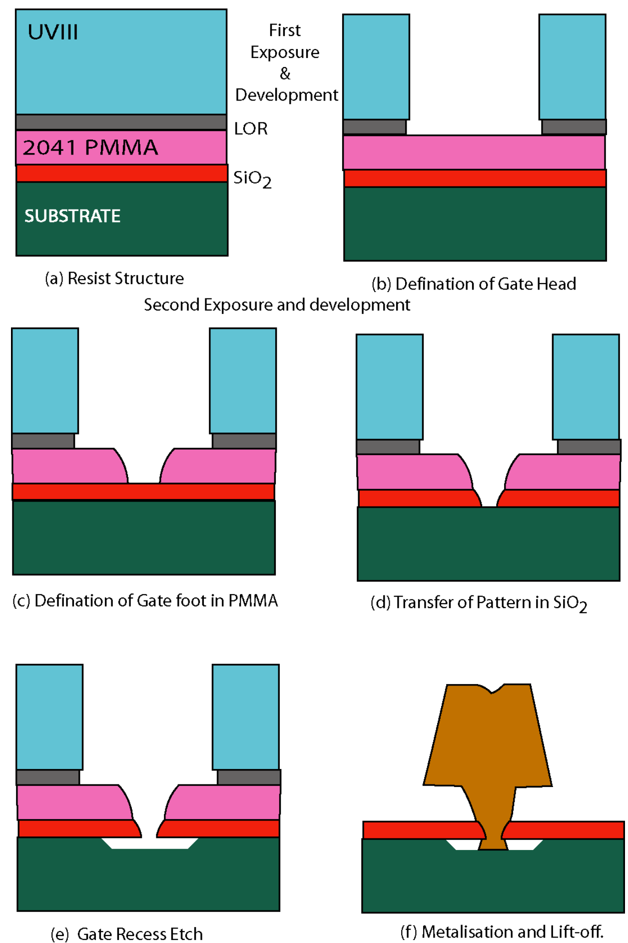


Figure 2. Figure 2 (a)-(f) Illustration of Two-stage Lithography Process.

The advantage of the two-stage lithography process is that the majority of the resist is removed during the first lithography stage. This reduces writing the gate foot to that of writing a 30nm line in a layer of PMMA 70nm thick. This is non-trivial but is more straightforward than forming T-shaped gate in 350nm of resist with a minimum feature size of 30nm. The main difficulty in this process is the alignment between the two lithography levels requiring a overlay accuracy of better than 75nm. With a suitable alignment strategy this overlay accuracy is achievable with the current e-beam tool.

III. FABRICATION

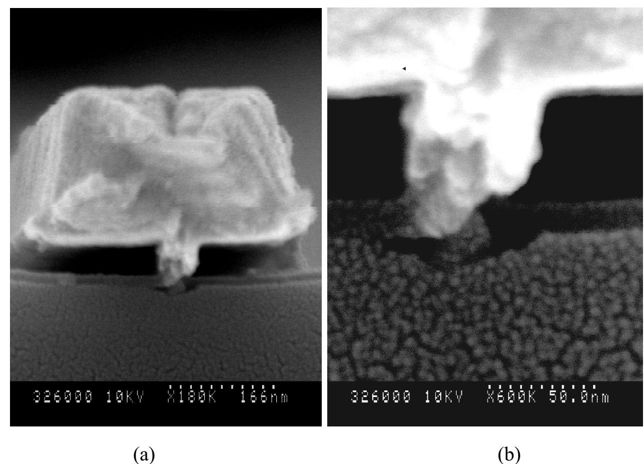
HEMT devices were fabricated using the methods described above. The devices were fabricated on a wafer with the layer design given in Figure 1. This wafer was grown by molecular beam epiltaxy by the MBE group at the University of Glasgow.

As is seen in Figure 1 the layer structure of the HEMT is very shallow, this and the use of relatively fragile materials such as $In_xGa_{1-x}As$ make the structure sensitive to damage to the material particularly at the surface. To ensure that the final device performance would not be degraded by damage to the transport characteristics of the material during fabrication each step was evaluated for damage the mobility and sheet concentration were measured before and after each process step.

The first stage in the fabrication of the HEMT after the layer structure has been grown is the deposition of the silicon dioxide layer by PECVD, this was used as it provided good thickness control and did not damage the material. The deposition of dielectric layer early in the process cycle prevents changes in the surface layer due to contaminates but most be removed for the formation of the mesa isolation level and the ohmic contacts. This was achieved using a dilute hydrofluoric acid etch. The ohmic contacts were defined by electron beam lithography and metallised with Ni:Ge:Au. The mesa isolation was performed using a non-selective etch and monitored electrically.

The initial step of the gate lithography was performed at 50keV with a dose of $80\mu C/cm^2$, this was developed in CD-26 photo-resist developer for 60 seconds. This both develops the UVIII layer and etches the LOR layer. The gate foot is then written with a 100keV beam with a minimum spot size of 12nm. The dose of this layer is substantially higher than the previous level, using a dose of $3300\mu C/cm^2$. The gate foot is developed in o-xylene for 60 seconds. The samples were then ashed in a low power barrel asher for 30 seconds prior to dry-etch to remove any resist residue that left on the surface after development. The gate foot pattern is transferred in the SiO_2 layer by dry etch using the PMMA as a mask. The dry etch process must show high selectivity of SiO_2 over PMMA and not damage the transport properties; this was achieved using CHF_3 and a RF power of 80W. This was found to successfully transfer the pattern through the SiO_2 layer and cause minimal damage. The gate recess offset was formed using a selective succinic acid based wet etch. The gate was finally formed with the evaporation of Ti:Pt:Au layers with a total thickness of 250nm. The devices were completed with the addition of Co-planar waveguide bond pads.

Figure 3 shows a cross sectional SEM image of a fabricated device. Figure 3(a) shows the complete gate region (magnified 190k times). The large gate head it clear with the stalk of the gate very well aligned in the center of the gate head. The height of the gate stalk is of the order of 60nm from the surface minimizing the parasitic gate capacitance. The SiO_2 layer is visible supporting the gate foot. Figure 3(b) shows the gate foot region at higher magnification (x600k), the gate foot is seem protruding through the gate support layer and into the gate recess region. The gate length of this particular device was 25nm. In general the gate length of devices studied varied between 25 and 30nm. The alignment between the two levels of lithography defining the head and the foot is very good with an overlay accuracy of around 25nm.



(a) (b)

Figure 3. Cross Sectional SEM images of fabricated 25nm lattice matched HEMT (a) Whole T-gate magnified 160k times (b) Gate foot region magnified 600k times

IV. CONCLUSIONS

This work has discussed the development of a fabrication process capable of fabricating lattice matched InP HEMTs with a gate length of less than 30nm. This process was fully compatible with the existing InP HEMT process flow and showed no evidence of performance degradation caused by material damage. The use of a two-stage process was seen to minimize forward scattering of electrons through the resist stack and allow gate lengths as low as 25nm to be written with a beam width of 12nm. It is anticipated; that with a tool capable of a small spot size the minimum feature size will be reduced further. The excellent overlay accuracy between the gate lithography levels of less than 25nm demonstrates the viability of this approach.

V. References

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