Sub-micron, Metal Gate, High-κ Dielectric, Implant-free, Enhancement-mode III-V MOSFETs

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***Abstract*—The performance of 300nm, 500nm and 1µm metal gate, implant free, enhancement mode III-V MOSFETs are reported. Devices are realised using a 10nm MBE grown $Ga_2O_3/(Ga_xGd_{1-x})_2O_3$ high-κ (κ=20) dielectric stack grown upon a δ-doped AlGaAs/InGaAs/AlGaAs/GaAs heterostructure. Enhancement mode operation is maintained across the three reported gate lengths with a reduction in threshold voltage from 0.26 V to 0.08 V as the gate dimension is reduced from 1 µm to 300 nm. An increase in transconductance is also observed with reduced gate dimension. Maximum drain current of 420 µA/µm and extrinsic transconductance of 400 µS/µm are obtained from these devices. Gate leakage current of less than 100pA and subthreshold slope of 90 mV/decade were obtained for all gate lengths. These are believed to be the highest performance sub-micron enhancement mode III-V MOSFETs reported to date.**

I. Introduction

Future scaling of CMOS in accordance with Moore's Law and to meet the demands of the ITRS roadmap will require various non-traditional CMOS solutions such as high-κ dielectrics, metal gates and high mobility channels [1,2]. Interest has recently focused on germanium and III-V based material systems as likely p-channel and n-channel solutions, due to their high intrinsic hole and electron mobilities respectively. Specifically, device modeling of III-V based MOSFETs through Monte Carlo simulation has demonstrated higher drive current for a given supply voltage compared with equivalent geometry Si MOSFETs [3]. In the past, the ability to reap the benefits of the high mobility III-V system for n-MOS applications has been hampered by the lack of a device quality gate oxide [4,5]. Recent work utilizing an MBE grown $Ga_2O_3/(Ga_xGd_{1-x})_2O_3$ dielectric stack (GGO) on GaAs however has demonstrated interface state densities sufficiently low to unpin the Fermi level at the oxide/semiconductor interface [6-8]. This gate stack technology, in conjunction with a suitably engineered underlying III-V layer structure, can be combined to realise enhancement mode III-V MOSFETs.

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II. Methodology

The III-V MOSFETs of this work use the "implant-free" architecture [7] shown schematically in Fig 1. The structure contains a modulation-doped, high mobility channel, surrounded by larger bandgap barriers. The carriers are thus well confined, providing charge control within the channel comparable to that achieved in ultra-thin body SOI MOSFETs. In the access regions which act like shallow source/drain extensions in conventional MOSFETs, the carriers are supplied to the channel from the ohmic contacts and the doping plane. Thermal budget constraints associated with efficient activation of implanted extensions are thereby overcome. The doping arrangement ensures that the access regions on either side of the gate have low resistance and the channel within the gate region is depleted by the work-function of a metal gate. This results in the positive threshold voltage required for E-mode digital applications, and simplified bias circuitry for analogue and RF components.

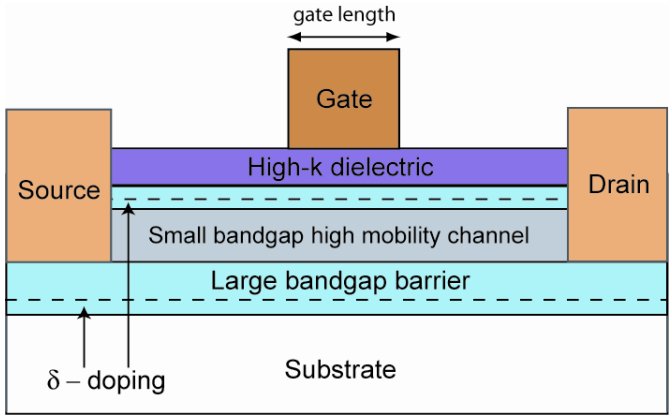

Fig. 1. δ-doped III-V MOS heterostructure device concept: A quantum well and subsequent device channel is formed in the layer with smaller bandgap than adjacent barrier layers. Carrier population of the channel is provided by δ-doping in barrier layers both above and below the channel. A gate metal with sufficiently high work function ensures depletion of channel within gate region with zero applied gate bias.

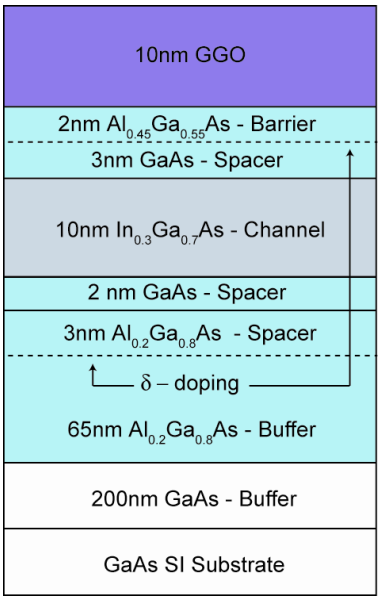

Fig. 2. Material layer structure used for MOSFET realisation.

III. PROCESS

The device heterostructure and subsequent 10nm GGO layer were grown using a dual chamber (MBE) system on a 3-inch semi-insulating GaAs substrate as detailed in [9]. The complete layer structure is shown in Fig. 2. A 10nm $In_{0.3}Ga_{0.7}As$ layer forms the compressively strained high mobility device channel. The surrounding GaAs/AlGaAs layers confine and separate channel carriers from the upper and lower δ-doped layers, reducing remote Coulomb scattering and maximizing channel mobility. MOSFET devices were realised using a two level fabrication process: Initially the gate level (Pt/Au) is defined, followed by the ohmic contact level (Ni/Ge/Au). To avoid the complication of an isolation process, a "wrap-around" gate design was adopted with which the gate contact completely encircles the drain contact. Pt was chosen as the gate contact metal due to its large workfunction. Both gates and ohmic contacts were written by electron beam lithography and subsequent metallisation patterned by the lift-off process. Prior to ohmic contact metallisation, the GGO dielectric layer was removed in the area to be metallised by wet chemical etching. Annealing of the ohmic contacts at 430C for 60s was performed post metallisation to induce alloying and form a low resistance ohmic contact to the heterostructure 2-DEG. Ohmic contact and sheet resistance figures of 0.4 Ω.mm and 550 Ω/□ respectively were extracted using the Transmission Line Method (TLM). Source-drain ohmic contact separation was set to 1.7µm for the 300nm and 500nm gate length devices, and 2.7µm for the 1µm gate length. Gates were defined mid-source-drain gap for all devices.

IV. RESULTS

DC measurements of completed devices were performed using an Agilent 4155 semiconductor parameter analyzer. Typical output characteristics (I_d:V_{ds} for given V_{gs}) for each device gate length are shown in Fig. 3. 1µm and 500nm gate length devices had source-drain bias swept from 0 to 2V, which was reduced to 1.7V for the 300nm gate device due to the onset of impact ionization beyond this voltage. Gate bias was increased in 0.2V steps from 0 to +2V for each device.

Positive threshold voltage (defined at I_d = 1µA/µm) and hence enhancement mode operation was confirmed for the three different gate length devices upon comparison of their transfer characteristics (I_d:V_{gs} for fixed V_{ds}) shown in Fig. 4. For each device, V_{gs} was swept from -0.2V to +2V, and a constant V_{ds} of 2V applied for the 1µm and 500nm gate devices, and 1.7V for the 300nm gate devices. Threshold voltage values of +0.26V, +0.16V, and +0.08V were obtained for the 1µm, 500nm and 300nm gate devices respectively.

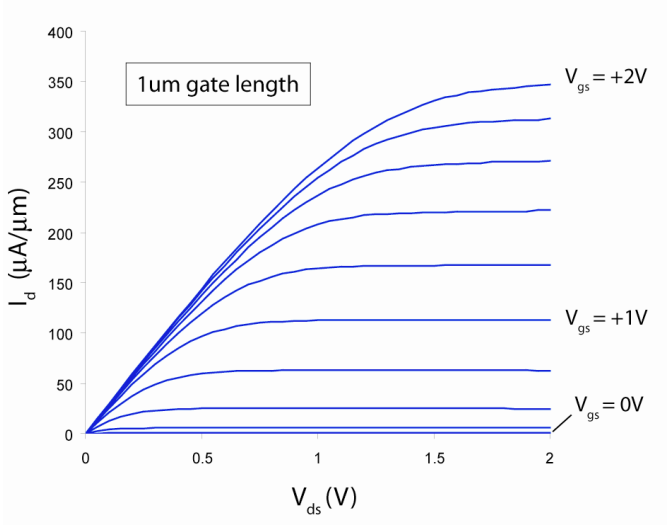

Fig. 3a. Output characteristics for 1µm gate length MOSFET with V_{ds} swept from 0 to +2V, and V_{gs} stepped 0.2V from 0 to +2V.

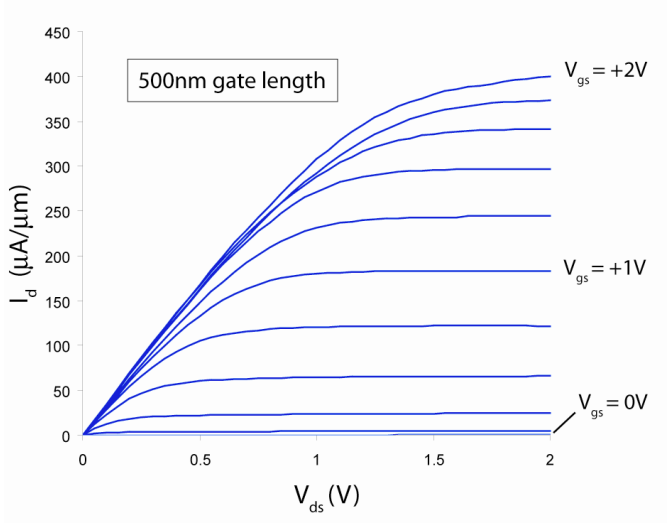

Fig. 3b. Output characteristics for 500nm length gate MOSFET with V_{ds} swept from 0 to +2V, and V_{gs} stepped 0.2V from 0 to +2V.

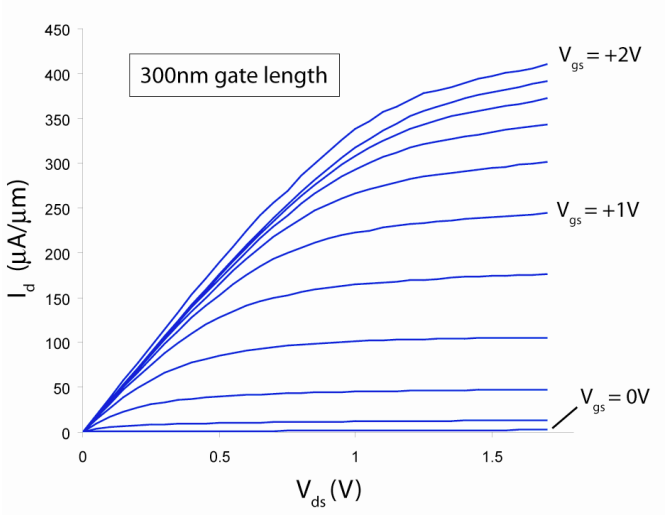

Fig. 3c. Output characteristics for 300nm gate length MOSFET with V_{ds} swept from 0 to +1.7V, and V_{gs} stepped 0.2V from 0 to +2V.

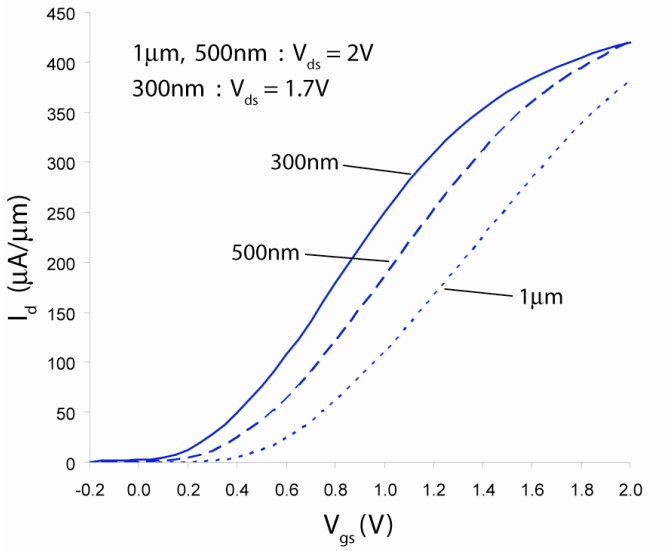

Fig. 4. Transfer characteristics for 300nm (continuous), 500nm (dash) and 1µm (dot) gate length MOSFET. V_{gs} swept from -0.2 to +2V, with V_{ds} constant at 2V for 1µm/500nm gate devices and 1.7V for 300nm gate devices.

The resistance of the DC probes used for device measurement was de-embedded to extract the extrinsic transconductance (g_m:V_{gs} for fixed V_{ds}) curves for each device (Fig. 5). Reduction of the device gate length from 1µm to 300nm produces an increase in the peak transconductance, coupled with a narrowing of the transconductance spread vs. gate bias. The gate bias at which the maximum transconductance occurs also reduces with reduced gate dimension. Peak g_m figures for devices were 310 µS/µm for the 1µm, 355 µS/µm for the 500nm, and 400 µS/µm for the 300nm gate devices. Additionally, gate leakage current from devices did not exceed 100pA, demonstrating the electrical integrity of the 10nm GGO dielectric layer across the presented bias range. Subthreshold slope was extracted from the subthreshold I_d:V_{gs} response to be ~ 90mV/decade for each of the presented gate lengths.

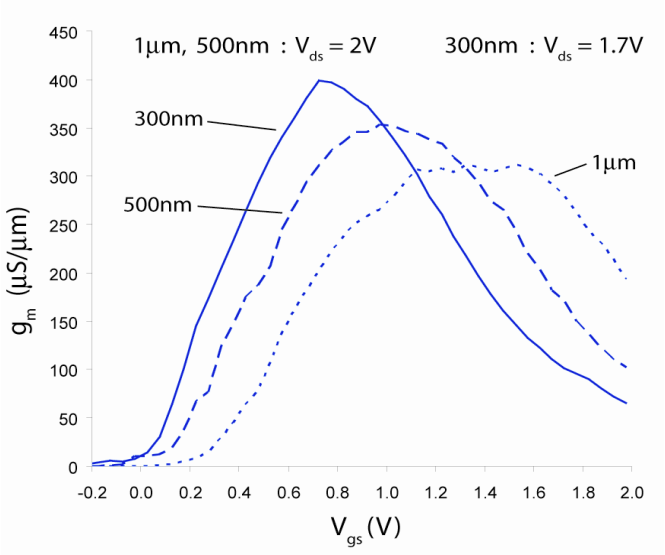

Fig. 5. Transconductance curves for 300nm (continuous), 500nm (dash) and 1µm (dot) gate length MOSFET. V_{gs} swept from -0.2 to +2V, with V_{ds} constant at 2V for 1µm/500nm gate devices and 1.7V for 300nm gate devices.

V. DISUSSION

Comparison of the results for the 1µm, 500nm and 300nm gate length devices indicates similar maximum drain current, gate leakage current and subthreshold slope. A reduction in threshold voltage and an increase in transconductance are also demonstrated as the physical gate length is reduced. Due to the varied source/gate separation for each of the 3 gate lengths however, the intrinsic transconductance must be extracted for each device to allow a direct comparison of their performance. Intrinsic transconductance curves are extracted by de-embedding the source access resistance using the expression:

$$g_{\mathrm{m-int}} = \frac{g_{m-ext}}{1 - g_{m-ext} R_s}$$

where $g_{m\text{-}int}$ is the intrinsic transconductance, $g_{m\text{-}ext}$ is the extrinsic transconductance i.e. measured, and R_s is the source resistance. The magnitude of the source resistance is calculated as the sum of the contact resistance plus the lateral resistance of the access region. Using an ohmic contact resistance of 0.4 Ω.mm and sheet resistance of 550 Ω/□ (obtained from the TLM data mentioned above), source resistances were calculated to be 0.87 Ω.mm for the 1µm, 0.73 Ω.mm for the 500nm, and 0.78 Ω.mm for the 300nm gate length devices. The resulting gate bias dependent intrinsic transconductance is shown in Fig 6. A similar trend is observed between extrinsic and intrinsic transconductance traces (Fig . 5. and Fig. 6.) where increased transconductance results from reduced gate length. This is indicative of non-equilibrium transport effects which are predicted to lead to high drive currents in suitably scaled sub-100 nm gate length devices [3].

Peak intrinsic transconductance values along with threshold voltage as a function of gate length are summarised in Fig. 7.

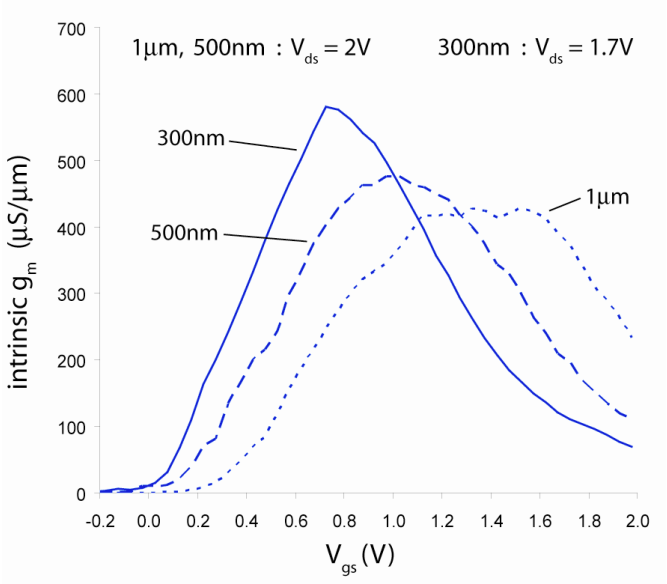

Fig. 6. Intrinsic transconductance for 300nm (continuous), 500nm (dash) and 1µm (dot) gate length MOSFET. V_{gs} and V_{ds} indicate applied i.e. extrinsic bias.

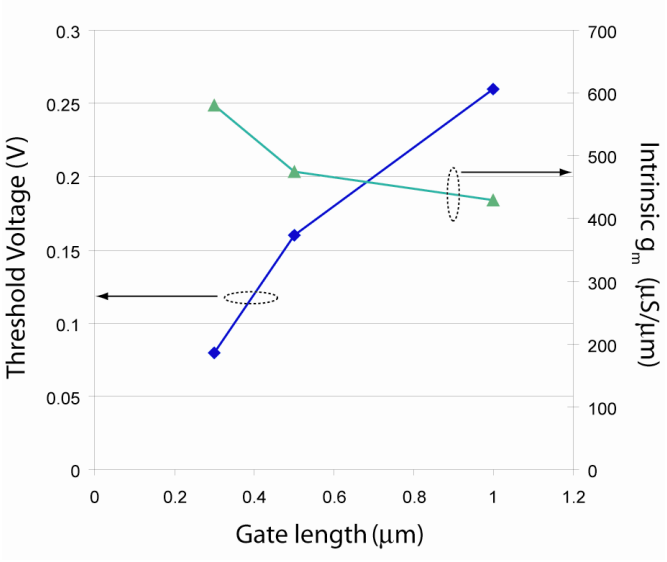

Fig. 7. Threshold voltage and intrinsic transconductance vs. gate length

The observed value and shift in threshold voltage with gate length provides information about the scalability of this device structure. The reduction of threshold voltage with gate length suggests a limit of ~200nm gate length for enhancement mode operation for the layer architecture of Fig 2. Below this dimension, modification of the material structure, most likely a reduction in the thickness of the 10nm GGO dielectric layer, thinning of the barrier layer above the channel and a modification to the doping strategy will be required for well scaled sub-200 nm gate length devices.

VI. Conclussion

300nm, 500nm and 1µm gate length enhancement mode, implant free III-V MOSFET device performance is reported. Enhancement mode operation is maintained across the three gate lengths with a reduction in threshold voltage from +0.26 V to +0.08 V as the gate dimension is reduced from 1 µm to 300 nm. An increase in transconductance is also observed with reduced gate dimension. Maximum drain current of 420 µA/µm, gate leakage current of less than 100pA and subthreshold slope of 90 mV/decade were obtained for devices along with extrinsic transconductance of 400 µS/µm. The gate length dependence of intrinsic transconductance suggests the onset of non-equilibrium transport effects for the smaller gate lengths, as predicted in the past by simulation. The impact of gate length on threshold voltage suggests a modification of the device design will be essential for the realisation of sub-100nm gate length devices to fully exploit the high mobility channel III-V materials. Nevertheless, we believe these to be the highest performance sub-micron enhancement mode III-V MOSFETs reported to date which show significant promise as a future aggressively scaled nMOS solution.

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