50-nm T-Gate Metamorphic GaAs HEMTs With f_T of 440 GHz and Noise Figure of 0.7 dB at 26 GHz

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***Abstract*—GaAs-based transistors with the highest f_T and lowest noise figure reported to date are presented in this letter. A 50-nm T-gate $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ Metamorphic high-electron mobility transistors (mHEMTs) on a GaAs substrate show f_T of 440 GHz, f_{max} of 400 GHz, a minimum noise figure of 0.7 dB and an associated gain of 13 dB at 26 GHz, the latter at a drain current of 185 mA/mm and g_m of 950 mS/mm. In addition, a noise figure of below 1.2 dB with 10.5 dB or higher associated gain at 26 GHz was demonstrated for drain currents in the range 40 to 470 mA/mm at a drain bias of 0.8 V. These devices are ideal for low noise and medium power applications at millimeter-wave frequencies.**

***Index Terms*—High-electron mobility transistor (HEMT), low noise, metamorphic, metamorphic high-electron mobility transistor (mHEMT), millimeter-wave imaging, nanometer gates, short gate.**

I. Introduction

HIGH indium concentration high-electron mobility transistors (mHEMTs) on GaAs substrates are an attractive transistor technology for millimeter-wave applications as they have the potential to combine the outstanding millimeter-wave gain and low noise performance of InP-based HEMTs [1]–[3] with the advantages of economies of scale and robustness offered by conventional GaAs processing [4]–[7]. In this work, we show 50-nm T-gate GaAs mHEMTs with the highest f_T of any GaAs-based three terminal device reported to date. Further, these devices have the lowest noise figure reported for any 50-nm gate length HEMT technology. These results clearly indicate the potential of aggressively scaled 50-nm length GaAs mHEMTs as viable candidates for array-based millimeter-wave imaging and sensing applications where low chip cost will be an important driver in determining application adoption.

II. Device Realization

The double delta-doped $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ metamorphic HEMT structure on a GaAs substrate scaled for 50-nm gate length devices is shown in Fig. 1. The double delta doped strategy was used to increase drive current, reduce access resistance and enhance linearity [8]. The 1200-nm metamorphic buffer graded linearly from GaAs to $In_{0.53}Ga_{0.47}As$ and followed by a 72-nm-thick $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ superlattice prior to the growth of the device layers.

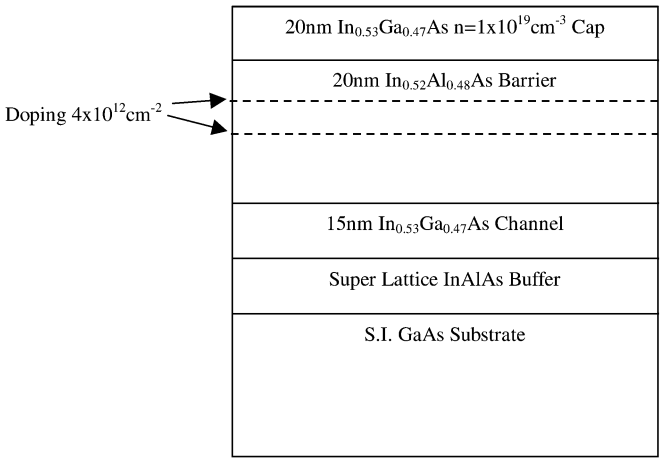

Fig. 1. Double-delta-doped $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ Metamorphic on a GaAs substrate.

After selective cap removal using a succinic-acid-based wet etch, room-temperature Hall mobility measurements yielded typical electron sheet charge density of 2.31×10^{12} cm^{-2} and a mobility of 6470 cm^2/Vs at room temperature. The relatively low value of mobility is most probably due to the double delta-doping strategy which increases ionized impurity scattering, however this does not compromise either dc of RF device performance, as shown below.

The device process flow begins with mesa isolation using an orthophosphoric acid/hydrogen peroxide/water (1:1:100)-based wet chemical etch. An isolation current of less than 200 pA/mm at 2 V was routinely obtained for an etch depth of 65 ± 5 nm (determined by atomic force microscopy), indicating high quality molecular-beam epitaxy growth of the mHEMT virtual substrate.

Ohmic contact resistances as low as 0.06 Ω·mm were obtained using an annealed 150-nm-thick Au:Ge:Ni based metallization. Devices were realized using a 1.5-μm source drain separation between which 50-nm gate length T-gates were aligned using a Leica EBPG5-HR 100 electron beam lithography tool operating at 100 keV and a UVIII/LOR/PMMA resist stack [9]. A pH5.5 selective succinic acid: ammonia hydrogen peroxide: water wet chemical etch was used to form the gate recess, prior to the deposition of 200-nm-thick Ti:Pt:Au gate metallization. A photograph of the completed device is shown in the inset of Fig. 5.

Fig. 2 shows a scanning electron microscope (SEM) image of the unpassivated 50-nm T-gate profile after metallization

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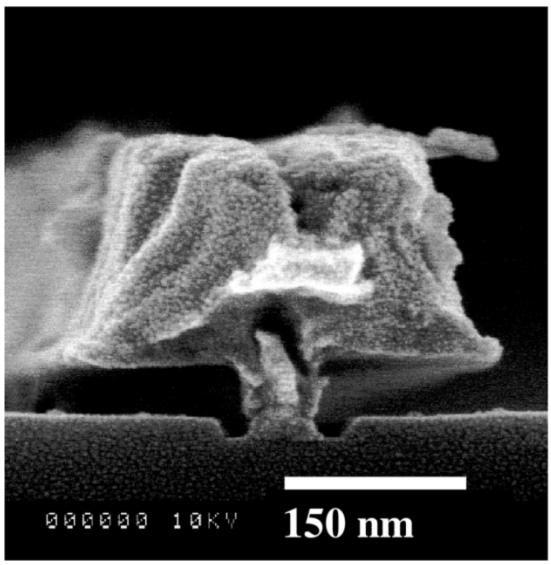

Fig. 2. Cross-sectional SEM of a 50-nm T-gate profile after metallization and liftoff.

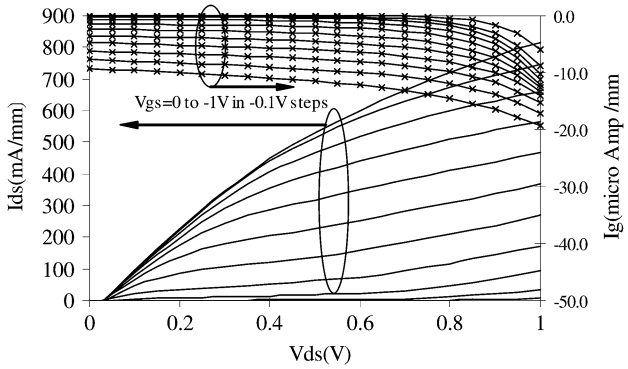

Fig. 3. Output characteristics of a two-finger 50-μm gate width, 50-nm gate length T-gate m-HEMT showing $I_{\rm dss}$ of 815 mA/mm. Gate leakage current of less than 20 μA/mm is observed across the operating range of the device $V_{\rm ds}$ up to 1.0 V and $V_{\rm gs}$ from 0 V to -1.0 V in -0.1-V steps.

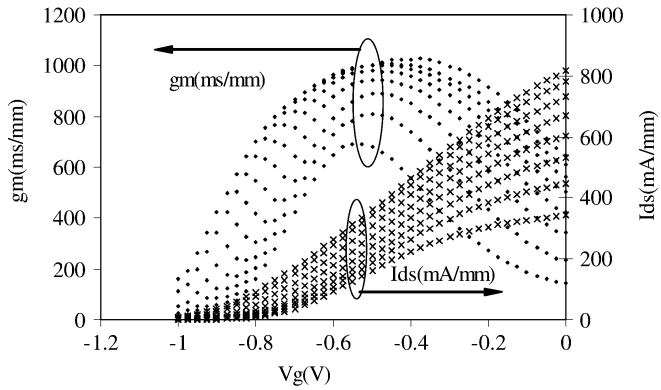

Fig. 4. Transfer characteristics of a two-finger 50-μm gate width, 50-nm gate length T-gate m-HEMT, a peak transconductance (g_m) of 1028 mS/mm was obtained, $V_{\rm ds}$ measured from 1 to 0.3 V in -0.1-V steps.

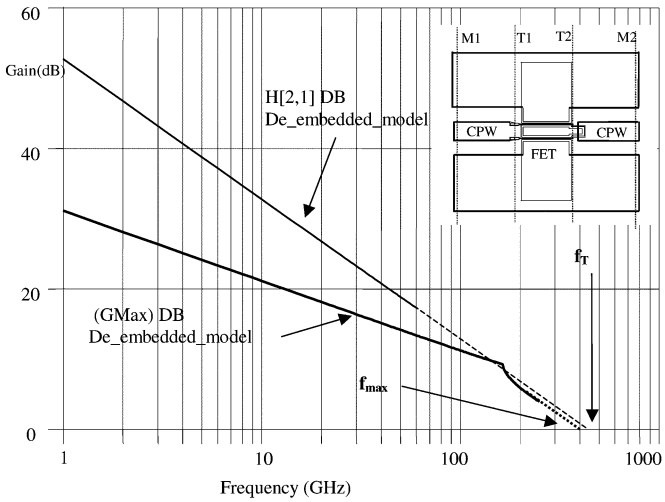

Fig. 5. RF performance of a two-finger 50-μm gate width with a 50 nm gate length T-gate m-HEMT, the device showed f_T of 440 GHz and $f_{\max}$ of 400 GHz. Inset shows diagram of the device and the definition of measurement reference planes for determination of f_T and $f_{\max}$. Insert, measurement reference planes at the probe tips M1 and M2. To de-embed the influence of the coplanar waveguide feedlines from the *S*-parameter measurements and thereby shift the measurement reference planes to the active device T1 and T2.

and liftoff. Finally, 50-Ω coplanar waveguide bondpads were defined to enable on-wafer characterization of the completed devices.

III. Device Performance

DC and RF characterization was performed using a probe station and on wafer RF probes from Cascade MicroTech. Typical dc output and transfer characteristics of a 2×50 μm wide device are shown in Figs. 3 and 4, respectively.

The dc performance metrics include $I_{\rm dss}$ of more than 800 mA/mm achieved at a drain bias, $V_{\rm ds} = 1.0$ V ($I_{\max}$ of 930 mA/mm was obtained), pinchoff voltage of -1.0 V, gate leakage current of less than 20 μA/mm (Fig. 3), peak extrinsic dc transconductance (g_m) of greater than 800 mS/mm for gate biases in the range -0.2 to -0.8 V (Fig. 4).

On-wafer *S*-parameter measurements were performed from 0.04 to 60 GHz, using an Anritsu 360 B Vector Network Analyzer and on-wafer RF probes from Cascade MicroTech. Calibration was performed using a Cascade Microtech Impedance Standard Substrate (ISS) and the LRRM technique which placed the measurement reference planes at the probe tips M1 and M2 (see inset of Fig. 5). To de-embed the influence of the coplanar waveguide feedlines from the *S*-parameter measurements and thereby shift the measurement reference planes to the active device T1 and T2 (see inset of Fig. 5), the measured *S*-parameters were fitted to a standard lumped element equivalent circuit model including CPW transmission lines at the input and output. This modeling yielded CPW line lengths of 230 μm and 230 μm at the device input and output respectively—In line with the physical geometry of the device. Following this de-embedding procedure, f_T and $f_{\max}$ were determined from the measured *S*-parameters. Fig. 5 shows the results of this analysis, yielding an f_T of 440 GHz and $f_{\max}$ of 400 GHz—To our knowledge, the highest f_T value reported to date for a GaAs-based three terminal device (previous best is 340 GHz [10]), and the highest $f_{\max}$ reported for 50 nm and shorter gate length transistor (previous best is 330 GHz [11]).

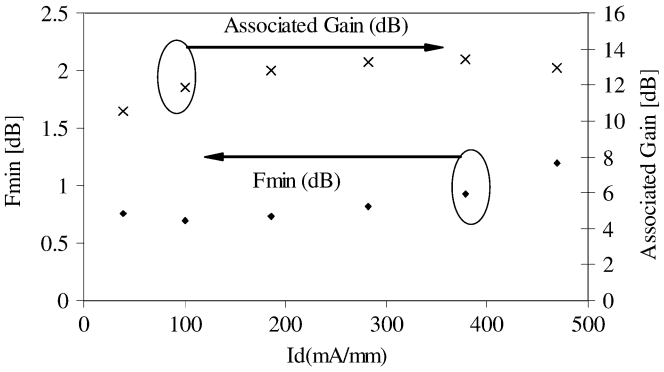

Fig. 6. Minimum noise figure and associated gain as function of drain current density$I_{\rm ds}$ (mA/mm) at 26 GHz of a two-finger 50-μm gate width 50-nm gate length T-gate m-HEMT biased at $V_{\rm ds} = 0.8$ V. The device showed less than 1.19-dB noise parameter and associated gain of higher than 10.5 dB at 26 GHz across a drain current range from 40 to 470 mA/mm.

The minimum noise figure and associated gain of 2×50-μm-wide devices were characterized using HP8510C Vector Network Analyzer, Agilent N4002A 26-GHz noise source and 2–26-GHz ATN NP5B Noise Parameter System. Fig. 6 shows the minimum noise figure and associated gain at 26 GHz with applied drain bias $V_{\rm ds} = 0.8$ V as a function of drain current from 40 to 470 mA/mm. Across this bias range, the devices showed minimum noise figure of less than 1.19 dB and associated gain of greater than 10.5 dB, with best performance of 0.7 dB minimum noise figure and 13.5 dB gain at drain current of 185 mA/mm. This performance arises from the aggressive scaling of the device vertical architecture which results in low access resistance, large drain current and high transconductance across a wide range of gate bias ranges (as shown in Fig. 4). We believe this noise data is world leading for a GaAs-based transistor technology.

IV. Conclusion

In this letter, we reported the performance of 50-nm T-gate $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ mHEMTs with excellent dc and RF characteristics. At dc, $I_{\rm dss}$ of 815 mA/mm and g_m of 1028 mS/mm were achieved. At RF, the devices exhibit f_T and $f_{\rm max}$ 440 and 400 GHz respectively, to our knowledge the highest f_T to date for any GaAs-based three terminal device. In addition, the devices have minimum noise figure of 0.7 dB and associated gain of 13 dB at 26 GHz, at drain current of 185 mA/mm. A minimum noise figure of less than 1.19 dB and associated gain greater than 10.5 dB at 26 GHz was demonstrated across a wide range of $I_{\rm ds}$ from 40 to 470 mA/mm. We believe this noise data is world leading for a GaAs-based transistor technology. These dc and RF performance metrics makes the technology ideally suited for both low noise and medium power millimeter-wave monolithic microwave integrated circuits applications.

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