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Programmable Active Pixel Sensor to investigate neural interactions within the retina

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ABSTRACT

Detection of the visual scene by the eye and the resultant neural interactions of the retina-brain system give us our perception of sight. We have developed an Active Pixel Sensor (APS) to be used as a tool for both furthering understanding of these interactions via experimentation with the retina and to make developments towards a realisable retinal prosthesis. The sensor consists of 469 pixels in a hexagonal array. The pixels are interconnected by a programmable neural network to mimic lateral interactions between retinal cells. Outputs from the sensor are in the form of biphasic current pulse trains suitable to stimulate retinal cells via a biocompatible array. The APS will be described with initial characterisation and test results.

Keywords: APS, neural network, lateral interactions, retinal implant, retinal prosthesis.

1. INTRODUCTION

Light arriving in the eye and the following perception of the world around us is not a straight forward process. The retina is a multilayered neural structure that lines the back of the eye. Light is detected by the photoreceptors at the back of the retina, converting photons into a neural signal. Before reaching the brain this signal is processed by the various layers of laterally and radially interconnected cells that combine signals from many photoreceptors. Ganglion cells near the inner surface of the retina send the signals to the brain via the optic nerve. Our understanding of the processes occurring within this visual pathway is important to developments in brain science. The significance of the lateral interactions between cells is of particular interest in the development of a retinal prosthesis. Two of the most common forms of blindness, age related macular degeneration and retinitis pigmentosa, cause degeneration of the photoreceptor cells. An electronic device that replaces the functionality of these cells can restore some vision to sufferers. This has been proven possible with implants produced by various independent groups [1-4]. Implants are possible at various locations along the visual pathway; epiretinal, subretinal and cortial implants have all been tested [5]. Depending on the location of the implant some parts of the pathway are inevitably bypassed. In an epiretinal implant, on the inner surface of the retina, the lateral and radial interactions between cells will be absent. Our program of work looks to develop key technologies to examine some of the long distance lateral interactions. We present an APS that functions as a combined image sensor, lateral neural network and ganglion cell stimulator.

The APS images the visual scene like a regular CMOS sensor. Though where a normal sensor might output a voltage, we use frequency modulated current waveforms that can stimulate the sort of fast action potentials seen with signals from the retina. The output stage for each pixel produces pulse trains suitable for stimulating ganglion cells at the right frequency for the level of illumination. With many pixel outputs connected to the retina via a dense microelectrode array it should be possible for the brain to perceive the visual scene. It is estimated around 500-600 or more pixels would allow people to walk down the street or recognize a face [6-7]. With 469 pixels, the APS we have designed is near this target. Some of the lateral connections between cells in the retina are replicated by a programmable neural network. Connections from pixel to pixel perform an edge enhancing effect.

The chip has been incorporated into a test system and characterised. Initial test results are positive, proving all round functionality of the chip. Here we present an overview of the chip design and the test results to date.

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2. SENSOR DESIGN

This is the second chip within this program of research [8]. Over the course of the program an incremental design and development route has been used. Building from the foundation of the first design we have made several advances: a large increase in the number of pixels and their arrangement, inclusion of a neural network within the chip and refined output pulse generation which is included for every pixel.

Figure 1 shows a block diagram of the pixel architecture. An integrating photodiode is used as the sensing element. This is followed by a neural network image processing stage and sample and hold circuit which feed into a voltage controlled oscillator (VCO) block. The VCO output sets the frequency of a biphasic pulse output driver for each pixel, which is individually connected to an electrode. The frequency of these pulses represents the brightness of a point in the image.

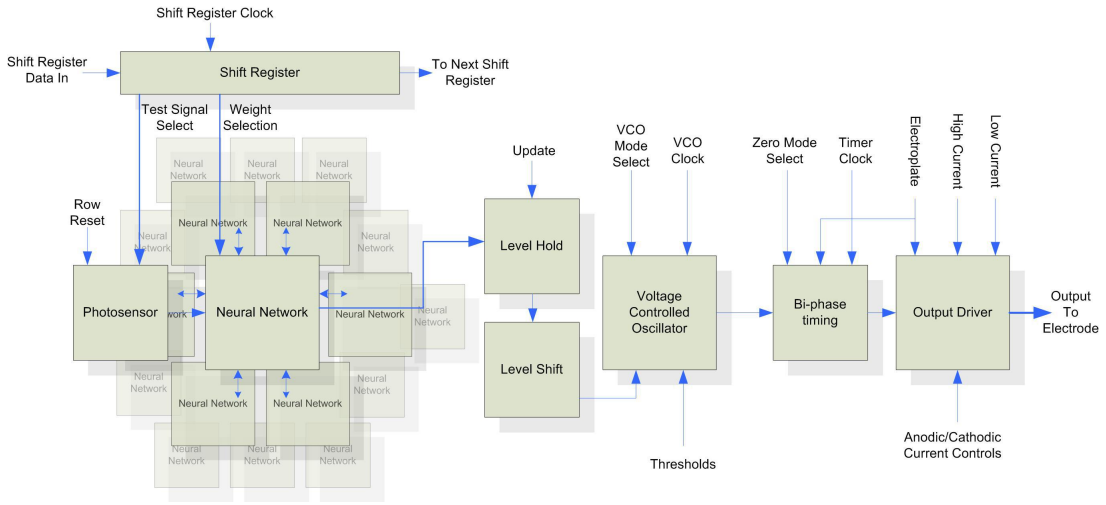

Fig 1. A block diagram of the sensor architecture from photosensor through to output drivers.

2.1 Pixel Array

The first development was to scale up the number of pixels from 100 to 469. This number is chosen to neatly form a hexagonal close packed pixel configuration. An additional 78 pixels surround the hexagonal array to complete the neural network and eliminate any edge effects. These pixels are not output. Light sensing cells within the retina naturally form up in a hexagonal pattern [9]. As technology size reduces, the aim is to match this arrangement with both the sensing elements and output electrodes. The spacing of the pixels centre to centre is 107.5µm. Light is detected and converted to an electrical signal by a charge integrating photodiode and source follower configuration as in a regular APS. Light incident upon the sensor creates a photocurrent within the pixel that is proportional to the intensity. The charge created is collected as a voltage signal at the photodiode. The relatively small opening to the photodiode of 11.4µm by 17.1µm gives a fill factor of only 1.9% however this is an acceptable sensitivity for imaging the average visual scene at a low frame rate. It is also possible to set any pixel to use a test signal in place of the photodiode. This feature can be both used in initial testing of the design or to program simple stimulation patterns into the array.

2.2 Neural Network

It is well accepted that some neural processing of the visual scene takes place within the retina before information is passed via the optic nerve to the brain [9]. As discussed in the introduction a retinal implant may bypass some neural processing. Elements of this processing are replicated on the chip by a programmable neural network. Experimentation with this will help develop a better understanding of retina-brain neural system. A target area for this neural network is to replicate the lateral connections of the horizontal cells over a significant area of the retina.

The neural network is located within the pixel array following on in the signal chain after the photodiode. A single layer neural network is implemented, designed to perform an edge detection effect that can be used to sharpen the image to varying degrees. This is achieved on a pixel by pixel basis using equation 1.

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$$Output = LightIntensity - \sum_{i=1}^{6} W_i \times NeighbourIntensity_i \quad (1)$$

W_i is the selected weight in a neighbouring pixel. The measure of intensity comes from the photosensor voltage which is inversely proportional to the light intensity. LightIntesity is that of the pixel whose output is to be calculated. $NeighbourIntensity_i$ is the light intensity in the 6 neighbour pixels. Output is a voltage to be produced for every pixel.

This function is implemented using current sources and sinks feeding into a current summing node within each pixel. The voltage output from the photosensor is used to generate a current that is mirrored to its 6 neighbouring pixels. This mirrored current is weighted for each neighbour using any combination of a 1/6th, 1/12th, 1/24th or 1/48th as set by a programmable register within each pixel. The weighted currents arriving from the neighbours are mirrored into a summing node and subtracted from the non-weighted current. The remaining current is either sourced or sunk through resistors connected to power (212kΩ) and ground (565kΩ) as in figure 2. The voltage produced at this node is the Output defined in equation 1. This sets zero or 'dark' at 2.326 volts (3.3 volt process) and gives a preferential voltage range to positive or 'bright' results (lower voltages). Negative results are suppressed.

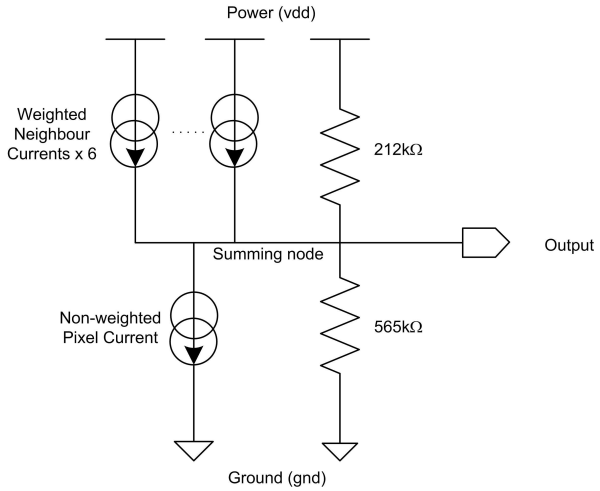

Fig 2. A simplified schematic of the neural network summing node.

2.3 Sample and Hold and Voltage Controlled Oscillator

A requirement of the chip is for continuous operation and output. The refresh rate is fully customizable to suit the imaging conditions. Typical frame rates are between 10 to 100 fps. A global pixel reset is used between integrations in place of the standard APS rolling shutter approach. This eliminates any artefacts in the image that could be created by the neural network seeing a mix of two frames. To maintain the same image between resets a storage capacitor is used to retain the output from the neural network. This stored value is updated shortly before reset of the photodiode.

The stored voltage is buffered to the input of the VCO stage by a simple amplifier with an NMOS source follower in the feedback loop. This buffer suppresses any remaining negative range from the neural network sum and preserves the stored voltage for the VCO.

The VCO takes the buffered voltage output and converts it to a square waveform, the frequency of which is determined by the input voltage. With this chip we have developed the added feature to choose between two frequency ranges ~0-50Hz or ~0-100Hz without changing thresholds or clock frequencies. This gives the option to increase the apparent dynamic range to suit the brightness of the visual scene. The smaller frequency range is still useful to retain good resolution at low frequencies. Figure 3 shows a schematic diagram of the VCO. This circuit requires two stages, a switched capacitor amplifier and a window comparator. Output frequency is a function of the step size of the switched capacitor circuit. The option to vary the output frequency is achieved by switching in an extra capacitor (C3Sel) to change the relative step size. A reset transistor is included that shorts the capacitor C3 this gives the VCO a known

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condition on power up and can be used to stop biphasic output from the chip. All other aspects of this circuit block remain the same as in the first chip of our program described previously [8].

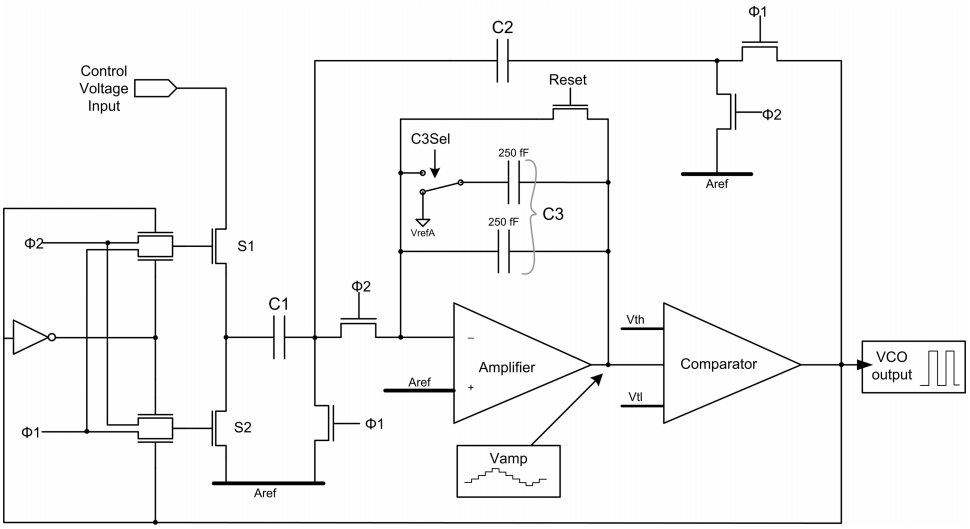

Fig 3. Voltage Controlled Oscillator simplified schematic

The VCO can be modelled with some simple equations. The frequency of oscillation is given by

$$f = \frac{1}{2\left(\frac{\Delta Vthresh}{\Delta Vstep}\right)\cdot \Phi_{PERIOD}} \tag{2}$$

Where $\Delta Vthresh = Vth - Vtl$ (High, Vth and low, Vtl comparator thresholds)

Φ_{PERIOD} is the period of the Phi clocks ~507μsec (to give the ideal freq. range), and ΔVstep is the voltage steps of Vamp. Positive and negative steps are the same size. This is given by

$$\Delta Vstep = \frac{C2(Vcp - Vref) + C1(Vref - Vcntl)}{C3} \tag{3}$$

Vcp is the positive comparator output voltage, Vcntrl is the input control voltage from the neural network and Vref is the VCO reference voltage which is set mid way between Vdd and Gnd., C1,2 and 3 are the capacitor values C2 = 10.15fF C1 = 26.00fF and C3 = 250fF or 500fF

Equations 2 and 3 demonstrate how changing the value of C3 alters the VCO operation. Fine tuning of the frequency range of operation can be performed by altering the threshold values.

Area restrictions in the pixel necessitate the use of small value capacitors. This will inevitably lead to differences in the frequencies generated by neighbouring pixels. The small capacitor sizes also mean high KTC noise that will cause the output frequency to vary by a small amount (jitter). The KTC noise for the smallest capacitor (C2=10fF) used is 643μV.

2.4 Biphasic Output Drivers and Electroplate

The pulse strength needed to stimulate ganglion cells within the retina varies with experimental conditions and can be dependent on the characteristics of the electrodes used. It is also of interest to experiment with pulse shape and charge balance. For these reasons as much flexibility as possible has been included in the design of the output driver circuits. This includes a high and low current mode to expand the possible range of outputs while retaining sensitive control at low currents.

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A timing circuit generates the control signals needed for the bi-phase output driver. It consists of 5 D-type flip-flops with a series of NAND, NOR and Inverter gates. Figure 4 shows the desired biphasic waveform and the control signal phases. The timing relationship of the bi-phase pulse width (t1) to the inter phase delay (t2) is fixed by the circuit architecture, but the exact value of t1 and t2 is determined by the timer clock frequency used. The times given in the figure below are for a typical master clock frequency of 10 kHz.

A second stage of the circuit contains controllable current sources and sinks that drive fixed current pulses off chip during the anodic and cathodic pulse phases. The intention is to push and pull a given amount of charge from the electrodes to stimulate the ganglion cells. This charge balance is important to avoid any damage to retinal cells due to build up of charge. An optional 'Zero' feature is also included to aid discharge of the electrodes to a mid rail reference voltage. This control, if selected, is active whenever the driver is not outputting a current, including the short inter phase delay. In normal operation charge balance can be achieved by independent tuning the anodic and cathodic currents.

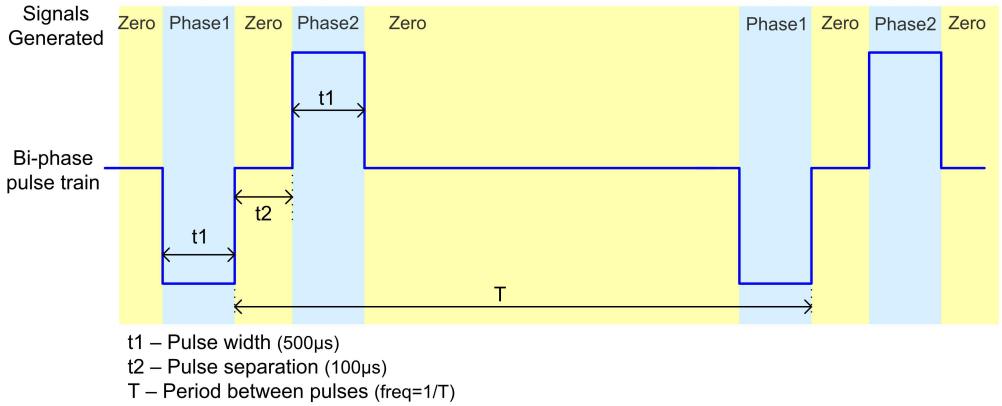

Fig 4. An example of two biphasic pulses with timer circuit phases overlaid.

This circuit uses a method similar to the neural network to generate reference currents that are then mirrored into switchable current sources and sinks that connect to bond pads. Switching is achieved by pulling the mirroring node to the appropriate rail (vdd, gnd) to turn off the output current. The bi-phase timing circuit is used to control the switches, providing a complete biphasic pulse. The figure 5 is a representation of the circuit schematic.

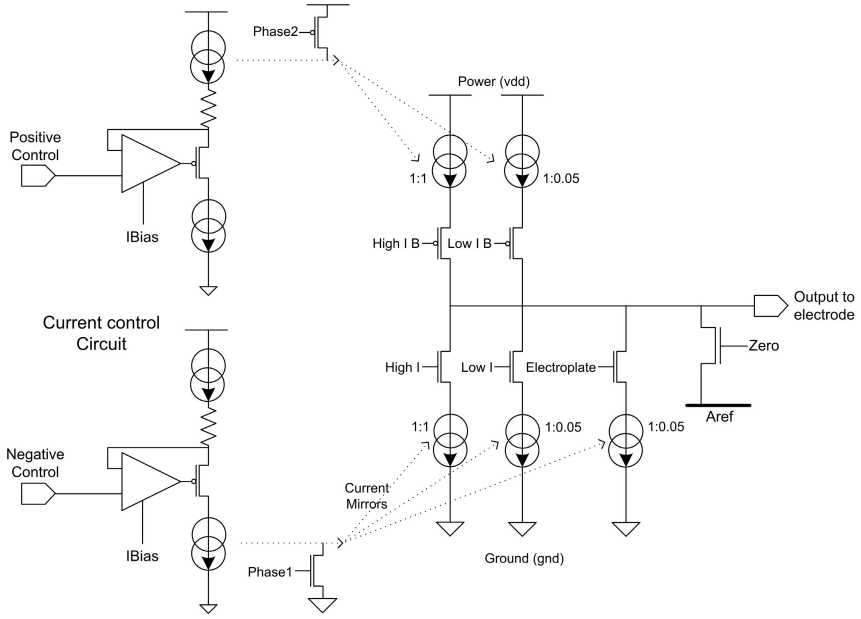

Fig 5. The biphasic output driver circuit that takes the control signals from the timer circuit to generate current pulses.

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Off chip control voltages feed into the current control circuit to set the base current from which the other mirrors work, either the high current mirror (HighI) or a step down mirror (1/20) for lower current (LowI). This current will be limited by the RC characteristics of the electrodes. This will have a greater effect if high currents are used, when the voltage developed across the resistance at the electrode-retina interface cannot exceed the supply voltage of 3.3 volts. An additional current sink is included to allow the chip to control electroplating during manufacture or repair to the microelectrode array. Table 1 gives the simulated range of output current settings for control voltage.

Table 1. Current output settings

Control Voltage	HighI output	LowI output
970 mV	30 µA	1.5 µA
2.52 V	1 µA	-
2.44V	-	100 nA

These particular values represent the range over which the control voltage is linear with respect to the output current. The control voltages can be extended beyond these points, but the relationship becomes rapidly non-linear. The output minimum is 28.37nA and the maximum 31.36µA, but fineness of control is lost beyond the values indicated in table 1.

3. RESULTS

3.1 Chip and Test Setup

Figure 12 shows a chip, wire bonded to the test system. A total of 568 bond pads are needed to connect all the power and control signals as well as 469 pixel outputs. To achieve this, 3 layers of bond pads were used on all sides of the chip. An aluminium fanout was produced to increase the bonding pitch enough to bond to a PCB.

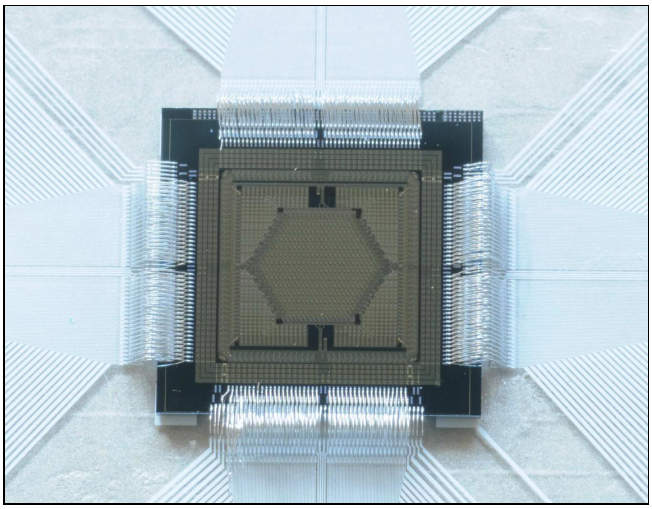

Figure 6. A close-up of the chip bonded to an aluminium fanout. The 3-level wire bonding can be seen, The pixel array and neural network are contained within the central hexagonal section of the chip. Surrounding this are the output controls and drivers. This chip is approx 7mm by 7mm.

Initial characterisation of the chip has been carried out independently of biological experiments using test outputs from various points along the signal chain.

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3.2 Output Frequency Ranges

The VCO was set to be controlled by the external test signal voltage. This was used to sweep the full range of the VCO, with the neural network suppressed having no weights selected. The frequency of the output pulses from one pixel was monitored while the test signal was varied from 1V to 3.3V. The response of the VCO is linear and covers the frequency ranges 1-50Hz and 5-100Hz as shown in figure 6.

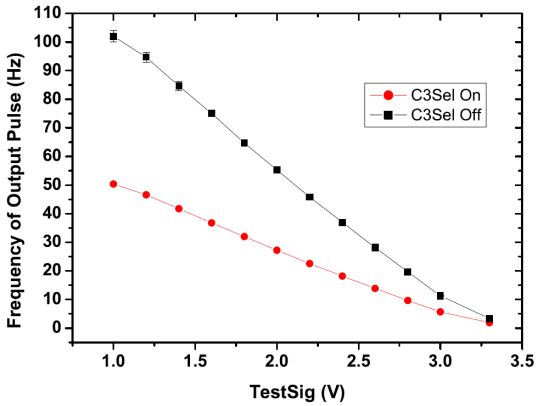

Fig 7. Plot of the frequency response of the output pulses as the control voltage (TestSig) to the VCO is varied. This shows the full range of the 100-1Hz required for retinal stimulation. The range selection options (C3sel) allows greater resolution at low frequencies.

3.3 Photodiode

To test the behaviour of the photodiode, the output pulse frequency of a pixel was monitored while the light intensity was attenuated using neural density filters. The results are shown in figure 7 for both frequency range options. Basic optics and light intensities similar to a well lit room were sufficient to produce a high frequency output, which dropped linearly as the light intensity was reduced. The solid lines are linear fits to the data points, with the values at the extremities excluded as the behaviour of the photodiode is non-linear in these regions.

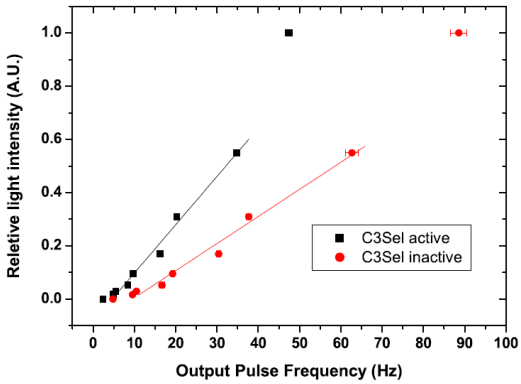

Fig 8. Variation of the frequency of the output pulses as the light intensity, incident on the sensor, is attenuated.

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3.4 Neural Network

Linearity of the neural network output was tested independently of the VCO using a test pixel from which the neural network sum is buffered out to an output pad for monitoring. Without any weights selected the neural network has the effect of buffering the input to the output. The linearity of this is important for proper functioning of the neural network. Figure 8 shows the output from the neural network as the test signal is used to sweep the input. It can be seen that that the linearity is extremely good over the desired operating range of 1 to 3 V.

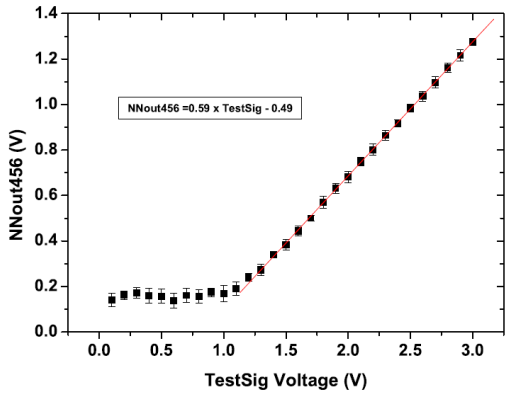

Fig 9. Linearity of the neural network summation as a function of the test signal voltage in place of the photodiode.

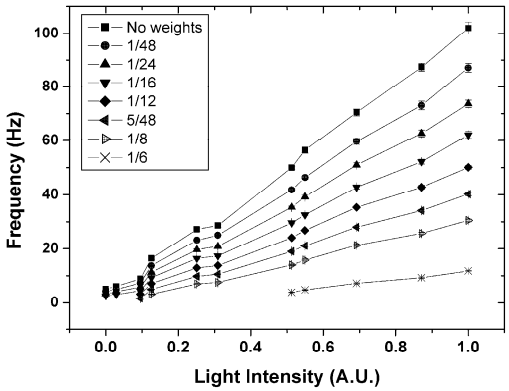

Fig 10. Output from the centre pixel in a cluster of nearest neighbours exposed to uniform light intensity. The light level is altered for various weight selections.

Testing of the various weight combinations was performed by programming a cluster of pixels to the same weight and varying the incident light intensity with neural density filters uniformly across the sensor. The centre pixel response is attenuated by a factor of the weight selected. Figure 9 shows the results from this test, the changes in gradient are proportional to the weight selected. It can be seen that with a 1/6 weight selected no all the signal is attenuated as would be expected given equation 1. This is thought to be due to some residual current in the neural network summing node. This could either be due to variation in the photodiode characteristics from pixel to pixel, or process miss match in the ratio of current mirrors in the neural network circuit. Further testing of the neural network is needed to fully characterise this circuit.

3.5 Biphasic Output Pulses and Current Modes

Figure 9 shows an example output pulse recorded from the chip. This shows the biphasic characteristics of a cathodic pulse followed by an inter-phasic delay of 100µs and then an anodic pulse. Figure 10 demonstrates the 'Zero' mode. In this mode we can see that by allowing the electrode output to be switched to the reference ground of the retinal sample (in this case a model made of discrete RC components) there is a decrease in the RC delay as current is reduced.

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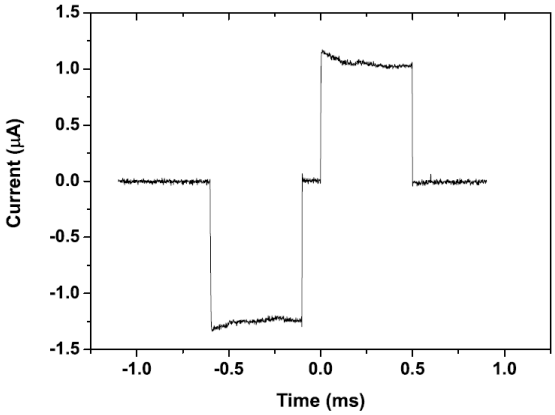

Fig 11. A biphasic current pulse produced by the chip. Each phase is 500µs in duration with and inter-phasic delay of 100µs. The pulse width can be altered by changing the clock frequency supplied to the chip.

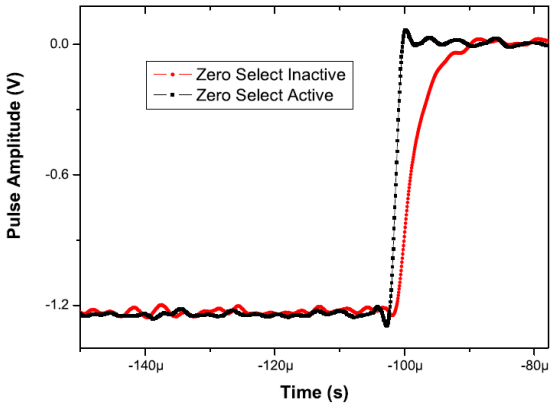

Fig 12. An example of the operation the 'zero' mode. The RC delay that results from the electrode/electrolyte interface can be negated by switching the chip outputs to the reference ground.

The amplitudes of the anodic and cathodic current pulses were measured as the current control voltages were varied across the useful range. Figure 11 show the current for high and low current modes.

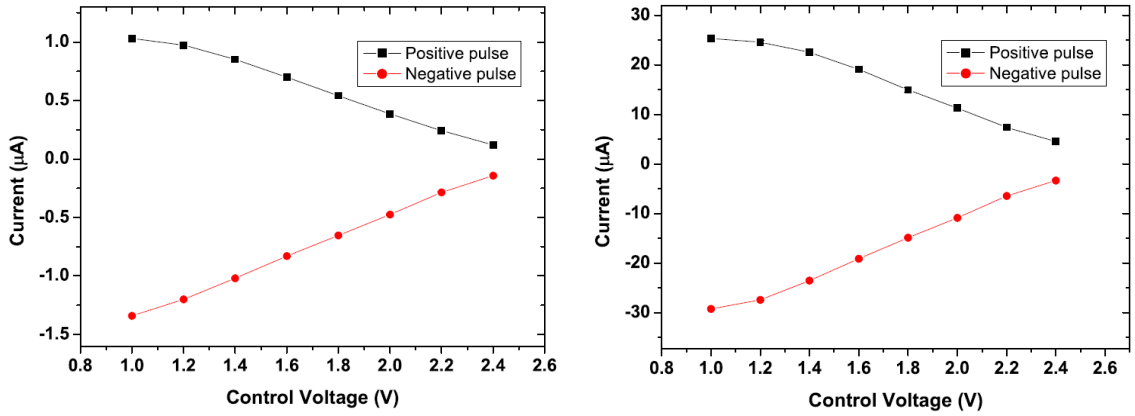

Fig 13. The variation of the current pulse amplitude with the externally supplied control voltage, operating in the low (left) and high (right) current modes. Asymmetry can be corrected for since positive and negative control voltages are independent.

From this characterisation it is possible to match anodic and cathodic pulses and achieve charged balanced biphasic pulses. The current range is from 30µA to 10µA for the cathodic pulses and 25µA to 10µA for the anodic pulses.

4. FUTURE DEVELOPMENTS

In the immediate future, chip testing is planned to continue and move towards preliminary biological tests. The first microelectrode arrays to be connected to the chip will utilise approximately 100 central pixels. Following on from this, larger arrays are being manufactured to make use of all 469 pixels.

With the next-generation ASIC we will look to include a more complex multilayer neural network to replicate other interactions across horizontal and radial cells in the retina. As new chip interconnect technologies become more widely

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available stacked chips are becoming a possibility for increasing the amount of signal processing in a given area. This could also open up options to connect electrodes more directly to the ASIC or even grow them from pads within the sensor array.

The integrating photodiode design used on this sensor does not have the large dynamic range of the eye. With the next chip logarithmic or other high dynamic range architectures will be explored. A logarithmic pixel would allow the sensor to cope with a wide variation of light intensity in the visual scene [10], in a similar way to the human eye.

It will also be important to meet other requirement of a realisable retinal prosthesis, such as wireless powering and power efficiency. Larger arrays of smaller pixels will also continue to be a requirement.

5. CONCLUSIONS

We have successfully designed an image sensor for experimentation with the function of the retina. It features a novel hexagonal array of 469 pixels interconnected by a neural network and includes biphasic outputs for all pixels. Test results to date show the chip operating to the original specifications. Further work is required to characterise the chip on a larger scale than single pixels, however this is much harder than a regular sensor given the form of the outputs. Results from the biphasic current circuits show the outputs meet the specifications which should allow successful activation of retinal ganglion cells in future experiments.

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