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## Statistical evaluation of 571 GaAs quantum point contact transistors showing the 0.7 anomaly in quantized conductance using cryogenic on-chip multiplexing

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The mass production and the practical number of cryogenic quantum devices producible in a single chip are limited to the number of electrical contact pads and wiring of the cryostat or dilution refrigerator. It is, therefore, beneficial to contrast the measurements of hundreds of devices fabricated in a single chip in one cooldown process to promote the scalability, integrability, reliability, and reproducibility of quantum devices and to save evaluation time, cost and energy. Here, we use a cryogenic on-chip multiplexer architecture and investigate the statistics of the 0.7 anomaly observed on the first three plateaus of the quantized conductance of semiconductor quantum point contact (QPC) transistors. Our single chips contain 256 split gate field effect QPC transistors (QFET) each, with two 16-branch multiplexed source-drain and gate pads, allowing individual transistors to be selected, addressed and controlled through an electrostatic gate voltage process. A total of 1280 quantum transistors with nano-scale dimensions are patterned in 5 different chips of GaAs heterostructures. From the measurements of 571 functioning QPCs taken at temperatures  $T= 1.4$  K and  $T= 40$  mK, it is found that the spontaneous polarisation model and Kondo effect do not fit our results. Furthermore, some of the features in our data largely agreed with van Hove model with short-range interactions. Our approach provides further insight into the quantum mechanical properties and microscopic origin of the 0.7 anomaly in QPCs, paving the way for the development of semiconducting quantum circuits and integrated cryogenic electronics, for scalable quantum logic control, readout, synthesis, and processing applications.

## Introduction

Semiconductor field effect mesoscopic devices, controlled and addressed by gate voltages, are fundamental in quantum science and technology applications. Quantum mechanics dominates their electronic properties and responses at cryogenic temperatures. The study of device characteristics often is based on the measurements of a single device, however even devices with an identical design and having the same fabrication process result in different physical characteristic properties. In this category, gate-defined semiconducting quantum point contact (QPC) transistors<sup>1</sup> or split-gate QPC field effect transistors (QFET) are necessary cryogenic quantum nano-electronic devices in spin and charge qubit-based quantum processors. Their differential conductance is quantized in units of  $G_Q=2e^2/h$ , where  $e$  is the electron charge, and  $h$  is Planck's constant<sup>2,3</sup>. However, there is an unanticipated shoulder at  $\sim 0.7 G_Q$ , referred to as the '0.7 anomaly'<sup>4,5</sup>, which is still not fully understood despite twenty years of research<sup>6,7</sup>. Various models have been proposed, including spontaneous spin polarisation<sup>4,8-10</sup>, Wigner crystallisation<sup>11,12</sup>, the Kondo effect<sup>13-16</sup>, and the smeared van Hove singularity<sup>17-20</sup>. Similarly, several experiments have been performed. For instance, Al-Taie *et al.* used an array of QPCs, with electron motion in the channels in the  $x$ -direction and the lateral confinement in the  $y$ -direction, and performed statistical quantum transport measurements at low temperatures<sup>21-23</sup>. They expressed the barrier and confinement curvatures in terms of the harmonic-oscillator energies,  $E_x = \hbar\omega_x$  and  $E_y = \hbar\omega_y$ , and studied the effect of disorders on quantum device performance. Moreover, Bauer *et al.* used the combination of a potential barrier and electron interactions to modify the van Hove singularity as a ridge-like structure in the local density of states (LDOS)<sup>17</sup>.

## Theory of QPC transistors

In this work, by studying a large array of on-chip integrated QPC devices we show that some of the features in our experimental results, taken at both  $T= 40$  mK and  $T= 1.4$  K, largely support the van Hove model with short-range interactions. The LDOS is a function of the dimensionless quantity  $\kappa=(\mu-V_c)/E_x=ae(V_G-V_G^{\text{riser}})/E_x$ , where  $\mu$  is the chemical potential,  $V_c$  is the central barrier height,  $a=dV_{SD}/dV_{SG}$  is the lever arm,  $V_G$  is the split gate voltage and  $V_G^{\text{riser}}$  is the split-gate voltage at the plateau riser. Electrons are slowed down where the LDOS is high and experience an enhanced effective interaction strength  $U_{\text{eff}}(\kappa)=U \cdot \text{LDOS}(\kappa)$ . Here,  $\kappa$  is proportional to  $V_G$  through  $\kappa=ae(V_G-V_G^{\text{riser}})/E_x$  and  $U$  is the interaction strength as defined in Eq. A1 of the Appendix. From the expression  $1-U_{\text{eff}}=dV_c^h/dV_c$ <sup>19</sup>, where  $V_c^h$  is the effective Hartree barrier height, as described in Eq. A2 in the Appendix, we can deduce

$$1-U \cdot \text{LDOS}(\kappa) = 1-U_{\text{eff}}(\kappa) \approx S_{TC}(\kappa) \quad (1)$$

Here, transconductance suppression  $S_{TC}$  is defined as the ratio between the measured transconductance ( $TC_{SD}=dG_{SD}/d\kappa$  and  $G_{SD}$  is the measured source-drain conductance) and non-interacting transconductance ( $TC^0=dG^0/d\kappa$  and  $G^0$  is the non-interacting

conductance). The non-interacting variables are marked with a superscript 0 throughout the paper.

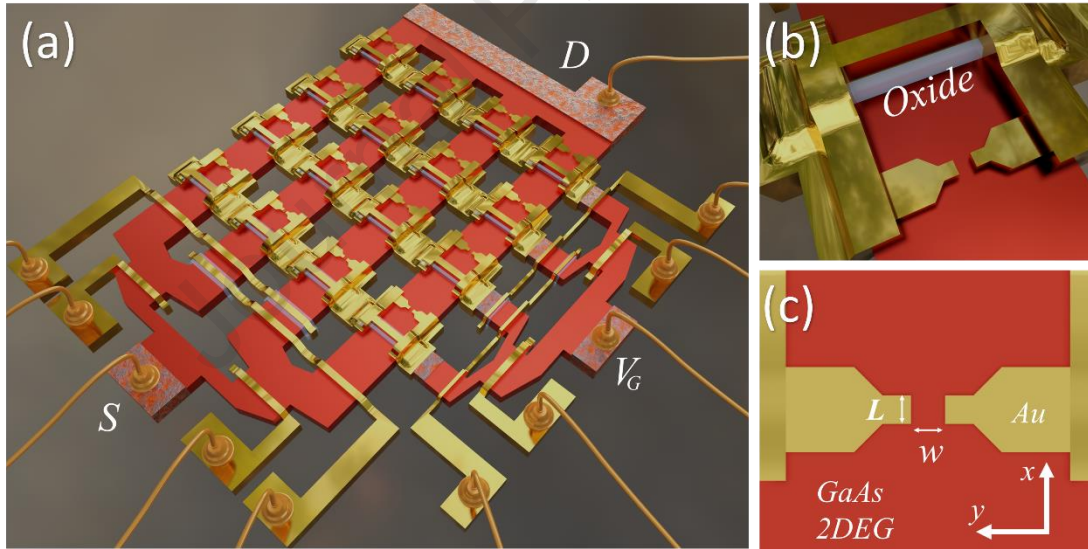
Equation (1) implies a direct link between  $S_{TC}$  and the  $LDOS$  ridge. The maximum of the  $LDOS$  ( $LDOS_{max}$ ) results in the strongest effective interaction strength ( $U_{eff}^{max}$ ), and thus the strongest transconductance suppression. We define the minimum of transconductance suppression as the ‘0.7 anomaly transconductance suppression  $S_{TC}^{0.7}$ ’. The position  $\kappa$  and conductance  $G$  at the minimum of transconductance suppression are defined as  $\kappa_{TC}^{0.7}$  and  $G_{TC}^{0.7}$ . Therefore,

$$1 - U \cdot LDOS_{max} = 1 - U_{eff}^{max} \approx S_{TC}^{0.7} \quad (2)$$

This equation shows the link between  $S_{TC}^{0.7}$  and  $U_{eff}^{max}$ . The  $LDOS_{max}$  and  $U$  scale with  $1/\sqrt{E_x}$ <sup>17</sup> and  $\sqrt{E_y}$ <sup>24</sup>, respectively. Substitution of these expressions into Eq. (2) gives

$$U_{eff}^{max} \propto \sqrt{E_y/E_x} \quad (3)$$

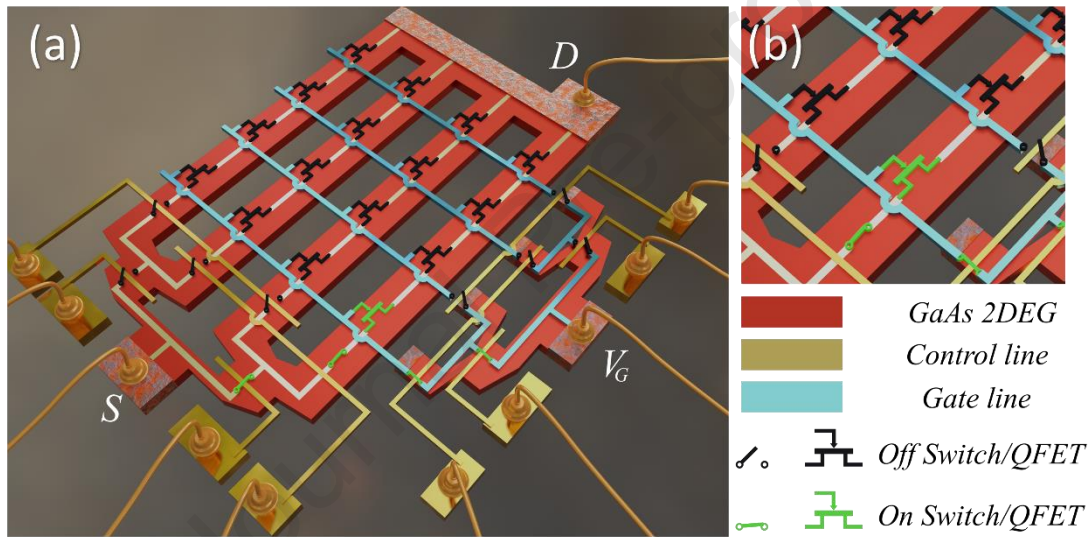
To explore the role of  $U_{eff}^{max}$ , it is necessary to investigate the statistics of  $E_x$  and  $E_y$  in a large array of devices and study the geometry effect on them (we define  $E_y/E_x = U_E$  to characterise  $U_{eff}^{max}$ ).



**Figure 1 3D schematic of the GaAs multiplexed quantum chip.** **a**, Overall structure of a 4-by-4 MUX design with Au gate represented by the bright metal yellow, and rough orange for Au/Ge/Ni Ohmic alloy. The smooth red connected to the ohmic metal is the channel formed by the MESA wet etch, and it is a 90nm thick GaAs 2DEG buried underneath. ‘S’, ‘ $V_G$ ’ and ‘D’ are labelled on the MESA represent source, drain and gate pads, respectively. The transparent blue under the gates is the metal gates insulating layer (oxide). Finally, the bright orange metal is the wire bonding connected to the pads. **b**, The enlarged view of a single addressable device in the 4-by-4 MUX array in split-gates representations. **c**, The plane top view of the split gates with the direction of  $E_x$  and  $E_y$  indicated.

### *Fabrication of large arrays of QPCs with on-chip multiplexing architecture*

With this aim, we developed a cryogenic multiplexer (MUX) architecture for large-scale nanofabrication and on-chip integration of QPC transistors. A total of 1280 quantum nanodevices on five different chips (labelled samples 1-5) are designed and manufactured. Each single chip contains 256 split-gate QPC transistors, with two 16-branch multiplexed source-drain and gate pads. Through this cryogenic multiplexed architecture, individual transistors are selected, addressed and controlled by using the electrostatic gating method. The wafer used for this experiment is a GaAs/AlGaAs heterostructure. First, optical lithography is performed followed by a 100nm deep MESA chemical wet etch with  $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O} = 1:8:1600$  for 150s. Secondly, the Ohmic contacts are defined with another optical lithography with an ‘undercut’ profile. The ohmic metal (AuGeNi alloy) is annealed at 430°C for 80s so that the metal diffuses into the 2DEG and makes contact with the MESA pattern from the previous step. An insulator is required for gates on the device.



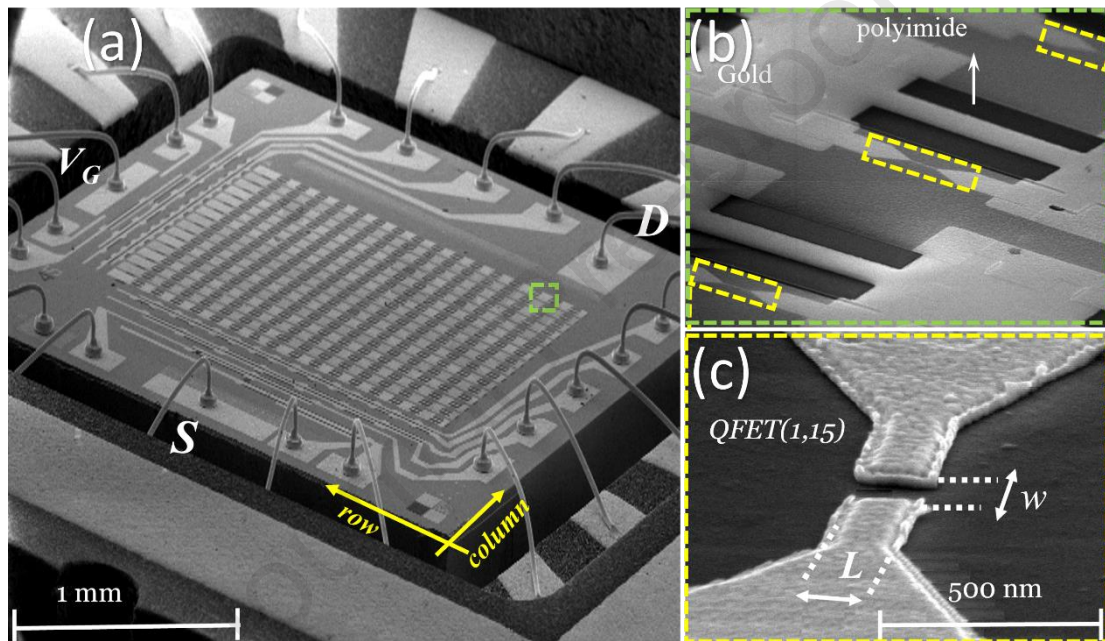
**Figure 2 Circuit representation of the GaAs field effect multiplexed quantum chip.** **a**, Circuit equivalent of a 4-by-4 MUX quantum field effect transistors with gate line represented by the bright blue, and control lines for both channel and gates are bright metal yellow. The white line represents the device conduction path. The off-state QFET and switch are black and the ones that are on are bright green. **b**, The enlarged view of the opened device with green switches switched on to activate that single QFET device.

A mixture of polyimide and T9039 with a 2:1 ratio is used as the insulator between the gates and the sample. After the insulating layer deposition, gates are defined with a similar process as the ohmic metal but with Ebeam-lithography as the QPC requires defining fine pattern. The final step is wire bonding and mounting the sample to the LCC chip carrier followed by loading in the cryostat or dilution fridges for cryogenic characterisation. A reduced-number MUX 3D model is shown in Fig. 1 along with the circuit representation in Fig. 2. Figure 1a explicitly shows the structure of a 4-by-4 MUX design with red 2DEG and bright gold gates on top. A single split-gate QFET is shown in the enlarged view of Figure 1b. Figure 2a is the circuit equivalent to the same MUX design shown in Fig. 1a. A zoomed view also shows how a single functioning



QFET is addressed by control lines which are represented by the bright green switches in Fig. 2b. Our MUX chips contain 256 QPCs of different widths  $W$  and lengths  $L$ , allowing the study of the roles of  $E_x$  and  $E_y$  (the shape of the saddle point potential) on the 0.7 anomaly. From low-temperature quantum transport measurements, we find that  $S_{TC}$  is strongest for the first plateau and stronger at the higher temperature of  $T=1.4$  K compared to  $T=40$  mK. A very strong  $S_{TC}$  can result in the spontaneous risers-splitting of transconductance (i.e. the appearance of two peaks on the transconductance curve between adjacent subbands).

Figure 3a shows a Scanning Electron Microscope (SEM) image of our semiconducting quantum multiplexed chip consisting of an array of 256 QPC transistors addressed by two MUXs. The selected area in Fig. 3a is enlarged in Fig. 3b, showing three QPCs in a row. Figure 3c shows a QPC with width  $W$  and length  $L$  labelled in the image.

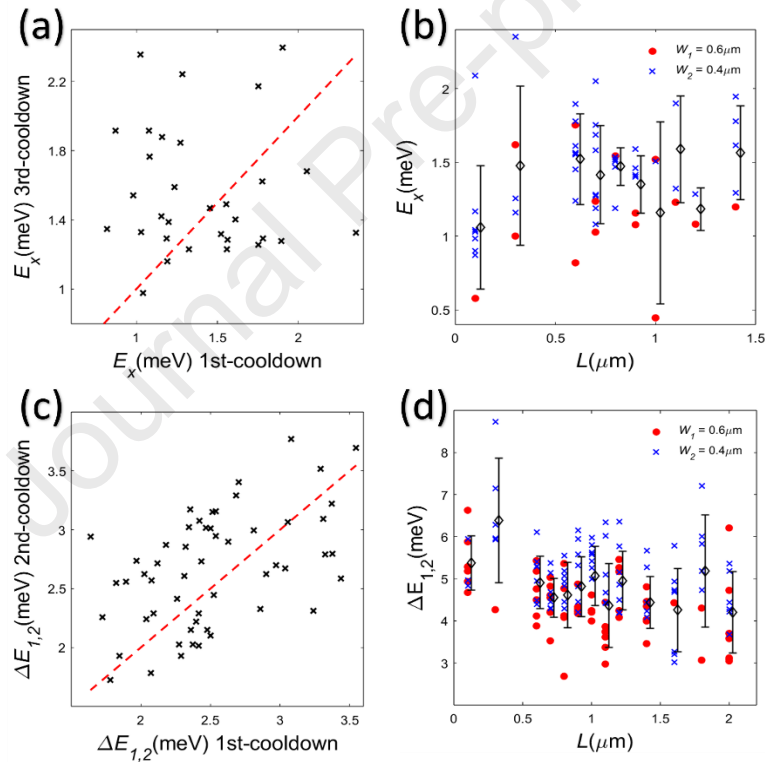


**Figure 3 SEM images of one GaAs quantum chip with a large array of multiplexed QFETs.** **a**, A quantum multiplexed (MUX) circuit consisting of 256 QPCs (QFETs) that are controlled and read out by only 19 electrical contacts. Each QPC is measured by addressing the row of source-drain multiplexer ( $S$  and  $D$  contacts are labelled in the figure) and the column of gates MUX ( $V_G$  contact is labelled in the figure), and is named in terms of the coordinate QFET (row, column). **b**, The enlarged area of the dashed-square defined in **a**, showing three split-gate quantum transistors in the first row  $QFET(1,14)$ ,  $QFET(1,15)$  and  $QFET(1,16)$  (marked with three dashed-rectangles). Polyimide is shown in black. **c**, The device  $QFET(1,15)$  with width  $W$  and length  $L$  labelled.

### *Cryogenic characterisation of on-chip multiplexed QPC transistors*

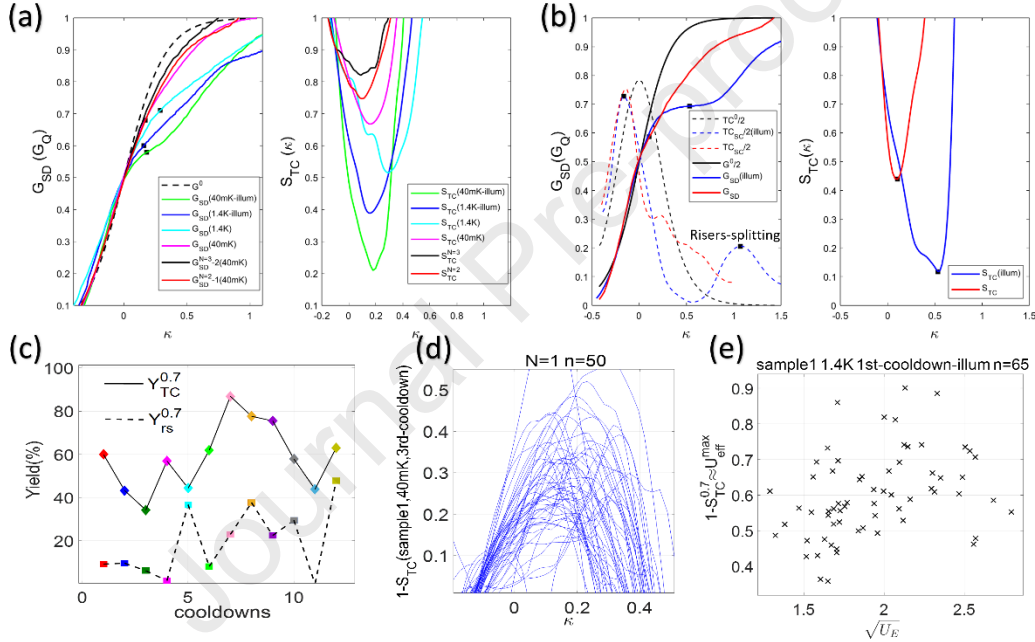
In total, 571 QPCs are successfully measured in chips 1-5 (out of a total of 1280 QPCs). First, only devices that show conductance suppression are investigated with a focus on the 0.7 anomaly. Second, only devices that have a good fitting of  $G^0$  with  $G_{SD}$

are investigated to ensure that the device has a parabolic potential barrier, as a precondition of the van Hove formulas. Here, a good fit is where  $G^0$  well coincides with  $G_{SD}$ . To extract  $E_x$ , we fit the lower half step of  $G^0$  with that of corrected  $G_{SD}$  based on the Landauer-Buttiker formula<sup>25</sup>. We extract  $E_x^N$  in these devices for the first three subbands ( $N$  is the subband index), in two forward (as the conductance decreases with gate voltage) and backward (as the conductance increases with gate voltage) sweep directions. Figure 4a shows a scatter plot of  $E_x$  values between the first ( $x$ -axis) and third ( $y$ -axis) cool-downs for  $n=33$  devices in sample 1 at  $T=40$  mK.  $E_x$  values are distinct for a different cooldown (from room temperature down to  $T=40$  mK), indicating that  $E_x$  is highly influenced by random fluctuations of the electrostatic potential from the different cooldowns. Figure 4b shows the geometry dependence of  $E_x$  for  $n=62$  devices in sample 1 at  $T=40$  mK.  $E_x$  values are nearly independent of the device length. In particular, the  $E_x$  values vary a lot for samples of the same length. The red dots (devices with width  $W_1=0.6$   $\mu\text{m}$ ) and blue crosses (devices with width  $W_2=0.4$   $\mu\text{m}$ ) are not distinct, showing  $E_x$  values are also independent of the device width. This suggests  $E_x$  is more influenced by the potential background than device geometry.



**Figure 4 Cryogenic evaluation of large array multiplexed QPCs.** **a**, Geometry dependence of the potential curvatures. Scatter plot of  $E_x$  between the first ( $x$ -axis) and third ( $y$ -axis) cooldowns for sample 1 at  $T=40$  mK.  $n$  counts the measured device number. The red dashed line (gradient=1) provides a guide to the eye. The results are in the forward sweep if not specified. **b**, Geometry dependence of  $E_x$  for sample 1 at  $T=40$  mK. The red dots and blue crosses represent devices with widths  $W_1=0.6$   $\mu\text{m}$  and  $W_2=0.4$   $\mu\text{m}$ , respectively. The error bar represents the mean  $\pm$  standard deviation for devices at each length, offset horizontally by  $0.025$   $\mu\text{m}$  for clarity. **c**, Scatter plot of  $\Delta E_{1,2}$  between the first ( $x$ -axis) and second ( $y$ -axis) cooldowns for sample 1 at  $T=40$  mK. **d**, Geometry dependence of  $\Delta E_{1,2}$  for sample 1 at  $T=1.4$  K after illumination.

The values of  $E_y$  are equal to the subband spacings  $\Delta E_{N,N+1}$  for a parabolic barrier and are extracted using DC bias spectroscopy. The drop of the applied DC bias voltage across the series resistance is corrected by using *Eq. A3* in the Appendix. Figure 4c is a scatter plot of  $\Delta E_{1,2}$  values between the first and second cooldowns for  $n=54$  devices in sample 1 at  $T=40$  mK, showing a repeatable correlation between the two measurements. The values of  $\Delta E_{1,2}$  are greatly amplified after illumination, presumably because illumination increases the carrier concentration so that a larger split-gate voltage is required to pinch off the device leading to a greater confining potential. Figure 4d shows the geometry dependence of  $\Delta E_{1,2}$  for  $n=143$  QFET nanodevices in sample 1 at  $T=1.4$  K. For length dependence, the means of  $\Delta E_{1,2}$  (marked with diamonds) show a weak negative correlation with length. For width dependence, the red dots tend to be below the blue crosses, indicating a larger width can result in smaller values of  $\Delta E_{1,2}$ . Thus,  $\Delta E_{1,2}$  is weakly correlated with both the length and width, which accords with the modelling by *Koop et al.*<sup>26</sup>.



**Figure 5 Transconductance suppression of the 0.7 anomaly in large array multiplexed QPCs.** **a**, Comparisons of  $S_{TC}(\kappa)$  (right) at  $T=40$  mK and 1.4 K before and after illumination, respectively, for device  $D$  (16,15), sample 1. **b**, Spontaneous risers-splitting for transconductance for device  $D$  (10,11), sample 1 at  $T=40$  mK. **c**, Comparisons of  $Y_{RS}^{0.7}$  (dashed line) with  $Y_{TC}^{0.7}$  (solid line) for samples 1-5 in 12 cooldowns.  $Y_{RS}^{0.7}$  ( $Y_{TC}^{0.7}$ ) is the yield of 1D devices showing risers-splitting (transconductance suppression). **d**, Curves of  $1-S_{TC}$  ( $\approx U \cdot LDOS$ ) as a function of  $\kappa$  for the first plateau, for sample 1 at  $T=40$  mK.  $n$  counts the device number. **e**, Correlation of  $1-S_{TC}^{0.7}$  with  $\sqrt{U_E}$  in  $n=65$  devices, in sample 1 at  $T=1.4$  K, after illumination.  $\rho(1-S_{TC}^{0.7}, \sqrt{U_E})=0.301$ .

Therefore, unlike  $E_x$ , which is difficult to adjust,  $E_y$  can be adjusted using the device geometry. A short and narrow QPC yields the strongest confinement. In this way, the control of  $U_{eff}^{max}$  can be realised. Figure 5a compares the  $S_{TC}$  of device  $D$  (16,15), sample



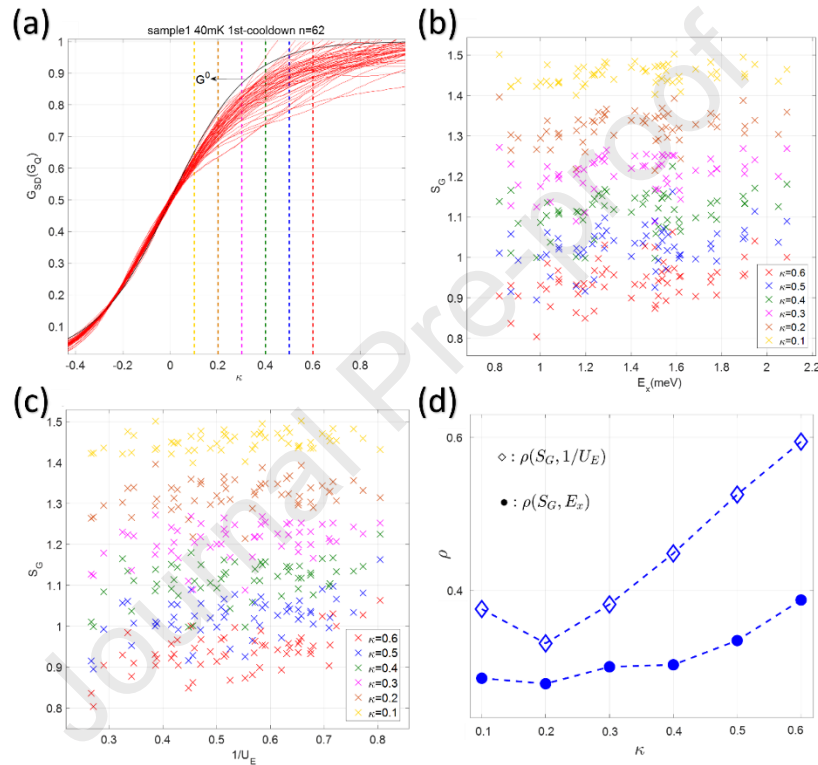
1 at  $T=1.4$  K, and  $T=40$  mK before and after illumination. The device has a width  $W=0.4$   $\mu\text{m}$  and a length  $L=0.1$   $\mu\text{m}$ .  $V_G$  axis is transformed into  $\kappa$  by  $\kappa=\alpha e(V_G-V_G^{\text{riser}})/E_x$ , where  $\alpha$  is the lever arm and  $V_G^{\text{riser}}$  is the split-gate voltage at the plateau riser with a conductance of  $0.5 G_Q$ . The  $\kappa_{\text{TC}}^{0.7}$  position is marked with black squares for each  $G_{\text{SD}}$  curve.  $S_{\text{TC}}$  is reduced (read the right axis) after illumination at both  $T=40$  mK and  $T=1.4$  K. For higher plateaus,  $G_{\text{SD}}^{N=2}$  (yellow curve) and  $G_{\text{SD}}^{N=3}$  (brown curve) are vertically offset by  $G_Q$  and  $2 G_Q$ , respectively, to the first plateau position.  $S_{\text{TC}}^{N=2}$  and  $S_{\text{TC}}^{N=3}$  are less reduced than  $S_{\text{TC}}$  for the first plateau.

The key points are as follows: (i),  $S_{\text{TC}}$  values are smaller at  $T=1.4$  K than those at  $T=40$  mK. This effect is consistent with the temperature dependence of the 0.7 anomaly as commonly reported<sup>4</sup> (i.e. the 0.7 anomaly becomes more pronounced as temperature increases<sup>1</sup>). (ii),  $S_{\text{TC}}$  values become smaller after illumination at both  $T=1.4$  K and  $T=40$  mK temperatures since illumination increases  $E_y$  but not  $E_x$ , resulting in larger values of  $U_{\text{eff}}^{\text{max}}$ . (iii), for higher plateaus,  $S_{\text{TC}}^{N=3} < S_{\text{TC}}^{N=2} < S_{\text{TC}}^{N=1}$ . This is because when the 1D subband index increases, the width increases, and the density in each sub-open regime increases<sup>17</sup> (i.e. at  $0.5-0.9 G_Q$ ), and  $U_{\text{eff}}^{\text{max}}$  drops to almost zero for the third plateau. Figure 5b illustrates the spontaneous riser-splitting of the transconductance for device  $D$  (10,11), sample 1 at  $T=40$  mK.  $TC_{\text{SD}}$  curve is the differential of smoothed  $G_{\text{SD}}$ . For  $TC^0$ ,  $TC_{\text{SD}}$  and  $S_{\text{TC}}=TC_{\text{SD}}/TC^0$  curves, read the right axis.  $S_{\text{TC}}^{0.7}$  is marked with triangles on  $S_{\text{TC}}$  curves before and after illumination. After illumination, due to a strong suppression of  $S_{\text{TC}}$  (circle-marked blue line), two split-risers (marked with dots) appear on  $TC_{\text{SD}}$  curve (star-marked green line).

After illumination,  $TC_{\text{SD}}$  is suppressed and  $S_{\text{TC}}^{0.7}$  decreased from a value of 0.44 before illumination to a value of 0.12, which gives rise to a local minimum and leads to the riser-splitting as indicated by the arrow in the  $TC_{\text{SD}}$  curve (star-marked green line). Thomas *et al.* regarded the riser-splitting as evidence for the spin-gap of spontaneously polarised spins<sup>5</sup>. However, after doing a statistical check on numerous devices, we find that the riser-splitting has a very low probability of occurrence, whereas the 0.7 anomaly suppression is observed much more often. Figure 5c compares the yield of 1D devices showing the riser-splitting  $Y_{\text{rs}}^{0.7}$  to the yield of devices showing transconductance suppression  $Y_{\text{TC}}^{0.7}$  in samples 1-5 in 12 different cooldowns. It is found that the number for  $Y_{\text{rs}}^{0.7}$  is much lower than the number for  $Y_{\text{TC}}^{0.7}$  at each cooldown. It is therefore inferred that the spontaneous polarisation model may not fit our results. A very large  $U_E=E_y/E_x$ , and the suppression of transconductance, but not spontaneous spin polarisation, cause the riser-splitting. Based on Eq. (1), we can use the expression  $1-S_{\text{TC}}(\kappa)\approx U\cdot\text{LDOS}(\kappa)$  to roughly characterise the effective  $\text{LDOS}(\kappa)$  shape. Figure 5d shows curves of  $1-S_{\text{TC}}$  for the first plateau, for sample 1 at  $T=40$  mK. The number of devices showing  $S_{\text{TC}}$  decreases with increasing  $N$ , showing a decreasing chance of the 0.7 anomaly for higher subbands. Furthermore, Fig. 5e shows that in sample 1 at  $T=1.4$  K, the Pearson correlation coefficient  $\rho$  of  $1-S_{\text{TC}}^{0.7}$  with  $\sqrt{U_E}$ , shown as  $\rho(1-S_{\text{TC}}^{0.7}, \sqrt{U_E})=0.301$ , indicating  $1-S_{\text{TC}}^{0.7}$  is positively correlated with  $\sqrt{U_E}$ . This obeys expression  $1-S_{\text{TC}}^{0.7}\propto\sqrt{U_E}$ , which is a combination of Eq. (2) and (3). Note that  $E_x$  also has an effect on  $S_{\text{TC}}^0$  in the non-interacting regime.

Next, we discuss the interaction effects on the whole curve of conductance suppression  $S_G=G_{\text{SD}}/G^0$  in our multiplexed quantum circuits. Figure 6a shows the first

step of conductance for  $n=62$  devices in sample 1 at  $T=40$  mK. The lower half step assembles together, and the 0.7 anomaly manifests different suppression levels compared with  $G^0$  in the sub-open regime. The  $E_x$  and  $1/U_E$  dependence of  $S_G$  at fixed  $\kappa$  positions (see vertical coloured lines) are shown in Fig. 6b and Fig. 6c, respectively. It can be seen that  $S_G$  is positively correlated with  $E_x$  and  $1/U_E$ . Figure 6d compares the Pearson correlation coefficient  $\rho$  of  $S_G$  with  $E_x$ , shown as  $\rho(S_G, E_x)$ , indicated with dots, and  $1/U_E$ , shown as  $\rho(S_G, 1/U_E)$ , indicated with diamonds, for different cooldowns. The diamond-marked lines are above the dot-marked lines, indicating  $\rho(S_G, 1/U_E) > \rho(S_G, E_x)$ , and  $S_G$  is more correlated with  $1/U_E = E_x/E_y$  than  $E_x$ . This underlines that the role of  $E_y$  on the 0.7 anomaly should be considered as being the same as that of  $E_x$ .



**Figure 6 Interaction effects on conductance suppression at fixed  $\kappa$  positions in large array multiplexed QPCs.** **a**, The first step of quantized conductance for  $n=62$  QPC devices in sample 1 at  $T=40$  mK. **b,c**, Dependence of  $S_G$  (offset upward in turn by 0.1 for clarity) on  $E_x$  (**b**) and  $1/U_E$  (**c**) at fixed  $\kappa$  positions (vertical coloured lines in **a**). **d**, Comparisons of  $\rho(S_G, 1/U_E)$  (marked with diamonds) with  $\rho(S_G, E_x)$  (marked with dots) as a function of  $\kappa$ .

### Summary

In short, we developed a cryogenic chip-integrated multiplexed quantum electronic circuit and demonstrated the statistical measurements of 571 split-gate quantum wires at sub-Kelvin temperature. From the measurements taken at temperatures  $T=1.4$  K and 40 mK, we found that our data largely agreed with van Hove model with short-range interactions. The 0.7 anomaly shows the strongest suppression of transconductance, which is governed by the ratio of the saddle point potential curvatures  $E_y/E_x$ . Moreover, we realised that the device geometry can be made to influence  $E_y$  but not  $E_x$ . The latter

is more sensitive to and is dominated by the potential background and is the same for short or long barriers of a given width of the channel, while the former is more geometry-dependent. We highlight that our method is a generic platform and can be applied to most kinds of material systems for further development of quantum devices and integrated circuits<sup>24-30</sup>. For instance, implementation of the presented integrated cryogenic on-chip multiplexing architecture to hybrid superconducting-semiconducting junctions may open up an avenue towards a better understanding of interfacial and geometrical effects in the behaviour of hybrid junctions, for topological superconducting network<sup>31-41</sup>. The proposed architecture can also be used for the control and readout of hybrid quantum electronic circuits for their potential applications in cryogenic nanoelectronics and fault-tolerant quantum processing.

### **Materials and methods**

Samples 1-5 are fabricated on a modulation-doped GaAs/AlGaAs heterostructure with two-dimensional electron gas (2DEG) formed 90 nm below the surface. The split gates are defined by electron-beam lithography. For sample 1, the carrier density and mobility are  $1.71 (3.39) \times 10^{11} \text{ cm}^{-2}$  and  $1.59 (3.82) \times 10^6 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$  before (after) illumination, respectively. For samples 2-5, the carrier density and mobility are  $2.08 (3.06) \times 10^{11} \text{ cm}^{-2}$  and  $3.06 (5.15) \times 10^6 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$  before (after) illumination, respectively. Samples 1, and 2 have the QFET device geometry with length  $L$  varying at fixed width  $W_1=0.6 \text{ }\mu\text{m}$  or  $W_2=0.4 \text{ }\mu\text{m}$ . Samples 3-5 have the device geometry with a fixed geometrical aspect ratio  $L/W$ . We perform two-terminal measurements using standard lock-in and AC excitation at 77 Hz. Samples 1-5 are measured at  $T=1.4 \text{ K}$  in a  $^4\text{He}$  cryostat. Sample 1 is measured at  $T=40 \text{ mK}$  in a dilution refrigerator in the absence or presence of magnetic fields. We use a red light-emitting diode (LED) for illumination purposes. The quantum transport measurements of the large arrays of chip-integrated multiplexed quantum devices were performed fully automated and performed by MATLAB.

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### Appendix

In Bauer's 1D tight-binding model, the interaction term in the Hamiltonian is given by Eq. (3.17) in Ref. 17, which we rewrite:

$$H_{\text{int}} = \sum_j U_j n_{j\uparrow} n_{j\downarrow} \quad (\text{A1})$$

Here,  $n_{j\uparrow(\downarrow)}$  counts for the number of electrons with spin  $\uparrow(\downarrow)$  at site  $j$ ; the on-site interaction strength  $U_j = U$  is assumed to be constant at sites in the central constriction region and drops to zero at outer sites.

Based on Eq. (3.26) (though treated only to first order) in Ref. 1, which we rewrite here,

$$1 - U_{\text{eff}} = \frac{dV_c^h}{dV_c} \quad (\text{A2})$$

$1 - U_{\text{eff}}$  is equal to the differential of the effective Hartree barrier height  $V_c^h$  with respect to the bare central barrier height  $V_c$ .

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To acquire a DC bias spectroscopy, the drop of applied DC bias voltage  $V_{DC}$  on series resistance  $R_s$  should be removed. The corrected source-drain DC bias voltage  $V_{SD}$  is

$$V_{SD} = V_{DC} - V_{DC} R_s \int_0^{V_{DC}} G_{SD} dV \quad (\text{A3})$$

where,  $G_{\text{DC}} = \int_0^{V_{\text{DC}}} G_{\text{SD}} dV$  is the DC conductance. We assume that the DC series resistance is equal to the AC series resistance, which is acquired by aligning the first plateau of  $G_{\text{SD}}$  to  $G_{\text{Q}}$ .

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**Declaration of interests**

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests:

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