Insights into the Ultra-Steep Subthreshold Slope Gate-all-around Feedback-FET for memory and sensing applications

Naveen Kumar, Ankit Dixit, Ali Rezaei, Tapas Dutta, César Pascual García and Vihar Georgiev, *Senior Member, IEEE*

Abstract— **Ultra-steep subthreshold slope FBFETs are promising candidates for next-generation memory and sensing devices. The characteristic of Subthreshold slope less than 10mV/dec enables efficient memory cell design and reduces power consumption during OFF-states, making FBFETs ideal for memory and sensing applications. In this paper, we demonstrate the use of FBFETs for both memory and sensing applications. For sensing, we have used Gouy-Chapman-Stern and site-binding model to calculate the surface potential on the sensing surface of the proposed device due to the protonation and deprotonations based on the pH of the electrolyte. For memory, we will target the memory window due to trapped charges or a single polyoxometalate cluster. We will show that the FBFETs can achieve a larger memory window and a sensing sensitivity crossing the Nernst limit. These results will demonstrate the potential of FBFETs for a wide range of applications.**

I. Introduction

In the ever-evolving realm of semiconductor technology, researchers and engineers constantly attempt to increase the performance of electronic devices. One crucial facet of this effort is achieving a low subthreshold slope (SS) [1-5], which is a critical criterion for analyzing the energy efficiency of transistors. Lower subthreshold slope devices offer reduced power consumption [6], faster switching rates [7-8], and improved battery life, making them vital for several applications in modern electronics.

The subthreshold slope is a measure of how efficiently a transistor turns on and off when migrating from the off-state to the on-state and vice versa. Traditional MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) have a theoretical minimum subthreshold slope of roughly 60 mV/decade at ambient temperature, which is a fundamental constraint for energy-efficient electronic systems. Low SS devices strive to exceed this constraint by leveraging novel materials, device architectures, and production approaches. By reaching a lower SS value, these devices can run at lower supply voltages, consume less power, and demonstrate improved performance. A few of the optimization techniques for Low SS Devices are (i) Advanced Gate Dielectrics [9]: One approach involves employing high-k dielectrics as gate insulators instead of the standard silicon dioxide. High-k materials offer improved gate control, minimizing leakage currents and subsequently lowering the subthreshold slope. (ii) Gate-all-around or Nanowire Transistors [10]: Employing nanowires as the channel material offers greater electrostatic control, leading to improved on-off performance and lower SS. (iii) Tunnel FETs (TFETs) [11]: TFETs exploit quantum tunneling phenomena to provide very efficient electron transport across the channel. This novel technique leads to subthreshold slopes below the theoretical limit of standard transistors. (iv) Doping Engineering [12]: Careful modification of the doping profile within the transistor's channel can enhance the device's ON-OFF characteristics and contribute to lowering the subthreshold slope.

The Potential Applications of Low SS Devices are (a) Energy-Efficient Processors: Low SS devices are crucial for generating power-efficient central processing units [13-14] (CPUs) and graphics processing units (GPUs) used in smartphones, laptops, and data centers. Improved energy efficiency in these gadgets directly correlates to extended battery life and reduced electricity consumption. (b) Internet of Things (IoT) Devices [15]: IoT devices frequently depend on battery power and are meant to be energy efficient. By adopting low SS transistors, these devices can improve their battery life greatly, ensuring longer operation without frequent recharging. (c) Wearable Electronics [16]: Wearable electronics, such as smartwatches and fitness trackers, demand ultra-low power consumption for seamless day-to-day operation. Low SS devices enable wearables to execute numerous functions without sacrificing battery life. (d) Biomedical Implants [17]: Medical implants demand reliable and long-lasting power sources. Low SS devices can lead to the creation of highly efficient bioelectronic implants that can function for extended periods without regular replacements. (e) Internet of Everything (IoE) Infrastructure [18]: The IoE connects numerous smart devices, including sensors and actuators, in a network. Low SS devices enable these networked systems to run efficiently while decreasing energy usage.

In this article, we investigate the notion of one of the low subthreshold slope devices (FBFET) followed by an exploration of its potential application in biosensing. Feedback FETs (FBFETs) [19] have a subthreshold slope of less than 10mV/dec, which makes them suitable for various digital or analog applications. FBFET behaves as a FET with negligible problems of tunneling across a junction or impact ionization which are widely used for steep-subthreshold devices [20-21]. Single amino acid sensing is important because amino acids are the building blocks of proteins, which are essential for life. By being able to sense single amino acids, we can gain insights into how proteins function and how they are involved in disease. Thus, we will use FBFETs for sensing a single

*Naveen Kumar, Ankit Dixit, Ali Rezaei, Tapas Dutta, and Vihar Georgiev are with the Device Modelling Group, Electronics and Nanoscale Engineering, James Watt School of Engineering, University of Glasgow (corresponding author e-mail: naveen.kumar@glasgow.ac.uk).

César Pascual García is with Nano-Enabled Medicine and Cosmetics Group, Materials Research and Technology Department, Luxembourg Institute of Science and Technology (LIST), Belvaux, Luxembourg.

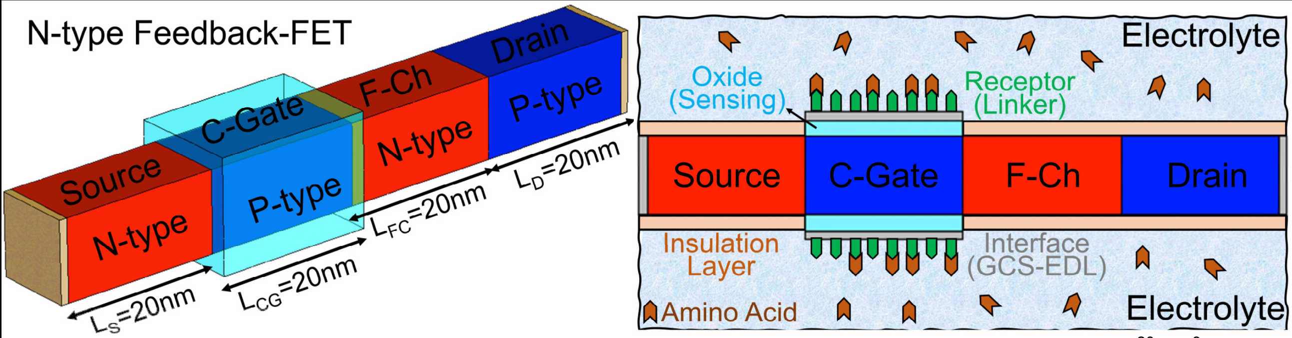

Figure 1. (a) 3-Dimensional structure of N-type Feedback Field-Effect Transistor with N-type source ($10^{20}cm^{-3}$), P-type control gate ($10^{20}cm^{-3}$), N-type feedback channel ($10^{20}cm^{-3}$) and P-type drain ($10^{20}cm^{-3}$). [Note: The dimensions of the various regions are as mentioned in the structure of 10nm×10nm square gate-all-around nanowire] (b) 2-Dimensional structure of the N-type Feedback FET (top view) enveloped with electrolyte in its surround with the exposed gate oxide regions (acting as sensing layer) with the linker or receptor molecules to capture the amino acids present in its vicinity.

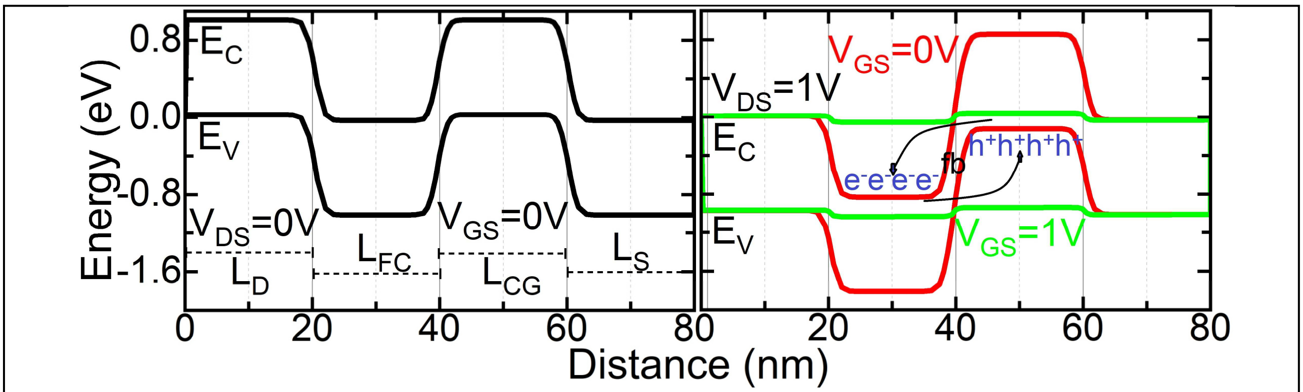

Figure 2. (a) Energy band diagram of the N-type Feedback Field-Effect Transistor in equilibrium state (applied drain bias and gate bias is zero) showing specific regions (b) Energy band diagram of the N-type Feedback FET in OFF-state (Red) (V_{DS}=1V & V_{GS}=0V) and ON-state (Green) (V_{DS}=1V & V_{GS}=1V) showing the feedback mechanism of transport of charge carriers between the control gate and feedback channel.

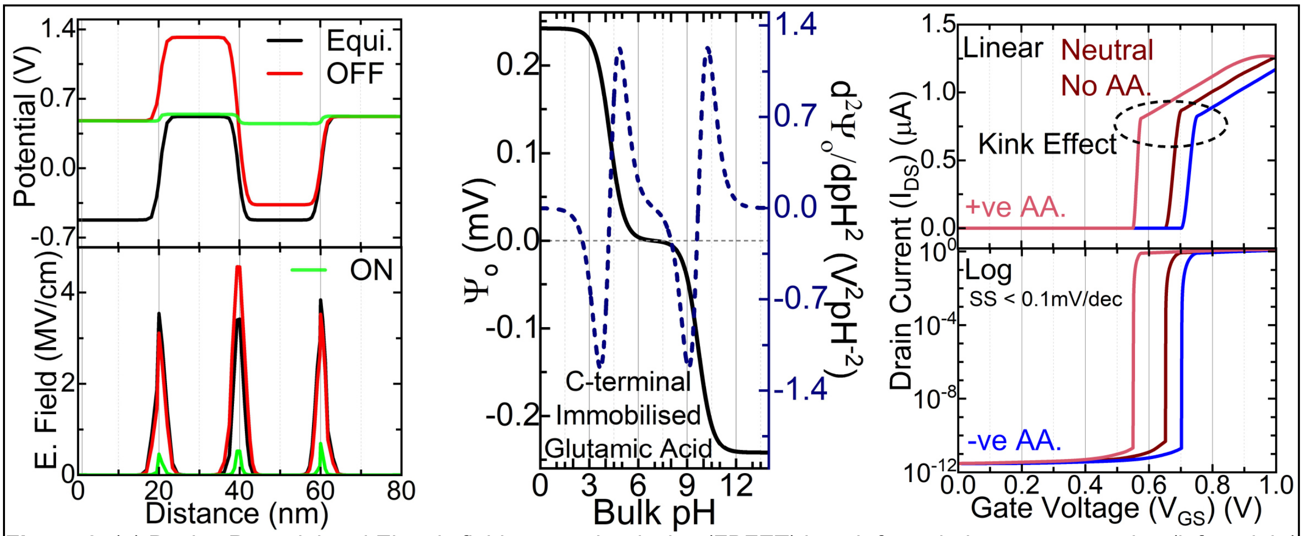

Figure 3. (a) Device Potential and Electric field across the device (FBFET) length from drain to source region (left to right) in equilibrium state (Black), OFF-state (Red) and ON-state (Green) (b) Surface Potential and Normalised 2nd Gradient of Surface Potential [$10^{-4}\times(d^2\Psi_o/dpH^2)/(\max(d^2\Psi_o/dpH^2))$] on the FBFET oxide surface with respect to the pH for Carboxy-terminal immobilized Glutamic Acid [Note: Calculated for electrolyte concentration=0.001M] (c) Drain current with respect to gate voltage in log and linear scale for the maximum density of charged (positive and negative) amino acid [density=$10^{12}cm^{-2}$].

amino acid and capture the effect of interface trap charges in terms of sensing applications.

II. Methodology and Results

The methodology is divided into two sections, device simulation and analytical model for amino acid fingerprints generation. We have developed a novel Biomolecule-

Oxide simulator to capture the interactions between amino acids and sensing surface (oxide) in the presence of an electrolyte [22-24]. Surface potential is calculated due to the generated charge density because of the protonation and deprotonation of amino acid along with the variation in pH of the electrolyte. FBFET was simulated with a PNPN doping profile consisting of a control gate and feedback channel other than source/drain regions. The calculated charge density was used on the oxide surface to mimic the presence of amino acid (Carboxyl-terminal immobilized Glutamic Acid) at the extreme pH values. Fig. 1(a) shows the 3D diagram of the 10nm×10nm square gate-all-around FBFET with the defined regions and dimensions. A 2D structure of the FBFET was shown in Fig. 1(b) as a top view of the 3D device including the electrolyte around the structure containing the amino acids with the receptor or linker molecules on the sensing surface (oxide). Based on possible experimental scenarios, the considered density of the receptor molecules is 10^{12} cm^{-2}. The behaviour of the simulated FBFET is clarified by the change in band energy for various operating conditions as shown in Fig. 2. The shifted drain energy by approx. 1eV and the reduction of band energy below the control gate confirm the effect of applied drain and gate bias respectively. The potential showed similar behaviour as of energy bandgap, and the electric field signified the abrupt junctions in equilibrium and OFF-state with a significant reduction in ON-state due to the drift of charge carriers along with the feedback mechanism while keeping the value less than the breakdown field for silicon. Fig. 3(b) and (c) show the shift of the drain current for positive and negatively charged amino acids. A detailed analysis of single molecule detection along with the memory window will be presented to show the exemplary advantages.

III. CONCLUSION

This research work presents a comprehensive methodology for generating amino acid fingerprints using both device simulation and analytical models. We have developed a novel Biomolecule-Oxide simulator that effectively captures the interactions between amino acids and the sensing surface (oxide) in the presence of an electrolyte. The FBFET (Field-Effect Transistor) device is simulated with a PNPN doping profile, incorporating a control gate and feedback channel along with source/drain regions. Furthermore, the research examines the effect of positive and negatively charged amino acids on the drain current, showcasing potential applications in single molecule detection. The study demonstrates the advantages of using this approach for amino acid detection, particularly highlighting the memory window for accurate identification. The proposed methodology and simulation results pave the way for further advancements in the field of biosensing and offer potential applications in areas such as medical diagnostics, environmental monitoring, and biotechnology.

ACKNOWLEDGMENT

This project has received funding from the European Union's Horizon 2020 research and innovation program under grant agreement no 862539-Electromed-FET OPEN.

REFERENCES

[1] Zhang, Q., Zhao, W. and Seabaugh, A., 2006. Low-subthreshold-swing tunnel transistors. IEEE Electron Device Letters, 27(4), pp.297-300.

[2] Lee, C.W., Nazarov, A.N., Ferain, I., Akhavan, N.D., Yan, R., Razavi, P., Yu, R., Doria, R.T. and Colinge, J.P., 2010. Low subthreshold slope in junctionless multigate transistors. Applied Physics Letters, 96(10).

[3] Gopalakrishnan, K., Griffin, P.B. and Plummer, J.D., 2002, December. I-MOS: A novel semiconductor device with a subthreshold slope lower than kT/q. In Digest. International Electron Devices Meeting, (pp. 289-292). IEEE.

[4] Paul, B.C., Raychowdhury, A. and Roy, K., 2005. Device optimization for digital subthreshold logic operation. IEEE Transactions on Electron Devices, 52(2), pp.237-247.

[5] Bol, D., Ambroise, R., Flandre, D. and Legat, J.D., 2009. Interests and limitations of technology scaling for subthreshold logic. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 17(10), pp.1508-1519.

[6] Kao, J., Narendra, S. and Chandrakasan, A., 2002, November. Subthreshold leakage modeling and reduction techniques. In Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design (pp. 141-148).

[7] Aziz, J., Kim, H., Hussain, T., Lee, H., Choi, T., Rehman, S., Khan, M.F., Kadam, K.D., Patil, H., Mehdi, S.M.Z. and Lee, M.J., 2022. Power efficient transistors with low subthreshold swing using abrupt switching devices. Nano Energy, 95, p.107060.

[8] Cristoloveanu, S., Wan, J. and Zaslavsky, A., 2016. A review of sharp-switching devices for ultra-low power applications. IEEE Journal of the Electron Devices Society, 4(5), pp.215-226.

[9] Salvatore, G.A., Bouvet, D. and Ionescu, A.M., 2008, December. Demonstration of subthrehold swing smaller than 60mV/decade in Fe-FET with P (VDF-TrFE)/SiO 2 gate stack. In 2008 IEEE International electron devices meeting (pp. 1-4). IEEE.

[10] Gandhi, R., Chen, Z., Singh, N., Banerjee, K. and Lee, S., 2011. Vertical Si-Nanowire $ n $-Type Tunneling FETs With Low Subthreshold Swing ($\leq\hbox {50}\\hbox {mV/decade} $) at Room Temperature. IEEE Electron Device Letters, 32(4), pp.437-439.

[11] Sharma, A., Goud, A.A. and Roy, K., 2014. GaSb-InAs n-TFET with doped source underlap exhibiting low subthreshold swing at sub-10-nm gate-lengths. IEEE Electron Device Letters, 35(12), pp.1221-1223.

[12] Jhaveri, R., Nagavarapu, V. and Woo, J.C., 2010. Effect of pocket doping and annealing schemes on the source-pocket tunnel field-effect transistor. IEEE Transactions on Electron Devices, 58(1), pp.80-86.

[13] Wang, A. and Chandrakasan, A., 2004, February. A 180mV FFT processor using subthreshold circuit techniques. In 2004 IEEE International Solid-State Circuits Conference (IEEE Cat. No. 04CH37519) (pp. 292-529). IEEE.

[14] Zhai, B., Pant, S., Nazhandali, L., Hanson, S., Olson, J., Reeves, A., Minuth, M., Helfand, R., Austin, T., Sylvester, D. and Blaauw, D., 2009. Energy-efficient subthreshold processor design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 17(8), pp.1127-1137.

[15] Lee, I., Sylvester, D. and Blaauw, D., 2017. A subthreshold voltage reference with scalable output voltage for low-power IoT systems. IEEE Journal of Solid-State Circuits, 52(5), pp.1443-1449.

[16] Baek, S., Bae, G.Y., Kwon, J., Cho, K. and Jung, S., 2019. Flexible pressure-sensitive contact transistors operating in the subthreshold regime. ACS applied materials & interfaces, 11(34), pp.31111-31118.

[17] Yang, J. and Skafidas, E., 2012. A low power MICS band phase-locked loop for high resolution retinal prosthesis. IEEE transactions on biomedical circuits and systems, 7(4), pp.513-525.

[18] Hsueh, F.K., Chen, W.H., Li, K.S., Shen, C.H., Shieh, J.M., Lee, C.Y., Chen, B.Y., Chen, H.C., Yang, C.C., Huang, W.H. and Chen, K.M., 2018, December. Ultra-low power 3D NC-FinFET-based monolithic 3D+-IC with computing-in-memory for intelligent IoT devices. In 2018 IEEE International Electron Devices Meeting (IEDM) (pp. 15-1). IEEE.

[19] Yeung, C. W., A. Padilla, T.-J. K. Liu, and C. Hu. "Programming characteristics of the steep turn-on/off feedback FET (FBFET)." In 2009 Symposium on VLSI Technology, pp. 176-177.

[20] Tura, A., and J. CS Woo. "Performance comparison of silicon steep subthreshold FETs." IEEE Transactions on Electron Devices 57, no. 6 (2010): 1362-1368.

[21] Cho, J., D. Lim, S. Woo, K. Cho, and S. Kim. "Static random access memory characteristics of single-gated feedback field-effect transistors." IEEE Transactions on Electron Devices 66, no. 1 (2018): 413-419.

[22] Kumar N, Dhar RPS, García CP, Georgiev V. "Discovery of Amino Acid fingerprints transducing their amphoteric signatures by field-effect transistors". ChemRxiv 2022. Not peer-reviewed.

[23] Kumar, N., Dhar, R., Garcia, C.P. and Georgiev, V.P., 2023. A Novel Computational Framework for Simulations of Bio-Field Effect Transistors. ECS Transactions, 111(1), p.249.

[24] Dhar, R., Kumar, N., Garcia, C.P. and Georgiev, V., 2023. Deriving a novel methodology for nano-BioFETs and analysing the effect of high-k oxides on the amino-acids sensing application. Solid-State Electronics, 200, p.108525.