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Background carrier concentration in intrinsic Ge-rich SiGe/Ge heterostructures integrated on Si(001)

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1. Introduction

Ge-rich silicon-germanium (SiGe) heterostructures are promising candidates for novel devices in the field of optoelectronic and photonic applications [1]. The possibility to manufacture those using CMOS-compatible materials and processes is an outstanding advantage.

As an example, the n-type Ge/SiGe material system has been proposed as a potential candidate for the realization of THz quantum cascade laser sources working at room temperature [2]. Here, the realization of the several mm-thick active layers, made of hundreds of quantum wells and barriers, are mandatory but extremely challenging to deposit since the strain balancing conditions have to be carefully achieved. Beside the effect of lattice strain on the band alignment of the complex quantum cascade structures, the plastic relaxation via the insertion of extended defects occurring in the growth process plays a major role in the charge profile existing in the device, which, in turn, strongly impacts the correct operation of devices. In fact, the existence of extended defects generates an electrical charge background that can combine with the intentional doping in the device design inducing a compensation or increase of the active carrier concentration. Therefore, the actual background carrier concentration needs to be known in order to counteract this problem during fabrication and to correctly describe the device electrical properties in the simulations.

In this work, we comprehensively studied the active carrier concentration in as-grown intrinsic $Si_{0.06}Ge_{0.94}$/Ge/Si heterostructures grown by reduced-pressure chemical vapour deposition (CVD) in a 200 mm CMOS pilot line. We conveniently use these Ge-rich SiGe virtual substrates because they are a promising foundation for the integration of n-Ge/SiGe superlattices on Si [3].

2. Results and Discussion

In order to identify the residual carrier concentration in the investigated heterostructure three complementary characterization techniques are applied: by Hall effect measurements we investigate the transport dynamics due to the defect-originated doping, while by capacitance-voltage (C-V) profiling and deep level transient spectroscopy (DLTS) the fixed charge distribution and the capture/release dynamics are investigated, respectively.

The investigated $Si_{0.06}Ge_{0.94}$/Ge heterostructures aligned for the different characterization techniques are schematically shown in Fig. 1. Measurements on both devices reveal a p-type conductivity of the intrinsic $Si_{0.04}Ge_{0.96}$ material in the operating temperature range of many optoelectronic devices.

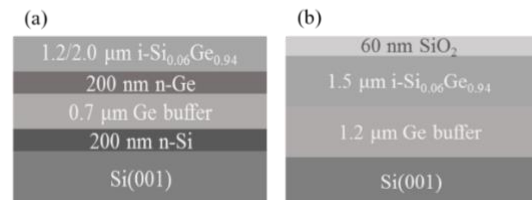

Fig. 1. The designed $Si_{0.06}Ge_{0.94}$/Ge/Si heterostructure used for (a) Hall effect and (b) C-V and DLTS measurements.

Figure 2 (a) demonstrates the temperature dependent sheet carrier density estimated by Hall effect measurements of the two investigated samples with different layer thicknesses. According to the differential Hall approach, a sheet carrier density of 3-4×10^{11} cm^{-2} is estimated in the temperature range between 100 K and 250 K corresponding to a constant hole density of 4×10^{15} cm^{-3} in the as-grown intrinsic $Si_{0.06}Ge_{0.94}$ layer (Fig. 2(b)).

Based on pulsed C-V characteristics of the fabricated MOS capacitors the carrier density profiles at temperatures below 200 K are calculated from the slope of a $1/C^2$-V plot and are shown in Fig. 3 (a). Again, a constant majority carrier density of approximately 5×10^{15} cm^{-3} of the nominal intrinsic $Si_{0.04}Ge_{0.96}$ layer is extracted as indicated in Fig. 3 (b). The existence of a free hole concentration including

ionized acceptors and compensating donors in the nominally intrinsic $Si_{0.04}Ge_{0.96}$ layer might be related to deep acceptor-like defect states inside the semiconductor bandgap [4].

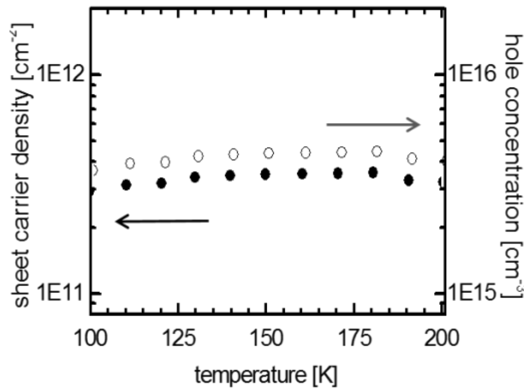

Fig. 2. The temperature dependent sheet carrier density and corresponding hole concentration of the $Si_{0.06}Ge_{0.94}$ layer as measured by the Hall effect.

Based on pulsed C-V characteristics of the fabricated MOS capacitors, the carrier density profiles at temperatures below 200 K are calculated from the slope of a $1/C^2$-V plot and are shown in Fig. 3 (a). Again, a constant majority carrier density of approximately $5x10^{15}$ cm^{-3} of the nominal intrinsic $Si_{0.04}Ge_{0.96}$ layer is extracted as indicated in Fig. 3 (b). The existence of a free hole concentration including ionized acceptors and compensating donors in the nominally intrinsic $Si_{0.04}Ge_{0.96}$ layer might be related to deep acceptor-like defect states inside the semiconductor bandgap [4].

In addition, the source of the included defect states is examined by DLTS. One dominant hole trap is found in the DLTS spectra at 225 K associated with a thermal activation energy of the bulk trap E_T of 0.325 eV above the valence band E_V estimated by an Arrhenius plot. The mid-gap position of the observed defect level implies an attractive trapping center for free carriers and/or effective generation-recombination center. This will impact the active carrier concentration in the final devices build by similar Ge-rich SiGe/Ge heterostructres and should be taken into consideration during fabrication and simulation.

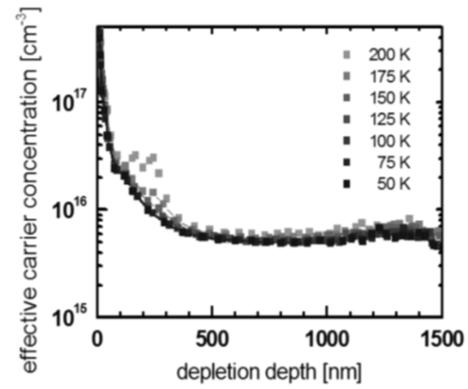

Fig. 3. Temperature dependent effective carrier concentration in dependence of depletion depth of the studied $Si_{0.06}Ge_{0.94}$ layer.

3. Conclusions

A background hole concentration in the mid 10^{15} cm^{-3} range is found in $Si_{0.06}Ge_{0.94}$/Ge/Si heterostructures. A hole trap at mid-gap position might be the reason for the residual p-type conductivity caused by acceptor-like bulk defects.

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