Recent Development of THz InP HEMTs at the University of Glasgow

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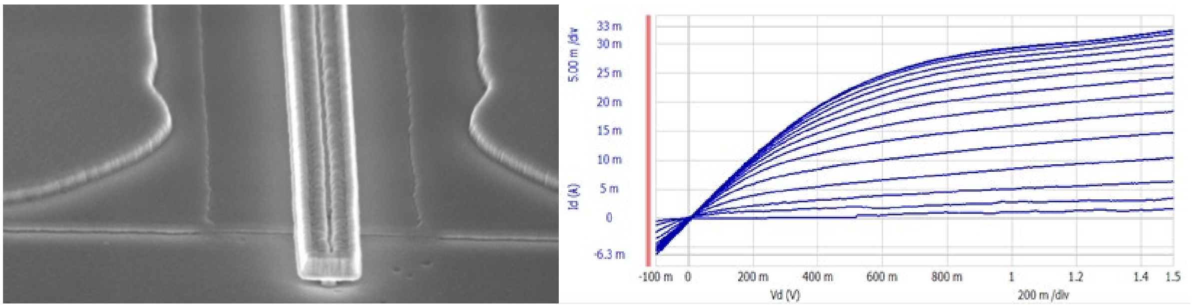
Abstract:

Transistors serve as the fundamental building blocks of modern electronics, encompassing a wide spectrum of applications, from digital and analogue to power, RF (Radio Frequency), and microwave circuits. Among these, High Electron Mobility Transistors (HEMTs) are best known for their superior performance in high-frequency capabilities, reaching hundreds of gigahertz, and low noise, closest to the quantum limit among other transistors.

The University of Glasgow has been pioneering in developing various transistor technologies, including MESFETs, MOSFETs, and HEMTs, utilising diverse materials such as InP, GaAs, GaN, and even diamond. In the past, the University achieved the distinction of demonstrating the fastest transistor e.g. f_T =440 GHz at that time [1]. However, due to a lack of demand in the market, progress in this field stalled temporarily. Recent advancements have reignited interest in these technologies, driven by the growing need for wider bandwidth in wireless communication, higher resolutions in RADAR systems, and the demand for low-power, low-noise amplifiers in quantum computing systems. Examples include 60 GHz indoor wireless local area networks, 77 GHz automotive radar systems, and passive imaging for improved visibility in foggy conditions and enhanced security. Furthermore, the range from 110 GHz to 170 GHz is being explored for 6G mobile networks, with the advantage of minimal atmospheric absorption in the W-band (75 GHz - 110 GHz), while the G-band (140 GHz - 220 GHz) opens doors to environmental and atmospheric monitoring from space. At even higher frequencies, such as the submillimetre range, data communication circuits can achieve impressive speeds of up to 260 Gbit/s.

In this abstract, we will showcase our recent developments in InP-based HEMTs that exhibit gain at frequencies exceeding 200 GHz. We will introduce a novel T-gate process designed to enhance reliability and achieve ultrafast performance. T-shaped Schottky gates, a common choice, strike a balance between current capacity, gate length reduction, and parasitic capacitance. However, fabricating gate lengths shorter than 50 nm presents significant challenges. Our controlled approach maintains a 50 nm gate length to improve device yield and overall performance simultaneously. Figure 1 below displays a scanning electron microscope (SEM) image of a fabricated InP HEMT with a 50 nm T-gate. In addition, we will demonstrate a physics-based model developed for optimising epitaxial layers. HEMTs are extremely sensitive to the thickness and doping profile of the epilayers, necessitating precise model calibration. We will demonstrate how delicate control over these elements, combined with material growth, fabrication processes, and electrical and RF performance tuning, plays a pivotal role in achieving superior device performance.

Finally, we will present experimental results on the electrical properties of the grown materials and Ohmic contacts as well as DC and RF measurements of the fabricated HEMTs.



(a) (b)

Figure 1. (a) SEM image of an InP HEMT with 50 nm T-gate. (b) IV characteristics of an HEMT. The device width is 15 µm.

[1] K. Elgaid, et al., "Low noise high performance 50 nm T-gate metamorphic HEMT with cut-off frequency f_T of 440 GHz for millimeterwave imaging receivers applications," International Conference on Indium Phosphide and Related Materials, 2005, Glasgow, UK, 2005, pp. 141-143, doi: 10.1109/ICIPRM.2005.1517439.