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Article

In-Plane III–V Nanowires on Si(1 1 0) with Quantum Wells by Selective Epitaxy in Templates

Enrico Brugnolotto,* Heinz Schmid, Vihar Georgiev, and Marilyne Sousa*

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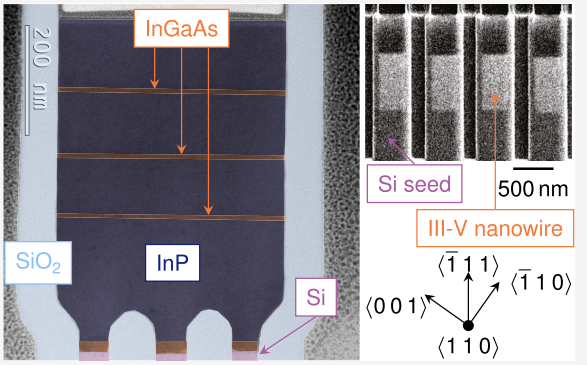
ABSTRACT: Heterointerfaces and quantum wells were realized in III–V nanowires monolithically grown from a silicon seed inside a silicon oxide template on a silicon-on-insulator wafer. InP, InGaAs, InAs, and GaAs were grown by metal-organic chemical vapor deposition. The yield of nanowires with a well-defined single-facet $\{1\ 1\ 1\}_B$ growth front was assessed using scanning electron microscopy, reaching 92.55%. Scanning transmission electron microscopy and energy-dispersive X-ray spectroscopy analysis revealed good composition control and the formation of sharp single-faceted quantum wells throughout the sample. The robustness of the process was further demonstrated by a forced merger of individual nanowires into one large crystal. In this sample, the quantum wells were as well defined as those in the single-seed nanowires. At the same time, we did not observe the formation of any dislocations at the merge location.



INTRODUCTION

Devices based on III–V heterostructures are well established in electronics, finding major applications in optical data communication and radio frequency (RF) amplifiers. The miniaturization of optically active III–V elements and their integration on silicon has increased in the last couple of decades, leading to the development of photonics as an alternative to traditional metal interconnects for short-range data transfer.[1−3]

In industry, integration of III–V semiconductors on Si is accomplished by the transfer of III–V material grown on lattice-matched substrates onto a supporting Si wafer.[4,5] This method allows manufacturers to avoid lattice mismatch as a source of defects entirely but implies increased production complexity and a limited integration density.[6−9] On the other hand, monolithic integration can offer high integration densities in very competitive time frames,[7] provided the issue of lattice-mismatch-borne defects[10−12] is addressed.

Selective area growth (SAG)[13,14] and aspect ratio trapping (ART)[15,16] explore different mechanisms that allow for the relaxation of the strained lattice and reduce the propagation of defects in the III–V material. A promising natural evolution of ART-SAG techniques[17,18] involves the growth of III–Vs in confined templates, such as in template-assisted selective epitaxy (TASE).[19] TASE enables the monolithic integration of III–V-based active photonic components such as photodetectors[20,21] and lasers[22,23] on Si through a versatile[24] CMOS-compatible process.

Typically, III–V growth on Si $\{0\ 0\ 1\}$ shows a multifaceted growth front, which can lead to compositional and thickness variations[25,26] due to differences in growth rates of different crystalline planes. Multifaceted growth can be suppressed by growing on Si (1 1 0) along a ⟨1 1 1⟩ direction,[27,28] and single-facet heterointerface formation was also described in homoepitaxy on InP (1 1 0) along a ⟨1 1 0⟩ direction, resulting in well-defined quantum well sections.[29,30]

Here, we systematically investigate growth uniformity, yield, and superlattice thickness control in an optimized single-facet growth regime on Si (1 1 0). We will first explain the growth process and characterization methods and subsequently report on the growth yield and the crystalline and compositional properties of the grown structures.

EXPERIMENTAL SECTION

The samples were fabricated from a (1 1 0)-oriented silicon-on-insulator (SOI) wafer consisting of a 70-nm-thick Si device layer on a 150-nm-thick buried SiO_2 layer. The device design is oriented on the Si (1 1 0) surface with an orthogonal ⟨1 1 1⟩ direction aligned along the nanowire growth direction. Additionally, we employ designs with template orientation tilted 20° away from the ⟨1 1 1⟩ direction.

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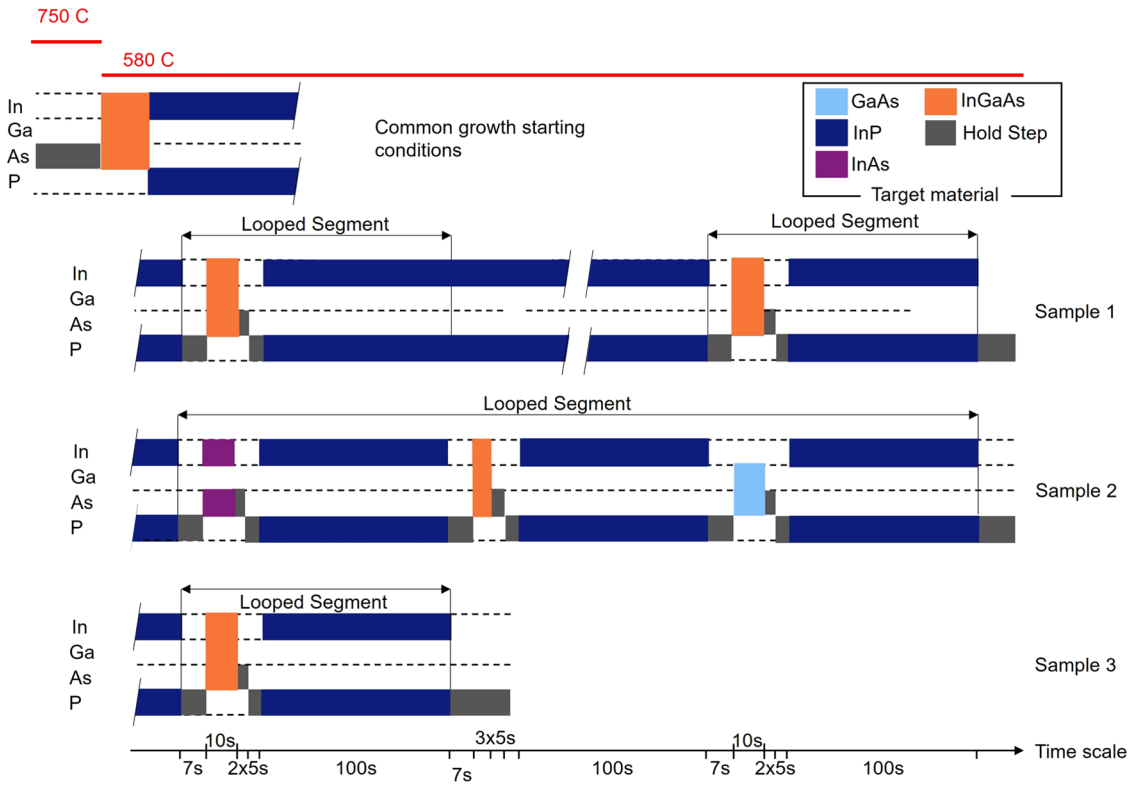

Figure 1. Schematic representation of the three growth recipes with target material color coded according to the legend at the top right. Colored blocks denote flow of the precursor of the element specified on the left-hand side of the respective line. The first line shows the temperatures at which the various steps of the recipe take place, while the second line shows the common growth steps for all three samples. To enhance readability, the deposition times of thick layers are not scaled with those of the Quantum Well segments. In particular, the long InP deposition steps in the looped segments are 100 s long. The Quantum Well and hold step are in scale with each other, with the post InP hold step being 7 s in P atmosphere and the post arsenide hold steps being 5 s in As atmosphere followed by 5 s in P atmosphere. The quantum well deposition steps are all 10 s long except for the InGaAs segment in sample 2 which is 5 s long.

The nanowire designs in samples 1 and 2 have four cross-sectional areas: 70 × 70 nm, 140 × 70 nm, 210 × 70 nm, and 280 × 70 nm. The thickness of the SOI device layer fixed the structure height at 70 nm. Structures containing three nucleation sites in sample 3 have a design cross-sectional area of 400 × 70 nm in the widest section.

The shapes of the nanowires and Si seeds are defined in the device layer in successive steps of e-beam lithography (EBL) and reactive ion etching (RIE). Template oxide deposition is achieved by atomic layer deposition (ALD) and plasma-enhanced chemical vapor deposition (PECVD). The template oxide is then opened at the end of the nanowires with successive steps of EBL and RIE.[19]

Etch-back of the Si layer in the template is performed using tetramethylammonium hydroxide (TMAH), resulting in a smooth {1 1 1} Si seed facet[31] perpendicular to the wafer surface. Immediately before growth, a 5-s-long dip in buffered hydrofluoric acid (HF) is performed to remove the native oxide on the Si seed surface.

Growth. Growth is carried out in a metal−organic chemical vapor deposition (MOCVD) reactor at 60 Torr equipped with a showerhead over a rotating susceptor. The latter can accommodate up to three 2-in. wafers. Each growth run was performed on 2 cm × 2 cm chips patterned as described in the previous section.

An initial baking step at 750 °C is followed by growth at 580 °C. The metal−organic precursors used in the growth are trimethyl indium, trimethyl gallium, *tert*-butylphosphine, and *tert*-butyl arsine.

Figure 1 schematically illustrates the recipes employed during the growth of the two studied samples. The first three growth steps are common to all samples: a baking native oxide desorption step takes place in an As-rich atmosphere, followed by a short InGaAs nucleation step and a further InP growth step designed to stabilize a single $\{1\ 1\ 1\}_B$ facet as the growth front.[28] V/III ratios and In/(In+Ga) fractions for every material are reported in Table 1. An InP-lattice-matched composition ($In_{0.53}Ga_{0.47}As$) was targeted for the InGaAs segments. As the growth takes place on a {1 1 1} facet, the In/(In+Ga) molar fraction has to be tuned to take into account the facet-dependent incorporation rates. For $In_{0.53}Ga_{0.47}As$, the In/(In+Ga) was thus set to a ratio of 0.16.[25]

After the initial steps, each growth recipe and growth time differ. One or more loop steps are added to create the quantum well superlattices. To improve heterointerface definition, a purge or hold step is included after each of the layers.[28]

A long InP segment separates the two looped segments in the recipe for sample 1 to highlight any changes in growth rates given by the proximity to the template opening. The superlattice of sample 2 incorporates InAs, InGaAs, and GaAs quantum wells. The InGaAs layers lattice-matched to InP had a reduced deposition time of 5 s, while the strained layers were grown during a 10-s-long deposition step. As shown in Table 1, the V/III ratio for InAs differs significantly from those of InGaAs and GaAs because the individual precursor flows were kept constant to avoid concentration fluctuations during the various deposition steps.

Characterization. Sample surveys were conducted with the scanning electron microscope (SEM) available in a dual-beam FEI

Table 1. V/III Ratios Used in the MOCVD Growth of the Nanowires

material	V/III ratio
InP	234
InAs	186
InGaAs	29
GaAs	34.4

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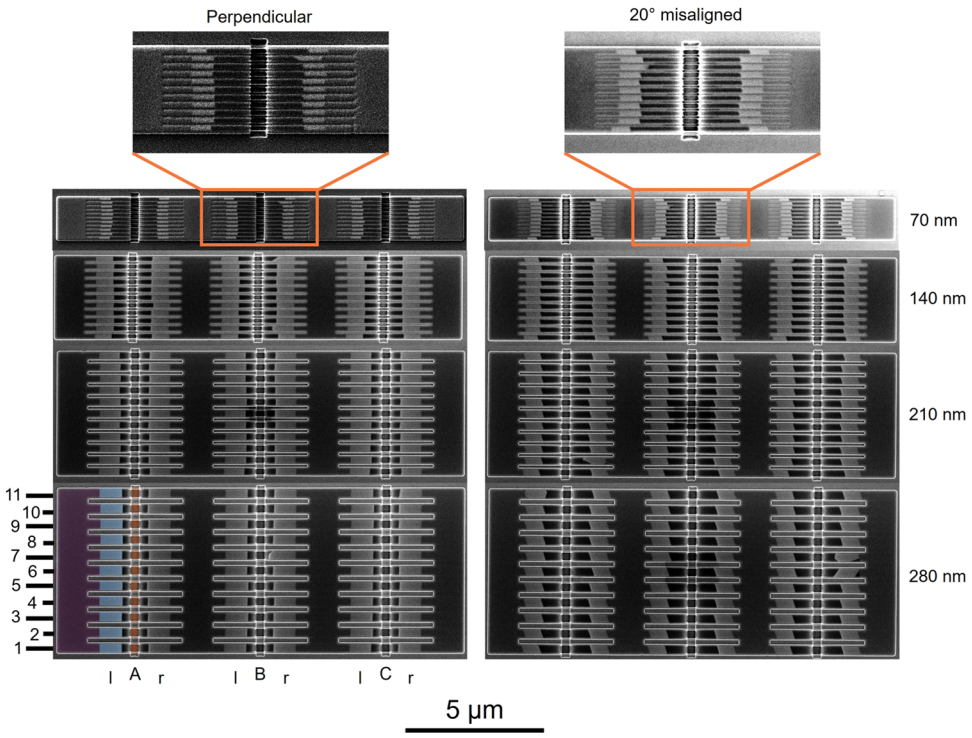

Figure 2. Top-view SEM images of arrays with grown III−V nanowires. The 70, 140, 210, and 280 nm wide wires are shown from top to bottom. The arrays on the left contain structures grown from a seed surface perpendicular to the template orientation, while the ones on the right are grown from seed surfaces forming 20° angles with the template walls. On the bottom left of the images, the three main elements of the arrays are highlighted in purple (silicon seed), light blue (III−V nanowires), and orange (template opening).

Helios NanoLab 450S focused ion beam (FIB) tool. The same tool was employed to create the electron transparent lamellae studied by using a double-corrected JEOL ARM-200F scanning transmission electron microscope (STEM). The microscope has a beam energy of (200 ± 0.3) keV. Energy-dispersive X-ray spectroscopy (EDS) measurements for compositional analysis were carried out with a JED-2300T detector mounted in the microscope's column.

RESULTS AND DISCUSSION

Figure 2 shows growth results from sample 1 of arrays containing template nanotubes of four different widths (70, 140, 210, and 280 nm). Each array contains 66 nanowires (in light blue) grown from silicon (in purple) and arranged in 33 pairs. Each pair of wires shares the same template opening (in orange).

Each wire in the array can be identified by its row, opening, and position relative to the latter. Each row is numbered from 1 to 11, starting at the bottom of the array. The template openings are marked by letters A-C; the wires connected to the opening to the left (l) or right (r) can be easily distinguished. Therefore, a string such as 9Br identifies a single wire in the array.

Our growth methodology aims to select and maintain a single $\{1\ 1\ 1\}_B$ facet as the nanowire's growth front. If a III−V wire end surface is multifaceted or is not parallel to the Si seed facet, the wire is classified as defective in this study without requiring a further in-depth STEM analysis. This first distinction allows evaluation of the fraction of "perfect" wires, defining a growth yield.

In Figure 2, the 280 nm 20° misaligned arrays present some defective wires in 11Al, 6Cr, and 7Cr; however, the other wires in each pair (11Ar, 6Cl, and 7Cl) appear "perfect". As is evident in the case of wire 6Cr, the wire grew into an unpredictable shape after nucleation, which did not cover the entirety of the seed surface. It is unclear if the source of defective wires can be attributed solely to the nucleation step, as there are other sites (70 nm misaligned B9l, 70 nm perpendicular B10r, 140 nm perpendicular 2Br, 11Br, and 280 nm perpendicular 7Br) that present a defective wire and fully covered seed. However, this finding suggests that nucleation plays an important role in the selection of the growth facet.

Another parameter that negatively affects the growth yield is the loss of growth selectivity and the resulting parasitic growth. This is ascribed to impurities or surface features promoting nucleation. An example of this is shown in Figure 3a, where a single defect of this kind affects many wires. Figure 3b also

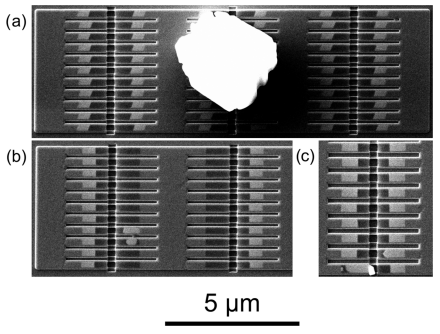

Figure 3. Examples of failure situations for TASE-grown wires: (a) large parasitic crystal obstructing many growth sites; (b) multiple seeds do not show nucleation of III−V material at all, while one site shows parasitic nucleation inside the template; (c) in the bottom row, after initial nucleation on the Si, a parasitic crystal developed inside the template and grew out of it.

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Table 2. Distribution of Failure Types for Samples 1 and 2[a]

	defect categories and occurrence						
	wrong facet	hidden by parasitic	oxide nucleated	seed exposed	long	short	no growth
sample 1	164	230	2	0	5	204	61
parallel	81	170	1	0	4	0	0
% of category	49.4%	77.9%	50%		80%	0%	0%
20° misaligned	83	51	1	0	1	204	61
% of category	50.6%	22.1%	50%		20%	100%	100%
sample 2	204	257	15	8	3	7	20
parallel	127	145	6	4	1	5	20
% of category	62.3%	56.4%	40%	50%	33.3%	71.4%	100%
20° misaligned	77	112	9	4	2	2	0
% of category	37.7%	43.6%	60%	50%	66.7%	28.6%	0%
total	**368**	**487**	**17**	**8**	**8**	**211**	**81**

[a]Each sample's total is broken down between wires grown parallel to or 20° misaligned away from the ⟨1 1 1⟩ direction. Percentages for these two sub-categories and an overall total are given.

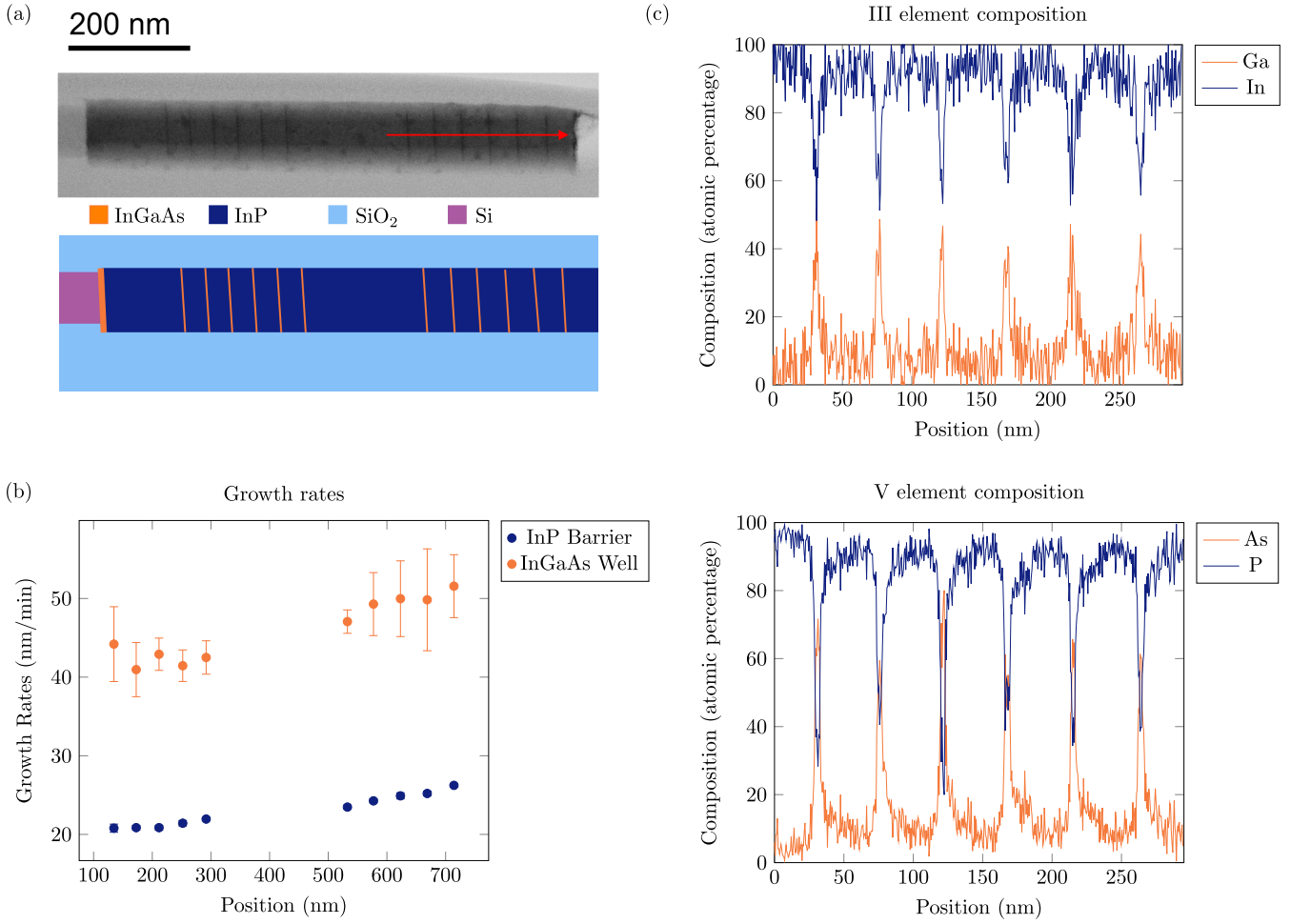

Figure 4. Characterization results for sample 1. (a) BF-STEM image of the cross section of one of the nanowires and corresponding schematic composition drawing. (b) Growth rates of InGaAs, in orange, and InP, in dark blue. Error bars on all x coordinates for both materials and on y coordinates for InP are smaller than the graphical markers. (c) Composition profiles calculated from an EDS line scan recorded on the location and with the direction marked by the red arrow in (a).

shows sites where parasitic nucleation occurred within templates and seed sites that did not undergo III−V nucleation, likely because of the lingering of a passivating SiO_2 layer on the Si seed surface. This happened despite the proximity to other correctly grown wires. Finally, the bottom row of Figure 3c illustrates an example where after the initial

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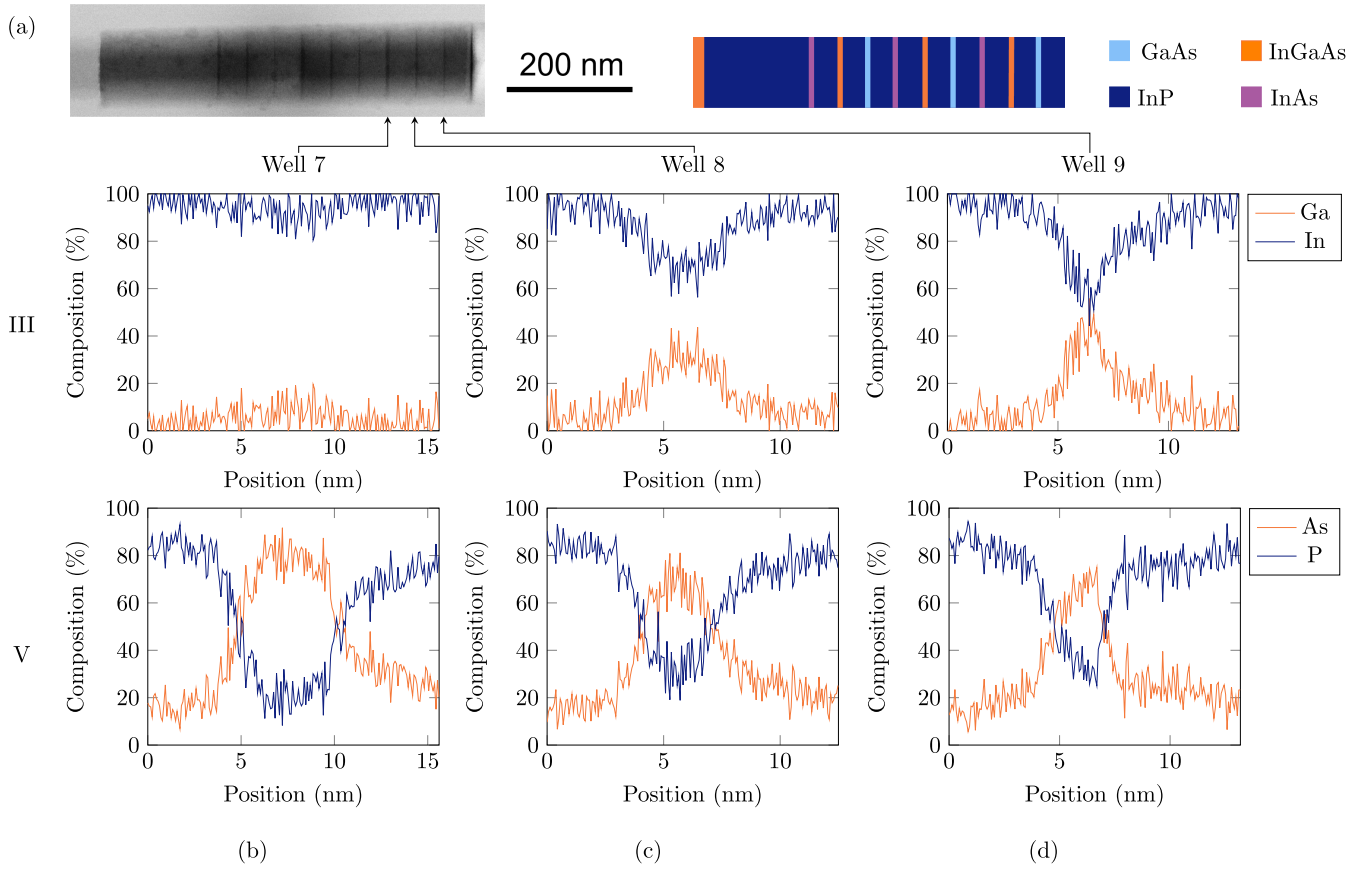

Figure 5. Analysis of sample 2. (a) BF-STEM image of the III−V nanowire, 9 lines corresponding to the arsenide layers and corresponding schematic drawing with colored layers indicating the design composition. Composition profiles for the seventh (b), eighth (c), and ninth (d) wells are calculated from EDS line scans carried out across the respective quantum well from left to right in the direction parallel to the growth axis.

nucleation event, the channel was obstructed by a parasitic nucleation growth within the channel, which extends outside the template. This type of growth configuration can potentially cause deposits similar to those in Figure 3a.

Yield Study. A survey of the arrays was carried out using samples 1 and 2, and involved 15,840 individual nanowires grown in 240 arrays grouped in 5 locations per sample. The areas investigated were the top left of the chips as well as randomly selected locations throughout it. Wires need to have two parallel visible {1 1 1} seed and end facets of equal length, and they need to have nucleated directly on the Si seed covering it in its entirety for them to be considered "perfect". Of the 15840 total wires, 14660 match these criteria, totaling a global yield of 92.55%.

Of the 7920 wires imaged for each sample, 7254 grew successfully in sample 1 and 7406 grew successfully in sample 2, resulting in corresponding growth yields of 91.59 and 93.51%. This result indicates that the different heterointerfaces of samples 1 and 2 do not significantly impact the growth yield.

Further analysis was carried out within each sample by comparing the growth yield for the templates parallel to the ⟨1 1 1⟩direction, and those tilted away from it. A larger number (9504 out of 15840) of wires of the first configuration were measured. For sample 2, the parallel and 20° misaligned configurations resulted in comparable growth yields of 93.73 and 93.75%, while sample 1 showed 94.84 and 86.71% growth yields for the same configurations. The larger difference in growth yields for parallel and 20° misaligned templates in sample 1 can be explained by one of the five randomly selected locations containing 20° misaligned arrays falling in an area of the chip with many nucleation issues. This area is reflected in Table 2 where sample 1 has a higher number of short and ungrown wires.

The total of 1180 nanowires that experienced growth failure are categorized according to the type of failure they experienced. Table 2 breaks down the number of defective wires for each sample between parallel and 20° misaligned templates by category. The first category, labeled "wrong facet", groups wires that terminate with a multifaceted surface or in a single facet that is not parallel to the seed surface and accounts for 368 wires (31.2% of the total defective wires). The second and largest category comprises wire locations hidden by a parasitic crystal (461 wires or 39.0% of the total failures). From a total of 240 arrays, 32 are affected by one or more parasitic crystals. Still, the parasitic crystals hide close to 15 (14.87 on average) locations for nanowire growth in each of these arrays. Hidden nucleation sites cannot be surveyed, and the wire status is unknown. If these wires are excluded from the total wire count on the basis that it is not certain how many of them are defective or perfect, the new total number of wires falls to 15,379 while the number of perfect wires stays at 14,660 raising the yield by 2.77 to 95.32%. The "oxide nucleated" category contains all of the cases where a III−V crystal randomly nucleated inside a template instead of the Si seed and counts 17 wires, 1.4% of the total. The wires in the category "seed exposed" have the expected end facet but did not fully cover the entire seed surface, leaving some of it exposed (8 wires, 0.7%). The category "long" comprises wires

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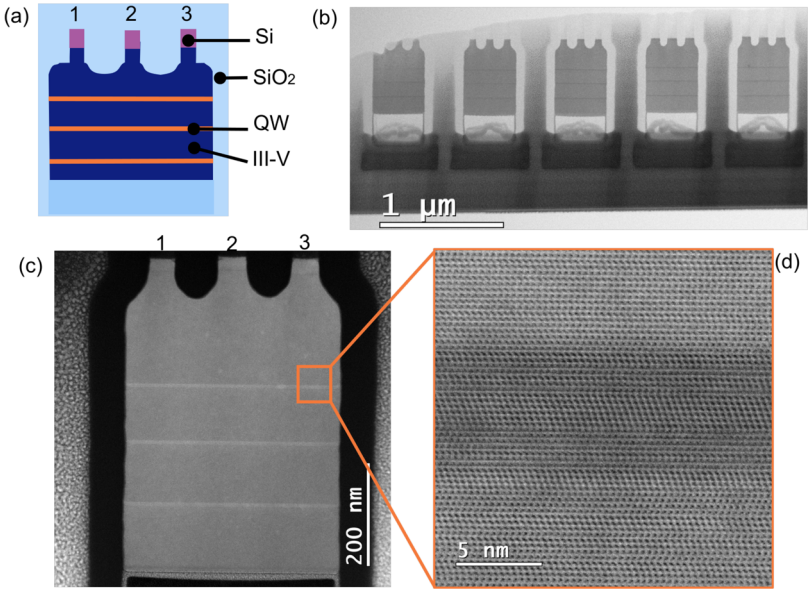

Figure 6. STEM analysis of quantum wells created in wide structures from the multiple nucleation sites. (a) Top-view schematic of the structure. (b) Plane-view image showing five adjacent structures. (c) ADF-STEM image of one structure. (d) High-resolution BF-STEM image of a single quantum well.

that were significantly longer than the others but did not have other defects, accounting for 0.7% of the defective wires for a total of 8. The last two categories are abnormally short wires and wire sites without growth with 211 (20.1%) and 81 (6.9%) counts each. These two categories of wires are more common in the area that presented nucleation issues in sample 1.

Heterointerfaces and Growth Rate in Nanowires. In-depth STEM and EDS analyses were performed to assess the structure of the nanowires. Figure 4a shows the STEM microscopy image of a FIB cross section of a wire from sample 1. The blurred regions at the top and bottom are due to the 30° cut angle employed to access the ⟨1 1 0⟩ imaging direction. The 4-nm-thin, on average, InGaAs segments are visible as 12 thin dark vertical lines in the dark gray body of the wire. The InGaAs layers visible in the cross section also act as time markers, recording the morphology of the growth front and revealing when a single facet is formed and maintained in the growth process. The observed 2° tilt of the heterolayers is explained by a tilt of the III−V lattice due to a strain relaxation-driven rotation of the crystalline growth axis during nucleation

Due to the presence of the SiO_2 template, the quantum wells develop only axially and not laterally. This results in improved composition control in heterolayers of ternary III−V compounds incorporated in the nanowires[25] and therefore is expected to allow for better control of the emission spectra. An EDS line scan of the last six InGaAs quantum wells was recorded along the direction indicated by the red arrow in Figure 4a. The resulting composition profiles are shown in Figure 4c, demonstrating consistent composition profiles across the wells with the In molar fraction being between 0.5 and 0.6. The uncertainty of 0.1 is given by the noise fluctuation of the EDS spectra.

A growth rate analysis is shown in Figure 4b, revealing a variation in the InP growth rate of around 6 nm min^{-1} from (20.7 ± 0.5) nm min^{-1} to (26.2 ± 0.2) nm min^{-1} along 600 nm of wire. Similarly, a 7 nm min^{-1} growth rate increase was recorded for the InGaAs segments. The error bars represent the 95% confidence interval on the measurement, calculated by averaging seven thickness measurements taken at various positions for each InP and InGaAs segment. This growth rate increase shows a moderate influence of the diffusional process on the growth dynamics of the samples.[32]

STEM and EDS analyses of sample 2 were conducted to assess the structure and influence of strained heterointerfaces (Figure 5a) on the growth of nanowires containing three InP-InAs-InP-InGaAs-InP-GaAs heterolayer sequences. Figure 5b shows the results of the InAs layer, where only the group V precursor must be switched. The EDS profile indicates that this layer has formed as intended with a phosphorus background level.

The InGaAs segment, with a target composition of $In_{0.53}Ga_{0.47}As$, grew In-rich, as seen from the EDS profiles in Figure 5c. A similar observation is made for the intended GaAs heterostructure: Figure 5d shows that this layer is heavily alloyed with a recorded In molar fraction close to 0.5. This indicates that the hold steps implemented in the growth recipe and designed to exhaust the group III element precursor (In) were set too short. Therefore, further optimization with prolongation of the purging step is suggested to improve composition control for these thin 3 nm wide heterostructures.

The growth rates of the InGaAs and InP layers were assessed with a process analogous to that used for the growth rates of sample 1. The InP growth rate is (23.8 ± 0.3) nm min^{-1} between the first InAs and the first InGaAs wells and (24.0 ± 0.4) nm min^{-1} between the third InAs and the third InGaAs wells. The InGaAs growth rates are (39 ± 3) nm min^{-1} for the first InGaAs well and (44 ± 2) nm min^{-1} for the third InGaAs well. All values are averaged from repeated measurements, and errors are given with 95% certainty. Thus, the growth rates of samples 1 and 2 are comparable for these materials.

The growth rates of the InAs and (expected) GaAs layers were analyzed using the same methodology. The InAs growth rate for the first InAs well is (26.4 ± 0.6) nm min^{-1} and (34 ± 1) nm min^{-1} for the third. The respective values for the first and third GaAs wells are (11.6 ± 0.9) nm min^{-1} and (12.5 ±

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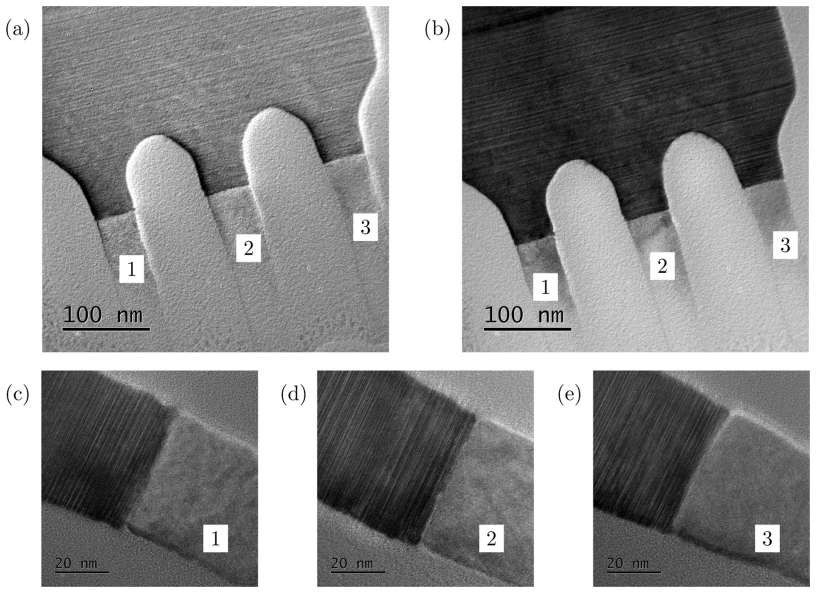

Figure 7. TEM analysis of the plane-view lamella. (a) BF-TEAM image of the nucleation and merge region, also shown in DF-TEM in (b). Close-ups of the left (c), middle (d), and right (e) interfaces between Si seeds and III−V material are also shown.

0.5) nm min^{-1}. This last result denotes a much slower growth for the (designed) GaAs layer, at around a fourth of the InGaAs quantum well. In conjunction with the alloying observed in the EDS analysis, these findings indicate that the growth-interrupting steps could be further optimized.

Growth of Wide Quantum Well Structures from Multiple Si Seeds. We fabricated test structures with a larger width to demonstrate the robustness of the developed epitaxy process and growth recipes. Furthermore, the template contains not only one Si nucleation area but three. Thus, the III−V crystal is nucleated in three points simultaneously and develops into short nanowires. These nanowires are then forced to merge into one large platelet with a well-defined geometry. The structure schematic is illustrated in Figure 6a.

Figure 6b shows a BF-STEM plane-view image of five adjacent structures after STEM lamella preparation. The image shows a high consistency in the overall size of the grown structures and in the presence of 15 quantum wells across five platelets. A single structure is shown in Figure 6c using annular dark-field (ADF-)STEM. The three light gray lines correspond to the InGaAs quantum wells. The high-resolution BF-STEM image in Figure 6d shows one of these quantum wells appearing in darker gray, with additional contrast from alternating stacking sequences forming rotational twin planes (RTPs), which are commonly observed for $\langle 1\ 1\ 1\rangle_B$ growth.[33] The quantum well runs uniformly throughout the entire width of the structure, indicating that the growth at this position took place on a single {1 1 1} plane. No other crystal defects were detected in the STEM mode.

Standard TEM analysis was performed to increase the sensitivity to detect structural defects (Figure 7). Figure 7c−e shows high-resolution BF images of the three Si/III−V junctions, confirming that nucleation was uniform and reproducible. No structural defects were detected beyond the III−V/Si interface, aside from the previously identified RTPs. BF and dark-field (DF) images of the structure are shown in Figure 7a,b and show uniform and featureless contrast. The varying intensity of the twin planes that run across the width of the sample is ascribed to thickness and alignment variation. A detailed inspection was conducted around the two expected merging points between the three crystals, with no indications of structural defects aside from RTPs. Tilting the sample to image other low Miller index planes was impossible with the available TEM sample holder.

No propagating dislocations or antiboundary defects from merging the three initial crystals could be detected. However, this does not exclude the possibility that lattice defects invisible under these imaging conditions might be present. It is unlikely for the three crystal lattices to merge in a perfect registry without the formation of defects.[34,35] However, here, the resulting defects remain confined: growth of smooth quantum wells that extend straight across the entire width of the structure would otherwise be impossible.

The specific sample geometry, growth directions, and material properties can explain these observations. The experiment is arranged so that a {1 1 1} growth front dominates and no other growth planes are formed. This is achieved by setting a growth condition favoring slow growth along the main ⟨1 1 1⟩ direction and fast growth in the ⟨1 1 0⟩ directions.[28] Under these conditions, efficient step flow occurs on the {1 1 1} facets. In such a configuration, the first wire to extend into the widening template section will spill over the spacers separating it from the neighboring wires and find itself supported on the other wire's {1 1 1} surface. Due to the efficient step flow on the {1 1 1} facets, mismatches of a few monolayers among the three wires are quickly resolved by forming one large growth surface that restabilizes a single $\{1\ 1\ 1\}_B$ growth front. A single crystal is established beyond these merging points, and growth can extend further into the template cavity. Growing one crystal with a single-faceted $\{1\ 1\ 1\}_B$ growth front in a step-flow regime allows for the creation of wider defect-free structures.[24]

CONCLUSIONS

We have grown and characterized III−V nanowires containing quantum wells directly on Si(1 1 0). This substrate allowed in-plane growth of III−V nanowires along the ⟨1 1 1⟩ directions, resulting in quantum wells oriented perpendicularly to the

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wafer surface. Optimizing the growth process to create a single $\langle 1\ 1\ 1\rangle_B$ growth facet resulted in a growth yield of 92.55%. Statistical analysis showed that neither a slight tilt in the mask orientation nor the growth of strained interfaces has a negative impact on the yield figure. Composition control and interface sharpness of the grown structures were assessed by EDS and TEM. Finally, we demonstrated the robustness of the growth process by forcing the merging of individual nanowires into a single structure. After the merging point, the quantum wells embedded in the crystal reveal the formation of a single-faceted growth front and the lack of dislocations and grain boundaries. Thus, the proposed approach is well suited for integrating electronic and photonic devices.

AUTHOR INFORMATION

Corresponding Authors

Enrico Brugnolotto − *IBM Research Europe - Zurich, 8803 Rueschlikon, Switzerland; School of Engineering, University of Glasgow, Glasgow G12 8QQ, United Kingdom;* orcid.org/0000-0003-2957-6823; Email: e.brugnolotto.1@research.gla.ac.uk

Marilyne Sousa − *School of Engineering, University of Glasgow, Glasgow G12 8QQ, United Kingdom;* Email: sou@zurich.ibm.com

Authors

Heinz Schmid − *IBM Research Europe - Zurich, 8803 Rueschlikon, Switzerland;* orcid.org/0000-0002-0228-4268

Vihar Georgiev − *School of Engineering, University of Glasgow, Glasgow G12 8QQ, United Kingdom;* orcid.org/0000-0001-6473-2508

Complete contact information is available at: https://pubs.acs.org/10.1021/acs.cgd.3c00806

Notes

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