Large-Scale On-Chip Integration of Gate-Voltage Addressable Hybrid Superconductor–Semiconductor Quantum Wells Field Effect Nano-Switch Arrays

Kaveh Delfanazari,* Jiahui Li, Pengchen Ma, Reuben K. Puddy, Teng Yi, Yusheng Xiong, Ian Farrer, Sachio Komori, Jason W. A. Robinson, David A. Ritchie, Michael J. Kelly, Hannah J. Joyce, and Charles G. Smith

Stable, reproducible, scalable, addressable, and controllable hybrid superconductor–semiconductor (S–Sm) junctions and switches are key circuit elements and building blocks of gate-based quantum processors. The electrostatic field effect produced by the split gate voltages facilitates the realization of nano-switches that can control the conductance or current in the hybrid S–Sm circuits based on 2D semiconducting electron systems. Here, a novel realization of large-scale scalable, and gate voltage controllable hybrid field effect quantum chips is experimentally demonstrated. Each chip contains arrays of split gate field effect hybrid junctions, that work as conductance switches, and are made from $In_{0.75}Ga_{0.25}As$ quantum wells integrated with Nb superconducting electronic circuits. Each hybrid junction in the chip can be controlled and addressed through its corresponding source–drain and two global split gate contact pads that allow switching between their (super)conducting and insulating states. A total of 18 quantum chips are fabricated with 144 field effect hybrid Nb- $In_{0.75}Ga_{0.25}As$ 2DEG-Nb quantum wires and the electrical response, switching voltage (on/off) statistics, quantum yield, and reproducibility of several devices at cryogenic temperatures are investigated. The proposed integrated quantum device architecture allows control of individual junctions in a large array on a chip useful for emerging cryogenic quantum technologies.

1. Introduction

Split-gate field effect transistors (FETs) consisting of source, drain, and split-gate electrodes are vital in integrated circuits, especially in facilitating energy-efficient high-speed switching in quantum hardware.[1,2] Semiconductors, such as InGaAs commonly form the channel of a FET and separate the source and drain metal electrodes. A gate dielectric electrically isolates the channel from the split gate electrodes. Therefore, the efficient operation of FETs depends on effective electrostatic coupling between the electric field caused by the split gate voltage and the semiconducting channel.[3] Classically, a FET functions as a conductance switch and operates in three regions.

Replacing the source-drain metal electrodes in conventional FETs with superconducting materials, such as niobium (Nb), will realize efficient and low-power consumption cryogenic logic

K. Delfanazari, Y. Xiong
Electronics and Nanoscale Engineering Division
James Watt School of Engineering
University of Glasgow
G12 8QQ Glasgow, UK
E-mail: kaveh.delfanazari@glasgow.ac.uk
K. Delfanazari, M. J. Kelly, H. J. Joyce
Electrical Engineering Division
Engineering Department
University of Cambridge
Cambridge CB3 0FA, UK

K. Delfanazari, J. Li, P. Ma, R. K. Puddy, T. Yi, D. A. Ritchie, M. J. Kelly,
C. G. Smith
Department of Physics
Cavendish Laboratory
University of Cambridge
Cambridge CB3 0HE, UK

I. Farrer
Department of Electronic and Electrical Engineering
University of Sheffield
Mappin Street, Sheffield S1 3JD, UK

S. Komori, J. W. A. Robinson
Department of Materials Science & Metallurgy
University of Cambridge
Cambridge CB3 0FS, UK

S. Komori
Department of Physics
Nagoya University
Furo-cho, Chikusa-ku, Nagoya 464-8602, Japan

devices, such as field effect controlled superconducting quantum point contacts (SQPCs) and gate-voltage controlled Josephson junctions (Josephson junction transistors or Josephson FETs).[4–7] Gate-controlled hybrid electronic devices have recently received considerable interest in quantum technology due to their unique technical advantages, e.g., they can work as conductance or current switches in cryogenic quantum circuits[8–10] or can be used as an artificial material platform for investigation of Andreev reflection, induced unconventional and topological superconductivity.[11–18] Such devices can therefore be engineered and integrated with wafer-scale semiconductor chips to form the building blocks of robust quantum computing systems. For these purposes, i) high yields, such as the reliability of hybrid junction and quantum device fabrication processes, ii) reproducibility of quantum phenomena from junction to junction and chip to chip, and iii) manufacturability of the complex hybrid quantum circuits must be systematically investigated. Such evaluation of hybrid junctions and coherent quantum circuits will inform us if they can be integrated into a scalable architecture for their use in real superconducting quantum hardware.

Here, for the first time, we report successful micro and nanofabrication of large-scale arrays of field-effect hybrid devices on an $In_{0.75}Ga_{0.25}As/GaAs$ semiconducting heterostructure chip. Our design and fabrication technique bring several advances to the scalable hybrid superconducting-semiconducting quantum circuits for the realization of cryogenic quantum hardware with complex structures: i) Our approach in using $In_{0.75}Ga_{0.25}As$ 2D electron gases (2DEG), which is located 120 nm below the wafer surface, while is challenging for circuit fabrication, opens up new opportunities for the integration of hybrid quantum circuits with InGaAs based advanced semiconducting electronic integrated circuits (IC). Moreover, the ability to tune the indium composition permits the formation of highly transmissive metal–semiconductor interfaces. ii) Our superconducting materials have not been sputtered in the same chamber as the semiconducting wafers making the quantum circuit fabrication accessible, and user-friendly as in situ deposition of superconducting and semiconducting films is expensive and out of the capability and affordability of most research groups. iii) Using Nb, as a type II superconductor with a larger superconducting gap and higher transition temperature compared to commonly used in situ fabricated Al-based circuits, allows the operation of hybrid quantum circuits at relatively high magnetic fields and high frequency making them compatible with most emerging quantum circuit platforms based on superconducting microwave coplanar waveguide resonators and circuit quantum electrodynamic systems. In fact, making high-quality Nb-2DEG interfaces, especially in large arrays, is much more challenging than Al-based hybrid interfaces, because of the nature of Nb-based hybrid interfaces, which we successfully overcome here. Our advanced techniques used in this work will help open up a new route toward the development of Nb-based hybrid quantum circuits. iv) For the first time, we fabricated a hybrid quantum IC on a large scale that is addressable and controllable with voltage signals, that is robust against noise compared to current biased circuits, in a compound material platform with a complex design and fabrication process compatible with the most advanced semiconducting ICs. v) The interesting properties of $In_xGa_{1-x}As$ 2DEG, such as low electron effective mass, large g-factor, and strong Rashba spin–orbit cou-

pling, make them a very attractive material platform for applications in electronics, spintronics, and photonics topological quantum computing.
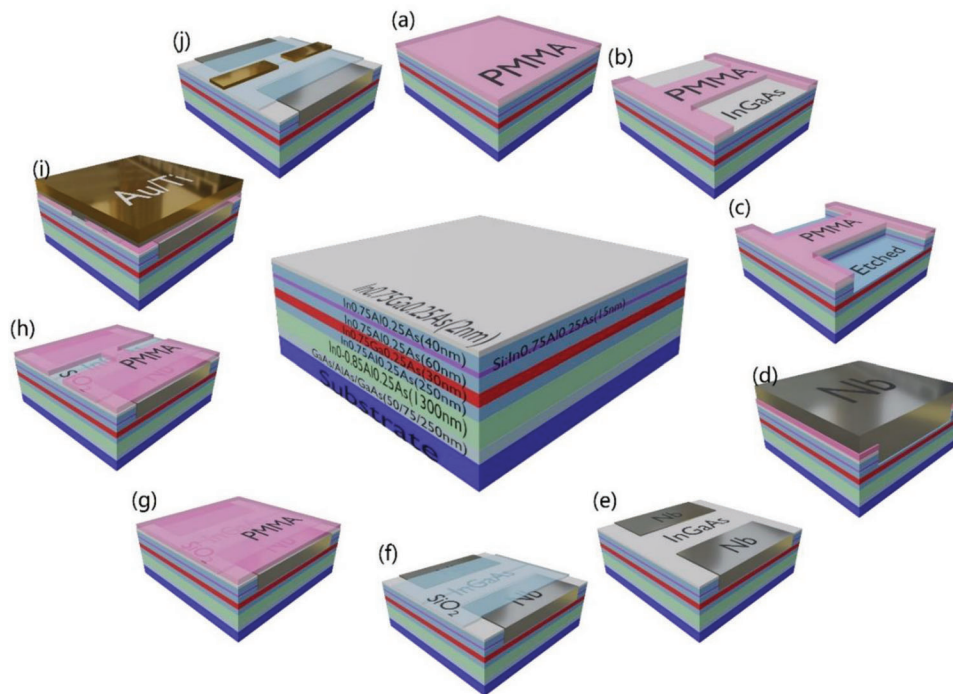
Therefore, the presented work is a considerable step toward realizing advanced voltage-tunable, low-power cryogenic quantum hardware based on hybrid superconductor–semiconductor electronic circuits.

2. Results and Discussion

The proposed quantum chip is based on $In_{0.75}Ga_{0.25}As/GaAs$ heterostructure as shown in **Figure 1**. The $In_{0.75}Ga_{0.25}As$ 2DEG with a 30 nm thickness is buried 120 nm under the surface. The wafer is first chemically cleaned with Acetone, and IPA, respectively. Usually, a 30s of oxygen plasma ashing is included in the cleaning processes. The fabrication of split-gate hybrid junctions starts with the mesa section in which the 2DEG is isolated with respect to electrodes that are defined later. The PMMA is spin-coated on the wafer as shown in Figure 1a, and e-beam patterning is performed to define the superconducting electrode pads which are Nb in this work as shown in Figure 1b. A chemical wet etching (see Figure 1c) followed by the formation of the 2DEG channel is performed before the Nb sputtering (Figure 1d), to form the hybrid Nb-2DEG-Nb junction as shown in Figure 1e. The chemical wet etchant is $H_2SO_4:H_2O_2:H_2O = 1:8:1000$ with a typical etching rate of 1 nm s^{-1}. Afterward, a 50 nm SiO$_2$ oxide layer grown via chemical vapor deposition (CVD) is used to isolate the junction as shown as a transparent blue layer in Figure 1f. Extra Buffered Hydrofluoric Acid will open the window for electrodes. Then another PMMA e-beam pattern is performed to define the split gate as shown in Figure 1e–h. Finally, the gate is defined via Au/Ti thermal evaporation followed by lift-off and a gated junction is fabricated as shown in Figure 1i,j. The ohmic contact area is made of gold/germanium/nickel (AuGeNi) to form a low resistance and good chemical bond (adhesion) to the semiconductor substrate. These pads are placed 100 μm away from the junctions to reduce the impact of the normal electrons on the superconducting electrons. The ohmic is etched down to the 2DEG region to perform tunnelling spectroscopy measurements between Nb and 2DEG. For ease of demonstration, only the fabrication process of a single hybrid junction is shown in Figure 1, however, the design allows wafer-scale nanofabrication.

A total of 144 gate-controllable hybrid S–Sm–S junctions are engineered and patterned on the surface of a semiconducting $In_{0.75}Ga_{0.25}As/GaAs$ heterostructure wafer. Every 72 hybrid junctions are designed to fit across nine smaller chips of 1×1 cm^2, each small chip containing an array of eight hybrid double (16 single) interface junctions embedded in superconducting circuits.

The eight hybrid junctions in each small chip are purposely fabricated with either identical or different geometries to investigate the reproducibility and robustness of the electrical response. They are individually controlled by two global gate pads; one pad is designed to control the left side and the other pad to control the right side of each split gate in the superconducting integrated circuits. Some junctions failed during the fabrication or wire bonding process, and their data are excluded from this study. **Figure 2**a shows the false-colored optical image of a

**ADVANCED
SCIENCE NEWS**

www.advancedsciencenews.com

**ADVANCED
ELECTRONIC
MATERIALS**

www.advelectronicmat.de

Figure 1. Hybrid superconductor–semiconductor quantum chip fabrication process: the schematic demonstration of a semiconducting wafer based on InGaAs/GaAs heterostructure is shown in the center. The 2DEG is a 30 nm thick $In_{0.75}Ga_{0.25}As$ quantum well located 120 nm beneath the surface. a) PMMA spin-coated on the wafer. b) E-beam patterning is performed, and PMMA is developed to form the pattern. c) Chemical wet etching to remove the layers above the 2DEG. d) Nb is sputtered on the etched area of the wafer. e) The Nb is lift-off, and the junction is formed. f) A 50 nm thick SiO_2 oxide layer grown by chemical vapor deposition (CVD). g) PMMA spin-coated. h) E-beam patterning and developing. i) Au/Ti is thermally evaporated on the PMMA pattern. j) The final step for a gated device fabrication after the lift-off of Au/Ti.

large-scale hybrid quantum chip before the final fabrication stages and dicing. The chip contains a total of 72 double interfaces (Nb-2DEG-Nb) junctions or 144 single interfaces (Nb-2DEG or 2DEG-Nb) junctions in a 1×1 cm^2 dimension. Figure 2b shows a packaged addressable quantum chip containing the structure shown in Figure 2c, which is wire-bonded to a leadless chip carrier (LCC) to be mounted in the cold finger of a cryostat or dilution refrigerator for characterization and cryogenic measurements. A chip-integrated field effect addressable quantum IC with an array of eight split gate hybrid double junctions is developed. It shows the false-colored optical image of one of the nine completed devices shown in Figure 2a after dicing and wire-bonding. The hybrid junctions are made from superconducting Nb as their source and drain electrodes and high-quality $In_{0.75}Ga_{0.25}As$ 2DEG as their active region.[19]

The yellow and orange pads and lines in the chip (see Figure 2c) are the two universal gate pads in the chip addressing the junctions and controlling the Cooper-pairs density between the source and drain of each hybrid junction through the application of an external DC voltage across two sides of split gates (yellow for the left, and orange for the right split gate controllers, respectively). Figure 2d is the false-colored SEM image of one gate-voltage controlled field-effect hybrid symmetric and planar 2D junction on the chip. The dashed-red rectangle area in (d) is enlarged and shown in Figure 2e, demonstrating the width w_c and length L_c of the constriction formed by the split gates. The side view of a field effect switch is schematically illustrated in

Figure 2f, where $In_{0.75}Ga_{0.25}As$ 2DEG, Nb electrodes, and gates are shown in red, grey, and yellow, respectively. The designed geometrical parameters of eight hybrid switches in each quantum chip are summarised in **Table 1**. The junction parameters are chosen to be large enough to investigate topological superconductivity in 2D systems[20–22] in the future generation of such devices. The geometrical parameters may vary from device to device after nanofabrication, especially for the length and width of the junctions, as the wet etch technique was used to take the unwanted semiconducting heterostructure areas and form source-drain leads and the active 2DEG region in between them. The fabricated junction parameters are commonly shorter than their designed dimensions.[13–19]

A depletion layer will form around the gate electrodes by applying a negative gate voltage to the split gates which defines a constriction in the quantum wells between two

Table 1. The designed geometrical parameters of eight hybrid field effect switches integrated into a single quantum chip.

| Junctions	J_1	J_2	J_3	J_4	J_5	J_6	J_7	J_8
L_c [nm]	400	400	400	400	400	400	400	400
W_c [nm]	400	300	200	100	100	100	100	100
L_J [μm]	1.4	1.4	1.4	1.4	1.4	1.4	1.4	3.2
W_J [μm]	5	5	5	5	5	5	5	5
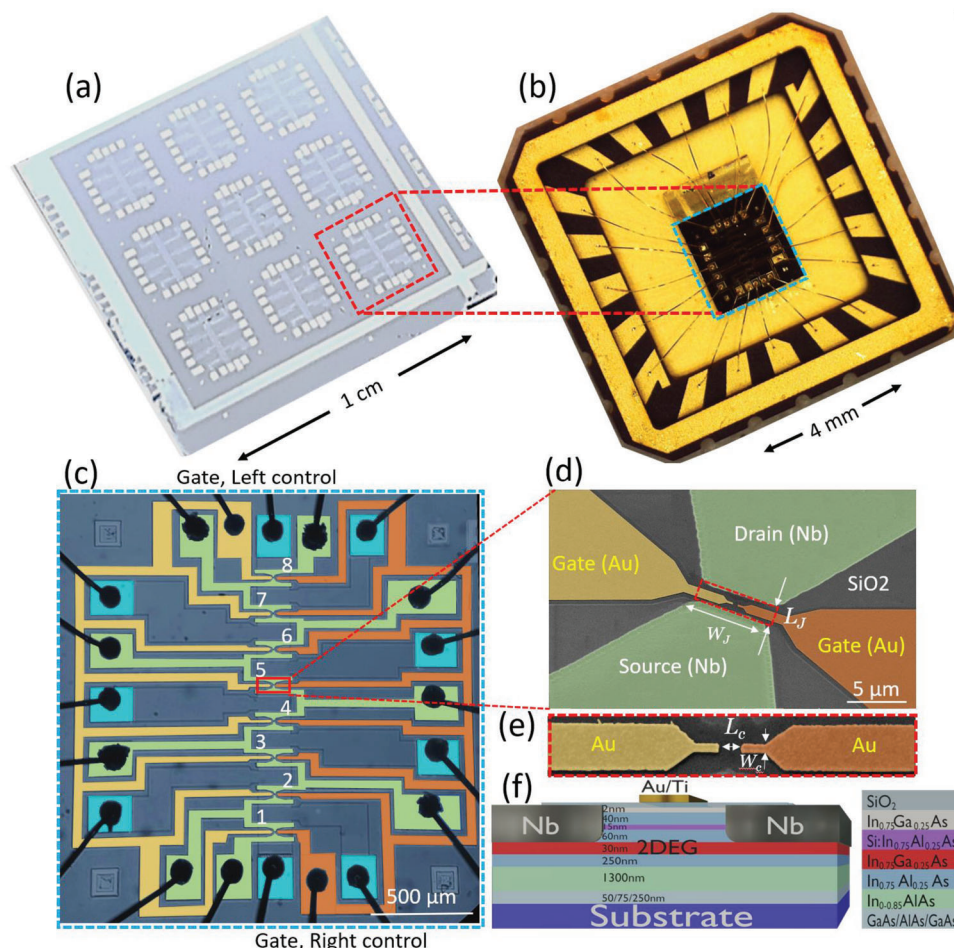
Figure 2. Gate voltage addressable hybrid quantum chip: a) the false-colored optical image of a chip containing large-scale integration of hybrid semiconductor–superconductor junctions, before the final fabrication stages. The chip contains a total of 72 double interfaces (Nb-2DEG-Nb) and 144 single interfaces (Nb-2DEG or 2DEG-Nb) junctions. b) A packaged addressable field effect quantum chip containing the chip shown in (c) after wire bonding to a leadless chip carrier (LCC). The chip is mounted in the cold finger of a cryostat or dilution refrigerator for the sub-Kelvin cryogenic test. c) The false-colored optical image of the addressable hybrid quantum chip containing an array of hybrid junctions made from superconducting Nb and high-quality $In_{0.75}Ga_{0.25}As$ 2D electron gas (2DEG) in $In_{0.75}Al_{0.25}As/GaAs$ heterostructure. Each junction in the chip can be addressed by applying voltages through two universal gate pads which are colored yellow and orange. The ohmic contacts, shown with cyan pads, are etched down to the 2DEG region, for the purpose of tunnelling measurements between Nb and 2DEG (the data is not shown here). The area between Nb and ohmic pads is all etched away except the active area where hybrid junctions are formed (mesa area). d) The false-colored SEM image of one gate-voltage controlled hybrid symmetric and planar 2D junction on the quantum chip. e) The dashed-red rectangle area in (d) is enlarged showing the split-gates area with a constriction width W_c and length L_c made from Au. A 50 nm thick SiO_2 dielectric was deposited to isolate the gates from the source-drain electrodes of the junctions. f) Schematic illustration of a field effect hybrid switch from the side view with detailed semiconducting heterostructure nanolayers. The 30 nm $In_{0.75}Ga_{0.25}As$ 2DEG is shown in red.

superconducting leads.[23,24] The constriction works as an electron waveguide (conducting quantum channel) in such a 2D electron system in our chips.[25] The split gate structure allows modulation of carrier density and mobility of the quantum wells beneath the gate electrodes and in the constriction area of the hybrid junction through the application of gate voltages. When the gate voltage is swept to negative values, the constriction length L_c will reduce from its initial value $L_c = 400$ nm to $L_c = 0$ in perfect conditions. Therefore, the split gate is a knob to control the hybrid switches' electronic response. The carrier density and mobility of the $In_{0.75}Ga_{0.25}As$ 2DEG in semiconducting heterostructure are defined by Shubnikov–de Haas measurement (see Experimental Section). The electron

mass of the 2DEG is determined to be $m^* = 0.039\ m_e$, where m_e is the free electron mass.[26] From $In_{0.75}Ga_{0.25}As$ 2DEG properties, the coherence length $\xi_N = \hbar v_F/2\pi k_B T \cong 200$ nm, assuming $T = 4$ K, and mean free path $l_e = e^{-1}\hbar\mu_e\ (2\pi n_s)^{1/2} \cong 2\ \mu m$ are calculated. Here, v_F is the Fermi velocity. Consequently, the hybrid junctions fit into the clean limit regime ($l_e > \xi_N$) with ballistic transports ($l_e \gg L$).[13]

Figure 3 plots the switching response of eight field effect devices (J1-J8) fabricated in a single chip, with the dimensions given in Table 1. All junctions are measured twice: i) the split gate voltage V_g is swept from $V_g = 0$ to -1 V (shown in black solid lines), and ii) V_g is returned from $V_g = -1$ to 0 V (shown in red solid lines). This measurement aims i) to study the
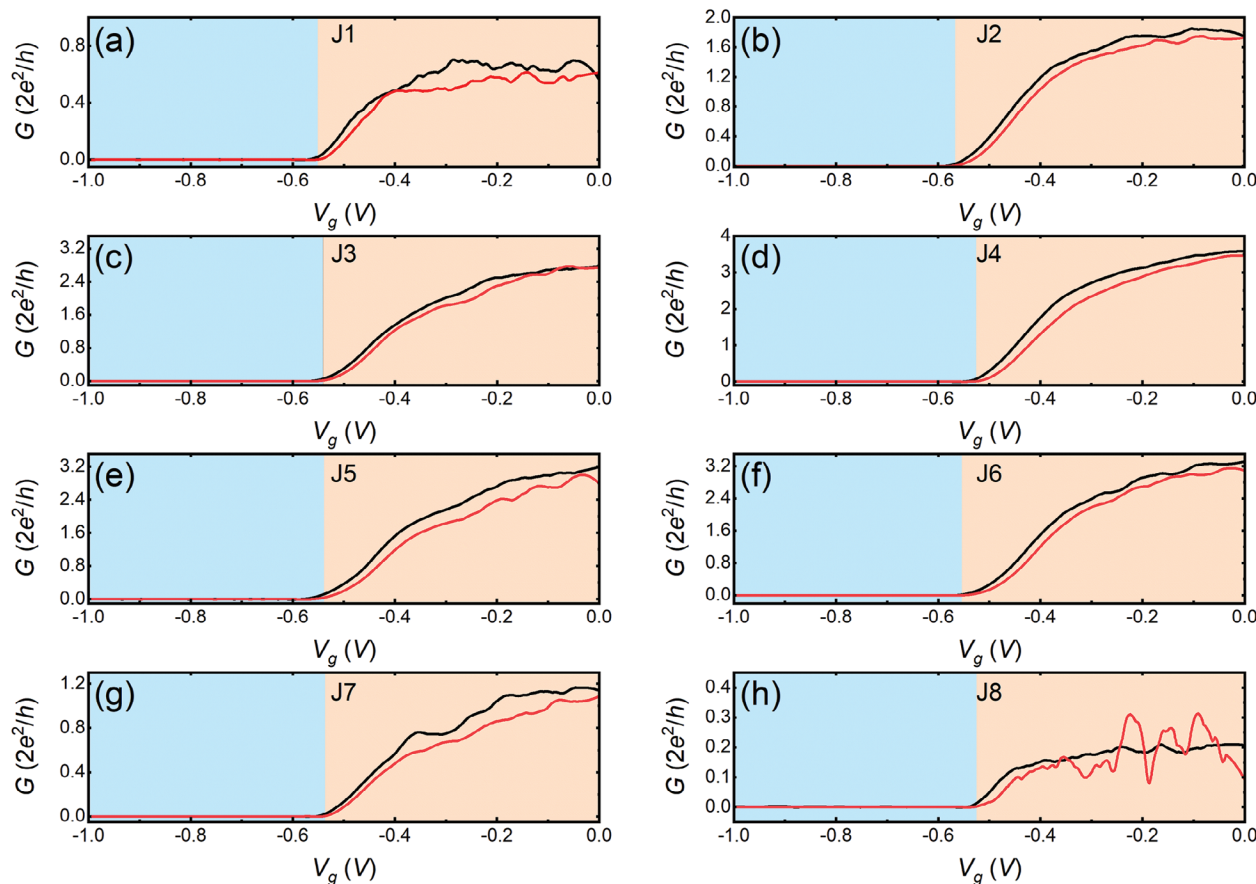
Figure 3. The conductance as a function of the electric field on the gates for eight (all) junctions in a single chip, measured at $T = 4$K. a) J1, b) J2, c) J3, d) J4, e) J5, f) J6, g) J7, and h) J8. There are two sweep directions from 0 to -1 V (black) and then from -1 to 0 V (red). Relatively good reproducibility of both effects are observed for all junctions in this chip.
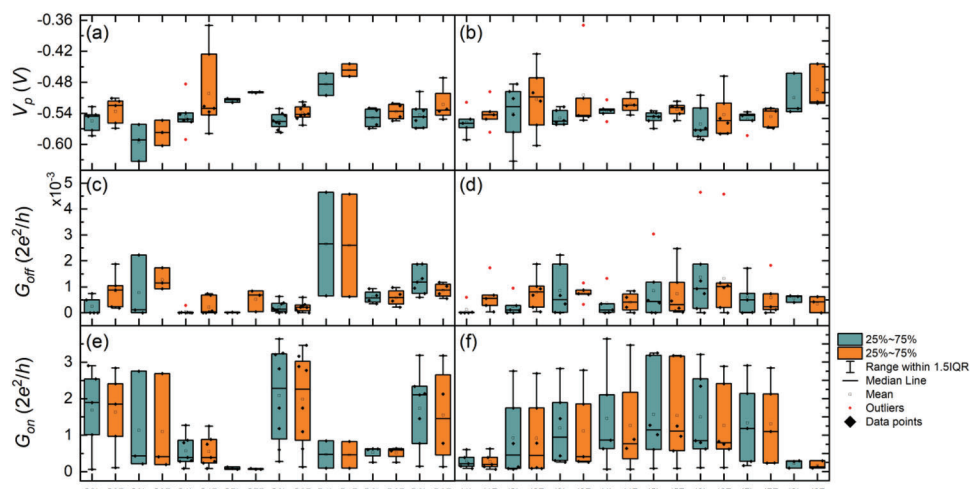
reproducibility of the conductance switching of each junction for two different sweep directions. ii) to investigate the reproducibility of conductance switching in junctions of various dimensions (but similar geometry) in a single chip.

We observe a relatively good reproducibility for two split gate voltage sweep directions (L and R) for all junctions in this and almost all measured chips. We observe conductance switching with very small hysteresis except for J8 which was purposely designed and fabricated larger than other junctions. This suggests that the quality and uniformity of the hybrid circuit gates, gate pads, and CVD-grown SiO_2 dielectric layer under gates used in the chips are of high fabrication standards. Moreover, the gate voltage leakage and Joule heating in most junctions are negligible or quite small, so the conductance curves for both sweep directions are almost overlapped. Since the distance between the Nb leads ($L_J = 3.2$ μm) is long in J8, hot electrons seem to lead to Joule heating and hysteresis in the junction so the left and right conductance sweeps do not fully overlap, nevertheless, the switching voltage is not affected. The orange and blue areas in Figure 3 show the hybrid switch ON and OFF states, respectively. Only a small DC switching voltage of $V_g = -0.55$ V is required to change the hybrid junction from conducting to isolating state. The ON state conductance G_{ON} of the

junctions varied by the junction's parameters, suggesting that the junctions' dimensions are altered during the fabrication process.

In **Figure 4**, the green color boxes are the data for left (0 to -1 V), and the orange boxes are the data for right (-1 to 0 V) gate voltage sweep directions, respectively, with 25–75% data distribution in the boxes. 1.5IQR is that 95% of the data points are distributed in the range. The Median is the middle value of the data distribution. The mean is the average of the data points. Outliers are the data points outside the 1.5IQR. The pinch-off (switching) voltages V_p, and ON (G_{ON}) and OFF (G_{OFF}) state conductance values are studied for a large number of chips, and junctions as summarized in Figure 4.
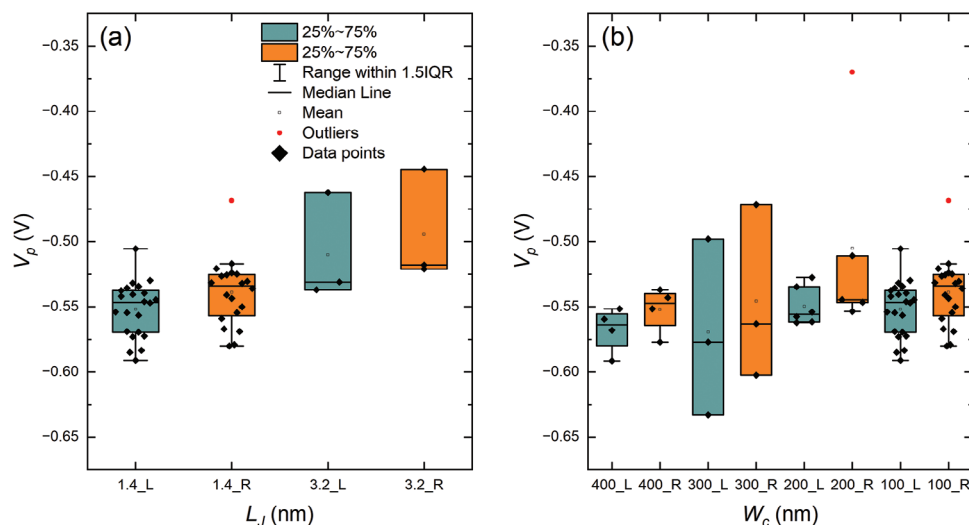
As shown in Figure 4a,b, the average pinch-off voltage V_p for both (L), and (R) sweep directions is ≈ -0.56 V for >75% of all measured junctions in a large number of chips (note that some junctions are not measured due to failure reasons, such as wire-bonding issues or broken contact pads). We observe relatively reproducible and consistent conductance switching response to the electric field induced by the split gates for several measured devices. This suggests that the next-generation hybrid nano-switches with improved design and performance could be used to control the cryogenic electronic hardware by the application of only -0.56 V or fewer DC voltages.

ADVANCED
SCIENCE NEWS

www.advancedsciencenews.com

ADVANCED
ELECTRONIC
MATERIALS
Open Access

www.advelectronicmat.de

Figure 4. Switching (pinch off) voltage of a) all measured chips, b) each with eight junctions for different sweeping directions measured at $T = 4$ K. Green color boxes are the data for the left sweeping gate voltage (0 to -1 V) and the orange boxes are the data for the right sweeping gate voltage (-1 to 0 V). c) Off-state conductance G_{off} for all the measured chips, each with eight junctions d) measured at $T = 4$ K. e) On-state conductance G_{on} for all the measured chips, shown as C or D, each with eight junctions f) measured at $T = 4$ K. On-state refers to the height of the conductance at zero gate voltage.
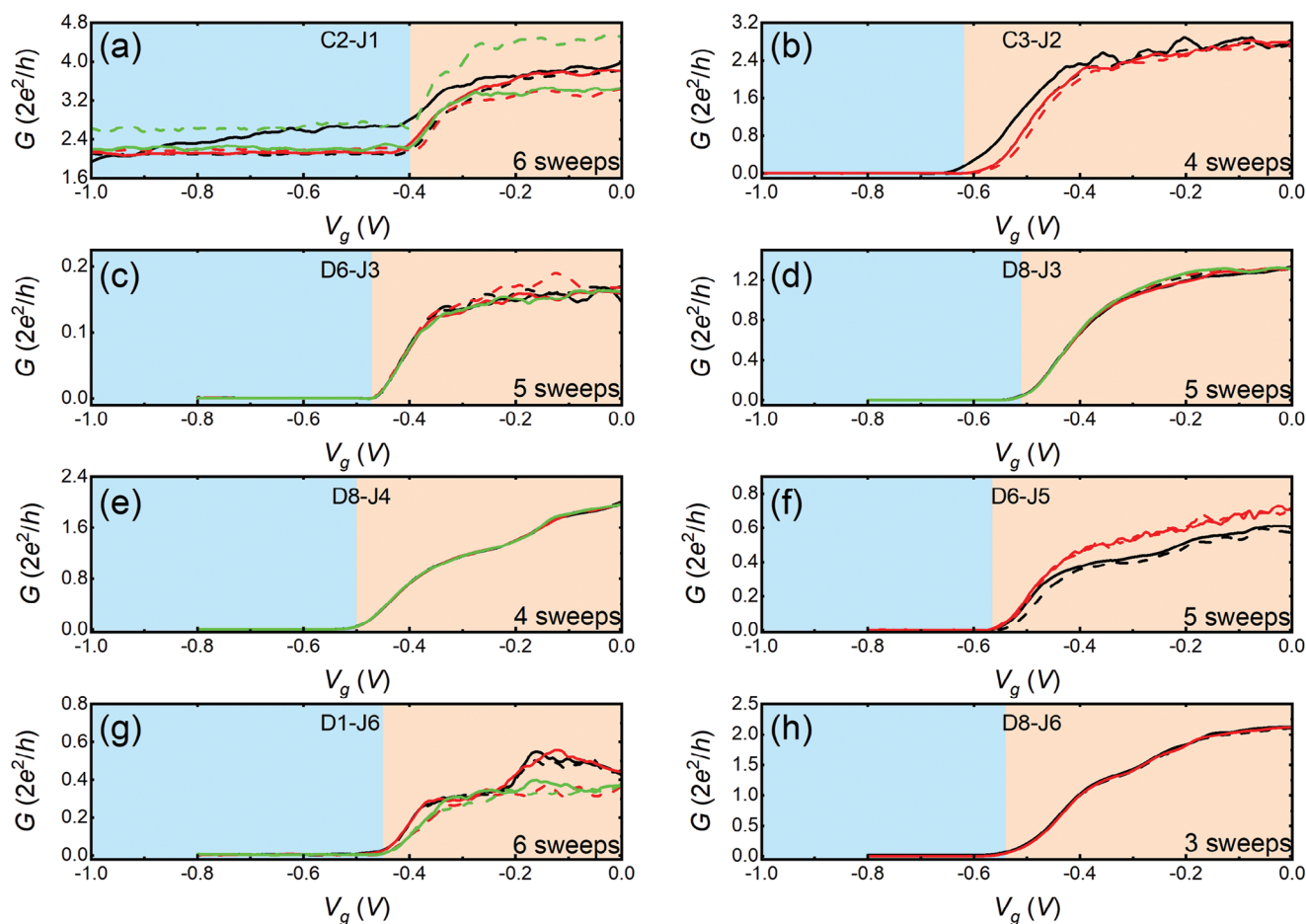
Figure 5. The conductance as a function of the electric field on the gates for devices with multiple sweeps to examine the reproducibility of the switching voltage, and ON and OFF states conductance.

2300453 (6 of 9)

**ADVANCED
SCIENCE NEWS**

www.advancedsciencenews.com

**ADVANCED
ELECTRONIC
MATERIALS**

www.advelectronicmat.de

Figure 6. Pinch off voltage V_p as a function of junction length L_J. Green color is the data for the left sweeping gate voltage (0 to -1 V), and the orange boxes are the data for the right sweeping gate voltage (-1 to 0 V). The data for chips 5 and 6 is absent. 1.5IQR is that 95% of the data points are distributed in the range. 25–75% means 25–75% of data are in the box. The median is the middle value of the data distribution. Mean is the average of the data points. Outliers are the data points outside the 1.5IQR. b) Pinch off (switching) voltage V_p as a function of constriction width W_c.

We also investigated the OFF-sate conductance G_{OFF} of the hybrid junctions in measured chips and plotted them in Figure 4c,d. The OFF-state conductance values for the majority of devices are almost zero soon after the application of ≈ -0.56 V confirming the uniformity of large-scale CVD-grown SiO_2 dielectrics on the wafer before dicing and forming the packaged quantum chips. Figure 4 suggests that the majority of the fabricated and measured field effect devices work as an ideal low dissipation switch under the application of split gate electric field in both voltage sweep directions. To analyze the manufacturability of the hybrid junctions we plot the ON state conductance G_{ON} for a number of chips as shown in Figure 4e,f. We find that G_{ON} varies from chip to chip suggesting that the geometrical and interfacial parameters of the hybrid junctions may change during the fabrication process. In order to have a more uniform response attention should be paid to etch process optimization to improve the hybrid junction interfaces. To be used in quantum circuits and processors, the large-scale manufacturability of hybrid conductance switches depends strongly on their reproducible and identical operational parameters. Here, we further investigate the reproducibility of switching voltage and ON-OFF state conductance parameters for several hybrid devices, both from the same and different chips, under multiple voltage sweeps (more than three times) as shown in **Figure 5**. We find that despite slight variation due to fabrication errors, the devices show many repeatable behaviors.

For example, although J1 of chip 2 does not completely pitch off even by the application of a large negative voltage, the conductance traces for six sweeps show slight deviation which could come from the nonuniform SiO_2 oxide layer under the split gates, slight gate leakage, and Joule heating due to the application of large voltages. The conductance switching failure of this device may be attributed to the formation of a different thickness of SiO_2 oxide layer compared to that of other junctions that show very good reproducibility and identical switching parameters (for in-

Table 2. Junction length L_J and constriction width W_c correlated quantum yield. The yield is subdivided into different junction lengths and constriction sizes. The table sorts total switching devices versus measured devices with the specific size.

L_J [µm]	1.4	1.4	1.4	1.4	3.2
W_c [nm]	400	300	200	100	100
Switching Devices	6	6	6	26	5
Measured Devices	7	7	8	35	9
Yield [%]	85.7	85.7	75	74.3	55.6

stance see D8- J3, and D8- J4 & J6 for several sweeps). This non-uniformity may be due to the formation of a thicker oxide layer, which prevents the hybrid junction from being completely pinch-off and switching off from a conductive to an insulator state. We further investigate the relationship between the dimensions of gated hybrid junctions and their pinch-off voltages and show the results in **Figure 6**. Specifically, the junction length L_J is found to have a slight positive correlation with the pinch-off voltage, with longer junctions requiring a lower voltage to pinch off the channel.

As shown in Figure 6a, this positive correlation may be due

Table 3. Two sets of measured devices are labeled with "C" and "D". The quantum yield counts for the working hybrid switch devices (showing switching response when the split gate voltage is swept to negative values) are divided by the total number of measured hybrid devices.

Chip ID	C1	C2	C3	C4	C7	C8	D1	D6	D8	D9	Total
Switching Devices	0	6	3	7	6	8	2	6	7	4	49
Measured Devices	8	7	8	8	8	8	2	6	7	4	66
Yield [%]	0	86	38	88	75	100	100	100	100	100	74.24

ADVANCED
SCIENCE NEWS

www.advancedsciencenews.com

ADVANCED
ELECTRONIC
MATERIALS
Open Access

www.advelectronicmat.de

to weaker proximity effects in the middle of the longer junctions under the gate, resulting from the extended junction length. Consequently, less gate perturbation may disturb the induced superconductivity, leading to an earlier pinch off of the channel. However, more data is needed to draw definitive conclusions about this relationship. In contrast, no obvious correlation is observed for constriction width W_c. In theory, the width determines the length of the quasi-1D/1D channel, and if this length is much smaller than the scattering length/mean free path, the channel remains in the ballistic regime. Further theoretical analysis and simulations are needed to confirm this hypothesis. This will also motivate us to study these devices at lower temperatures to properly form the 1D channels. As these studies are not the focus of the present work will be discussed elsewhere. In **Table 2**, we summarize the yield with respect to the junction and constriction dimensions. The constriction width W_c varies from 400 to 100 nm with fixed junction length $L_J = 1.4$ μm. As another control knob, junctions with $W_c = 100$ nm and $L_J = 3.2$ μm are fabricated to study the effects of the longer junctions. Such devices are found to show the minimum ON state conductance as discussed above and therefore offer the lowest yield. A slight reduction in quantum yield is observed with decreasing constriction width W_c.

Most of the non-switching junction with small W_c shows negligible conductance at zero gate bias, which may be due to the surface charge accumulation under the split gates that are enough to pinch off the channel without extra gate bias or due to the electron leak into the gate rather than transport from source to drain. We observe a total yield of 74.24%, which counts for the working switches divided by the total number of measured devices, for a large array of hybrid devices as shown in **Table 3**. This includes yield for reproducibility of the conductance of individual hybrid switches when their split gates voltage is swept from 0 to −1 V and then reversed from −1 to 0 V.

3. Conclusion

We reported the first successful micro and nanofabrication of a large array of chip-integrated hybrid field effect quantum nanoelectronics devices and demonstrated a systematic experimental investigation of their conductance switching performance under the application of gate electric fields. We demonstrated techniques for the successful fabrication of novel cryogenic gate voltage addressable nanoelectronics chips with negligible gate voltage leakage and with high switching response statistics, reproducibility rate, and quantum yields. We found that to make efficient cryogenic switches, the attention should especially be on the quality junction geometrical and interfacial parameters as the former influence the uniform switching voltages and the latter have a direct effect on the ON-OFF state conductance. The OFF-state conductance is also a function of the quality oxide layers isolating the source-drain electrodes of hybrid junctions from split gate electrodes. The techniques and experimental data presented here show that our field effect nano-switch devices, with modified designs and fabrication strategy, may help the development of novel cryogenic electronic switches for various classical or quantum cryogenic applications.

4. Experimental Section

Device Fabrication: The devices were based on MBE-grown $In_{0.75}Ga_{0.25}As$ quantum wells in $In_{0.75}Al_{0.25}As$/GaAs high mobility semiconducting heterostructure. The wafer's detailed information had been discussed in the earlier works.[26] A three-inch wafer was diced into smaller pieces of 1.5 × 1.5 cm chips. From the bottom to the surface of the chip, it contained a GaAs substrate (500 μm), buffer layers of GaAs, AlAs and GaAs (50, 75, and 250 nm), an InAlAs step-graded buffer layer (1300 nm), and an InAlAs buffer layer (250 nm). The 2DEG was a 30 nm thick $In_{0.75}Ga_{0.25}As$ quantum well with electron density $n_s = 2.24 \times 10^{11}$ (cm^{-2}) and mobility $\mu_e = 2.5 \times 10^5$ ($cm^2 V^{-1} s^{-1}$) in the dark. On top of the 2DEG quantum well, there were layers of $In_{0.75}Al_{0.25}As$ spacer (60 nm), n-type modulation-doped $In_{0.75}Al_{0.25}As$ (15 nm), $In_{0.75}Al_{0.25}As$ layer (45 nm), and InGaAs cap layer (2 nm).

Device Characterization and Cryogenic Measurements: The devices were characterized to ensure the height of resists, active regions, insulator thickness, etc., by Dektak Surface Profilometer, Veeco, before dicing. Each LCC led quantum chip was loaded into a 4K dip station for cryogenic tests. A standard lock-in technique was used to measure the quantum transport by superimposing a small ac-signal at a frequency of 70 Hz and an amplitude of 5 μV to the hybrid junction DC bias voltage and measuring the ac-current. The gates were swept by DC voltages supplied from NiDAQ national instruments modules that could provide low noise signals between ± 10 V_{DC}.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

[1] T. D. Clark, R. J. Prance, A. D. C. Grassie, *J. Appl. Phys.* **1980**, *51*, 2736.
[2] M. Shur, *Appl. Phys. Lett.* **1989**, *54*, 162.
[3] M. Shur, L. F. Eastman, *IEEE Trans. Electron Devices* **1979**, *26*, 1677.
[4] T. Nishino, M. Miyake, Y. Harada, U. Kawabe, *IEEE Electron Device Lett.* **1985**, *6*, 297.
[5] H. Takayanagi, T. Kawakami, *Phys. Rev. Lett.* **1985**, *54*, 2449.
[6] Z. Ivanov, T. Claeson, T. Andersson, *Jpn. J. Appl. Phys.* **1987**, *26*, 1617.
[7] T. Nishino, M. Hatano, H. Hasegawa, F. Murai, T. Kure, A. Hirawa, K. Yagi, U. Kawabe, *IEEE Electron Device Lett.* **1989**, *10*, 61.

[8] T. W. Larsen, K. D. Petersson, F. Kuemmeth, T. S. Jespersen, P. Krogstrup, J. Nygård, C. M. Marcus, *Phys. Rev. Lett.* **2015**, *115*, 127001.

[9] G. De Lange, B. Van Heck, A. Bruno, D. J. Van Woerkom, A. Geresdi, S. R. Plissard, E. P. A. M. Bakkers, A. R. Akhmerov, L. Dicarlo, *Phys. Rev. Lett.* **2015**, *115*, 127002.

[10] S. J. Weber, *Nat. Nanotechnol.* **2018**, *13*, 877.

[11] J. Shabani, M. Kjaergaard, H. J. Suominen, Y. Kim, F. Nichele, K. Pakrouski, T. Stankevic, R. M. Lutchyn, P. Krogstrup, R. Feidenhans'l, S. Kraemer, C. Nayak, M. Troyer, C. M. Marcus, C. J. Palmstrøm, *Phys. Rev. B* **2016**, *93*, 155402.

[12] M. Pita-Vidal, A. Bargerbos, C.-K. Yang, D. J. Van Woerkom, W. Pfaff, N. Haider, P. Krogstrup, L. P. Kouwenhoven, G. De Lange, A. Kou, *Phys. Rev. Appl.* **2020**, *14*, 064038.

[13] K. Delfanazari, R. Puddy, P. Ma, T. Yi, M. Cao, Y. Gul, I. Farrer, D. Ritchie, H. Joyce, M. Kelly, C. Smith, *Adv. Mater.* **2017**, *29*, 1701836.

[14] K. Delfanazari, M. J. Kelly, C. G. Smith, R. K. Puddy, P. Ma, T. Yi, M. Cao, C. Richardson, I. Farrer, D. A. Ritchie, H. J. Joyce, M. J. Kelly, C. G. Smith, *IEEE Trans. Appl. Supercond.* **2018**, *28*, 1.

[15] K. Delfanazari, R. K. Puddy, P. Ma, T. Yi, M. Cao, Y. Gul, I. Farrer, D. A. Ritchie, H. J. Joyce, M. J. Kelly, C. G. Smith, *J. Magn. Magn. Mater.* **2017**, *459*, 282.

[16] A. Fornieri, A. M. Whiticar, F. Setiawan, E. Portolés, A. C. C. Drachmann, A. Keselman, S. Gronin, C. Thomas, T. Wang, R. Kallaher, G. C. Gardner, E. Berg, M. J. Manfra, A. Stern, C. M. Marcus, F. Nichele, *Nature* **2019**, *569*, 89.

[17] H. Ren, F. Pientka, S. Hart, A. T. Pierce, M. Kosowsky, L. Lunczer, R. Schlereth, B. Scharf, E. M. Hankiewicz, L. W. Molenkamp, B. I. Halperin, A. Yacoby, *Nature* **2019**, *569*, 93.

[18] W. Mayer, M. C. Dartiailh, J. Yuan, K. S. Wickramasinghe, E. Rossi, J. Shabani, *Nat. Commun.* **2020**, *11*, 212.

[19] K. Delfanazari, P. Ma, R. Puddy, T. Yi, M. Cao, Y. Gul, C. L. Richardson, I. Farrer, D. Ritchie, H. J. Joyce, M. J. Kelly, C. G. Smith, *J. Visualized Exp.* **2019**, *150*, 57818.

[20] L. Serra, K. Delfanazari, *Phys. Rev. B* **2020**, *101*, 115409.

[21] M. Hell, M. Leijnse, K. Flensberg, *Phys. Rev. Lett.* **2017**, *118*, 107701.

[22] F. Pientka, A. Keselman, E. Berg, A. Yacoby, A. Stern, B. I. Halperin, *Phys. Rev. X* **2017**, *7*, 021032.

[23] T. J. Thornton, M. Pepper, H. Ahmed, D. Andrews, G. J. Davies, *Phys. Rev. Lett.* **1986**, *56*, 1198.

[24] H. Z. Zheng, H. P. Wei, D. C. Tsui, G. Weimann, *Phys. Rev. B* **1986**, *34*, 5635.

[25] C. W. J. Beenakker, H. van Houten, *Solid State Phys.* **1991**, *44*, 1.

[26] C. Chen, I. Farrer, S. N. Holmes, F. Sfigakis, M. P. Fletcher, H. E. Beere, D. A. Ritchie, *J. Cryst. Growth* **2015**, *425*, 70.

2300453 (9 of 9)