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# Unintentional p-type conductivity in intrinsic Ge-rich SiGe/Ge heterostructures grown on Si(001)

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H. Tetzner,[1,a)] W. Seifert,[1] O. Skibitzki,[1] Y. Yamamoto,[1] M. Lisker,[1] M. M. Mirza,[2] I. A. Fischer,[3] D. J. Paul,[2] Monia De Seta,[4] and G. Capellini[1,4]

## AFFILIATIONS

[1]IHP-Leibniz-Institut für Innovative Mikroelektronik, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany
[2]James Watt School of Engineering, University of Glasgow, Rankine Building, Oakfield Avenue, Glasgow G12 8LT, United Kingdom
[3]Experimentalphysik und Funktionale Materialien, BTU Cottbus-Senftenberg, Erich-Weinert-Straße 1, 03046 Cottbus, Germany
[4]Dipartimento di Scienze, Università Roma Tre, Viale G. Marconi 446 Roma 00146, Italy

[a)]Author to whom correspondence should be addressed: tetzner@ihp-microelectronics.com

## ABSTRACT

In this work, we investigate the effective background charge density in intrinsic $Si_{0.06}Ge_{0.94}$/Ge plastically relaxed heterostructures deposited on Si(001). Hall effect measurements and capacitance–voltage profiling reveal a p-type conductivity in the nominally intrinsic layer with a hole concentration in the mid $10^{15}\,cm^{-3}$ range at temperatures between 50 and 200 K. In view of the carrier freeze out that we observe below 50 K, we attribute the origin of these carriers to the ionization of shallow acceptor-like defect states above the valence band. In addition, one dominant hole trap located at mid-gap position is found by deep level transient spectroscopy. Carrier trapping kinetics measurements can be interpreted as due to a combination of point defects, likely trapped in the strain field of extended defects, i.e., the threading dislocation.

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Ge-rich silicon-germanium (SiGe) heterostructures are promising candidates for a variety of optoelectronic and photonic applications.[1] The possibility to manufacture those using silicon (Si) CMOS-compatible materials and processes is an outstanding advantage. However, the large lattice and thermal mismatch between the Si substrate and Ge (4.2%) requires a careful strain management during the epitaxial growth.[2,3]

As an example, the n-type Ge/SiGe material system has been proposed as a potential candidate for the realization of a THz quantum cascade laser working at room temperature.[4–8] According to Ref. 9, these structures are extremely challenging to grow since the strain balancing conditions for the realization of the several $\mu$m-thick active layer have to be carefully controlled.[10,11] In addition to the effect of the lattice strain on the band alignment of the complex quantum cascade structures, the plastic relaxation via the insertion of extended defects in the reverse graded SiGe virtual substrate (RGVS) plays a major role in the device charge profile, which, in turn, strongly impacts its functioning.

It has often been observed that the existence of extended defects, such as misfit dislocations (MDs) and threading dislocations (TDs), generates an electrical charge background that can superimpose with the intentional doping in the device design, inducing a compensation or increase in the active carrier concentration.[8] Therefore, the actual background carrier concentration needs to be carefully evaluated in order to counteract this problem during fabrication and to correctly describe the device electrical landscape in simulations.[8,10]

Unfortunately, little is known about the background doping of intrinsic Ge-based heterostructures in the literature.[12–15] Although an initial p-type conduction or a transition from n-type to p-type conductivity is reported in plastically deformed Ge crystals,[12] Ge-rich SiGe-on-insulator structures,[14] $Si_{0.7}Ge_{0.3}$/Si heterostructures,[13] and GeSn films grown on Ge substrates,[15] its cause has still not been fully clarified yet. Generally, such p-type conduction is attributed to acceptor-like defect states introduced during plastic deformation and/or strain relaxation.[12–14]

To contribute shedding light on this issue, in this work, we comprehensively studied the active carrier concentration in as-grown intrinsic $Si_{0.06}Ge_{0.94}$/Ge/Si heterostructures. We have investigated this particular composition of the SiGe RGVS since it is of interest for the integration of strained-balanced n-Ge/SiGe superlattices on Si.[16] The heterostructure has been investigated by means of three complementary characterization techniques: Hall effect measurements have been


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employed to investigate the transport dynamics due to the defect-originated doping, while capacitance–voltage (C–V) profiling and deep level transient spectroscopy (DLTS) have been employed to investigate the charge distribution and the capture/release dynamics, respectively.

The $Si_{0.06}Ge_{0.94}$/Ge heterostructures were grown on 200 mm Si(001) substrates by reduced pressure chemical vapor deposition (RP-CVD) using an industry-grade ASM Epsilon 2000 reactor at a pressure of 80 Torr. The Ge buffer growth comprises a Ge seed layer of 100 nm thickness grown at 350 °C using a germane-nitrogen gas mixture followed by a fully relaxed Ge layer of 1.2 $\mu$m at a temperature of 550 °C. Subsequently, the intrinsic $Si_{0.06}Ge_{0.94}$ layer was deposited at 550 °C using silane and germane as reactant gases. Further details on the growth procedure can be found in Ref. 16. The $Si_{0.06}Ge_{0.94}$ epilayers feature a threading dislocation density (TDD) of $2 \times 10^7$ cm$^{-2}$ measured by Secco etch pit count.[16]

We have realized three samples (see Fig. 1). In the two samples, dedicated to Hall measurements, 1.2 and 2 $\mu$m thick $Si_{0.06}Ge_{0.94}$ epilayers were grown on a VS featuring 200 nm thick n-doped layers ($1 \times 10^{17}$ cm$^{-3}$) of Si and Ge, which were introduced by phosphine co-doping during the growth on top of the Si substrate and the Ge buffer, respectively. As discussed in the following, these layers allow us to electrically separate the virtual substrate from the intrinsic $Si_{0.06}Ge_{0.94}$ epilayer of interest for this study. To avoid auto-doping in the subsequent intrinsic epilayers, the wafer is unloaded from the RP-CVD reactor, which undergoes a wet cleaning process. The other sample, dedicated to C-V measurements, is made of an intrinsic 1.5 $\mu$m thick $Si_{0.06}Ge_{0.94}$ layer grown on an intrinsic VS.

Hall bars were fabricated on the $Si_{0.06}Ge_{0.94}$/Ge heterostructures as schematically shown in Fig. 1(a). The six-terminal bars, 100 $\mu$m wide and 1000 $\mu$m long, were fabricated by aluminum (Al) deposition followed by a contact annealing step using rapid thermal processing (RTP) at 350 °C for 30 s. Subsequently, the surrounding $Si_{0.06}Ge_{0.94}$ material was etched by inductively coupled plasma (ICP) mesa-etching.[17] Hall effect measurements were performed with a Lakeshore 7700A series Hall system in a temperature range between 20 and 300 K and a maximum magnetic field of 1.5 T.

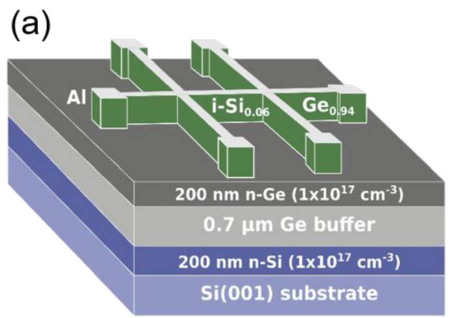
Metal-oxide-semiconductor (MOS) capacitors were fabricated by depositing a 60 nm-thick silicon dioxide ($SiO_2$) layer on top of the heterostructures by high density plasma-CVD at 300 °C using an Applied Materials Centura cluster tool [see Fig. 1(b)]. The oxide thickness was selected to serve as an effective barrier for possible leakage currents through the $SiO_2$. As a gate contact, a 500 nm thick Al layer was sputtered at 2 kW on top of the gate dielectric. The wafer backside Ohmic contacts were formed by an indium-gallium (InGa) eutectic. The use of a low resistivity Si substrate ($\rho = 0.008$–$0.012\ \Omega$ cm) allows to minimize the series resistance $R_S$ in the MOS structure.

Capacitance–voltage (C–V) and deep-level-transient spectroscopy (DLTS) measurements were performed at temperatures ranging from 50 to 300 K in a Janis closed-cycled helium cryostat connected with a PhysTech FT 1230 system working at 1 MHz test frequency on diodes having an area of $8.2 \times 10^{-3}$ cm$^2$. The MOS devices were measured from top to bottom as indicated in Fig. 1(b). In all measurements, the voltage was applied to the top gate contact.

In Fig. 2, we show the temperature dependent carrier density and carrier mobility extracted from Hall measurements for both investigated samples, featuring $Si_{0.06}Ge_{0.94}$ layer thicknesses of 1.2 and 2.0 $\mu$m. A sheet hole density ranging between $5 \times 10^{11}$ and $1 \times 10^{12}$ cm$^{-2}$ is observed for both samples in the temperature range of 50–250 K. Such residual p-type conductivity is in line with previously observed results on similar Ge-rich SiGe layers[13,14] as well as in GeSn films grown on Ge substrates[15,18] and plastically deformed Ge bulk materials.[12]

The drop in sheet carrier density below 50 K [see Fig. 2(a)] is associated with the freeze out of charge carriers in the heterostructure. A carrier freeze out at this temperature points toward the existence of shallow acceptor levels above the valence band edge that could be responsible for the observed p-type conductivity. In consequence of the hetero-integration on Si and the absence of any dopants, the included TDs can be a reasonable source of the shallow acceptor-like defect states. As reported in the literature, as-grown dislocations and dislocation networks introduced by plastic deformation are assigned to shallow one dimensional energy bands split off from the valence and conduction band in bulk Ge.[19–21] Above 250 K, the carrier density is dominated by the contribution of electrons in the n-doped Ge layer [see Fig. 1(a)] indicated by the change in sign of the Hall voltage and, consequently, of the Hall coefficient. Their contribution to the transport is probably caused by leakage in the p-n junction underneath induced by TDs.[22]

Possible explanations for the slight difference observed in the sheet carrier density of the two measured samples are either a remaining contribution from the VS underneath or a non-uniform carrier distribution depending on the thickness of the intrinsic $Si_{0.06}Ge_{0.94}$ film. To isolate the contribution of the intrinsic $Si_{0.06}Ge_{0.94}$ layer by excluding the regions closer to the relaxed SiGe/Ge heterojunction, we assume that the thicker 2.0 $\mu$m i-$Si_{0.06}Ge_{0.94}$ behaves as the linear combination of the 1.2 $\mu$m thick sample plus an additional 0.8 $\mu$m of i-$Si_{0.06}Ge_{0.94}$ material. By taking into account the difference in thickness t = 0.8 $\mu$m of the probed region and the difference in sheet carrier



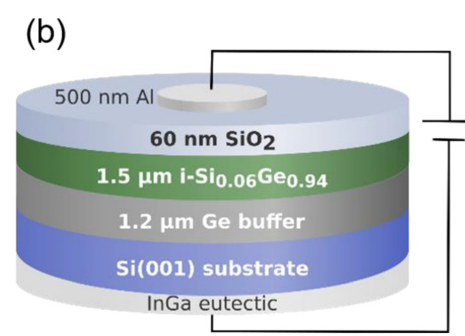




**FIG. 1.** Sketch of the fabricated (a) Hall bar devices and (b) MOS capacitors.

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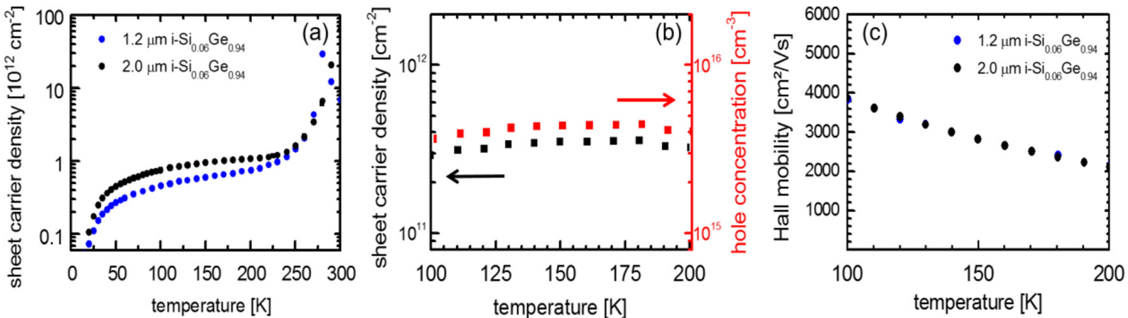



**FIG. 2.** Temperature dependent (a) sheet carrier density measured by Hall for 1.2 and 2.0 $\mu$m thick $Si_{0.06}Ge_{0.94}$ layers, (b) the difference in sheet carrier density and corresponding hole concentration, and (c) Hall mobility of both samples.

density $N_S$ measured between the two samples, we can evaluate the average hole density for the upper 0.8 $\mu$m of the 2.0 $\mu$m thick i-$Si_{0.06}Ge_{0.94}$ sample through the relationship $N_S = \frac{N}{t}$. We obtain a hole density of $N \sim 4 \times 10^{15}$ cm$^{-3}$ in the whole temperature range considered [Fig. 2(b)].

Independently of the slight difference in carrier density, we notice a similar Hall mobility ranging between 2000 and 4000 cm$^2$/V s in both samples in the considered temperature regime [Fig. 2(c)].

We now discuss the results of the C–V analysis. By probing MOS capacitors, we are able to investigate the charge distribution profile along the growth direction of the $Si_{0.06}Ge_{0.94}$/Ge/Si heterostructure.

Measured C–V curves in Fig. 3(a) feature an oxide capacitance $C_{ox} = 470$ pF that corresponds to an oxide thickness $d_{ox}$ of 60.25 nm estimated by $d_{ox} = \varepsilon_0\varepsilon_r A/C_{ox}$, where A is the gate area, $\varepsilon_0$ is the vacuum, and $\varepsilon_r$ is the relative permittivity of the $SiO_2$ ($\varepsilon_r = 3.9$). The estimated $d_{ox}$ is in very good agreement with the targeted thickness of 60 nm during fabrication. The accumulation observed at negative gate voltages implies a p-type conductivity of the intrinsic $Si_{0.06}Ge_{0.94}$ layer, in agreement with the results obtained by Hall effect measurements.

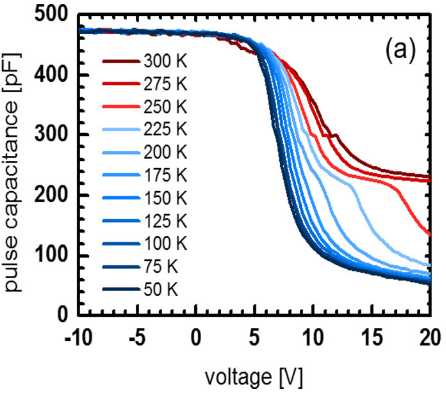
In order to ensure the deep depletion condition in the MOS capacitors during the C–V measurements, a pulse capacitance is measured instead of a high-frequency capacitance.[23] Here, at each measurement point, the MOS capacitor is first held in accumulation and then pulsed to the certain reverse bias values for 100 $\mu$s to measure the deep depletion capacitance. However, the signal shoulder observed in the C–V characteristic for $V > 10$ V at $T > 200$ K [Fig. 3(a)] evidences a deviation from the deep depletion condition. Minority carriers have had enough time to be generated inside the $Si_{0.06}Ge_{0.94}$/Ge heterostructure within the voltage pulses at elevated temperatures but are suppressed at lower temperatures since the time constant of minority carrier emission increases with decreasing temperature.[23–25] Consequently, we limit ourselves to evaluate the carrier concentration in the 50–200 K temperature range.

In Fig. 3(b), we show the potential-dependent depletion width $x_d = \varepsilon_0\varepsilon_r A/C_{sc}$, where $C_{SC}$ is the semiconductor capacitance and $\varepsilon_r = 15.93$ is the relative permittivity for the $Si_{0.06}Ge_{0.94}$ layer estimated by using the Vegard's law. Here, the information depth extends from the oxide-semiconductor interface into the $Si_{0.06}Ge_{0.94}$/Ge heterostructure. Hence, we can provide information on residual carrier concentrations through the entire $Si_{0.06}Ge_{0.94}$ layer and in the first 0.5 $\mu$m of the Ge buffer by applying a maximum reverse bias of 20 V.

The carrier density profiles at temperatures below 200 K are calculated from the slope of a 1/C$^2$-V plot.[23] Here, the depletion dependent majority carrier concentration $N(x_d)$ of the MOS capacitor is estimated by

$$N(x_d) = \frac{2}{q\varepsilon_0\varepsilon_S A^2 d(1/C2)/dV} \quad (1)$$

where q is the elemental charge. The corresponding temperature dependent majority carrier densities as a function of depletion width are shown in Fig. 4(a). The increase in carrier concentration at the top surface region ($0 < x_d < 300$ nm) will be neglected based on the Debye length limitation, resulting in errors in pulsed capacitance



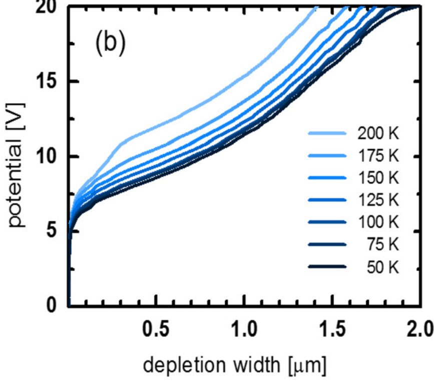




**FIG. 3.** (a) Temperature dependent pulse C–V characteristics and (b) corresponding information depth depending on the applied potential.

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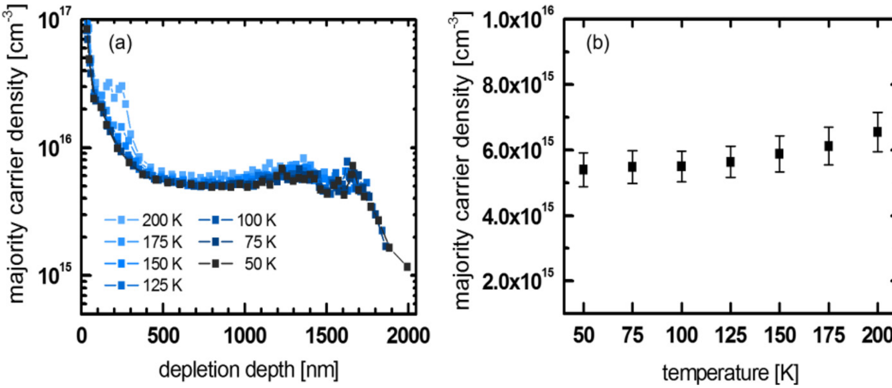


FIG. 4. Temperature dependent (a) effective carrier concentration profile in the $Si_{0.06}Ge_{0.94}$/Ge heterostructure and (b) majority carrier density in the $Si_{0.06}Ge_{0.94}$ layer.

doping density determinations in MOS capacitors.[23] However, from Eq. (1), we can extract a majority carrier density in the nominal intrinsic $Si_{0.06}Ge_{0.94}$ of $\sim 5 \times 10^{15}$ cm$^{-3}$. This value is in very good agreement with the average hole density of $\sim 4.2 \times 10^{15}$ cm$^{-3}$ derived by Hall effect measurements. Again, we observe an almost constant ($5–6 \times 10^{15}$ cm$^{-3}$) carrier density in the $Si_{0.06}Ge_{0.94}$ layer in a temperature regime between 50 and 200 K as shown in Fig. 4(b), suggesting a full occupation of acceptor-like states. For $T < 100$ K, it becomes possible to additionally extend the space charge region into the equally intrinsic Ge buffer layer. Here, the carrier concentration decreases down to $1 \times 10^{15}$ cm$^{-3}$ after overcoming the defective $Si_{0.06}Ge_{0.94}$/Ge heterointerface at a depth of 1.5 $\mu$m.

Additionally, we probe the defect states inside the $Si_{0.04}Ge_{0.96}$/Ge heterostructure by DLTS that can also contribute to the observed p-type conductivity.[26]

In this study, a reverse voltage $V_R = 20$ V and a filling pulse voltage $V_P = 0$ V were applied at the gate to drive the MOS capacitor from depletion into accumulation for a duration of $t_p = 100$ $\mu$s. As already commented, for this bias condition, the space charge region extends from the oxide interface up to a maximum of 2 $\mu$m into the $Si_{0.04}Ge_{0.96}$/Ge heterostack [see Fig. 3(b)]. The capacitance transient was recorded with a period width $T_w = 51.2$ ms.

One dominant hole trap is found in the spectra of Fig. 5(a). The axis of ordinates represents the first sine coefficient b1 of the Fourier transform of the measured capacitance transient, which is an equivalent to the standard DLTS rate window.[23] The peak at $T = 225$ K is associated with a bulk trap with a thermal activation energy of $E_T = 0.325$ eV above the valence band $E_V$ estimated by an Arrhenius plot. The corresponding hole capture cross section is calculated to be $\sigma = 8.69 \times 10^{-17}$ cm$^2$, which is in the same order of deep levels found in other Ge/Si heterostructures.[27,28]

Assuming a similar bandgap for the $Si_{0.06}Ge_{0.94}$ layer and Ge (0.67 eV), the observed defect level is located at mid-gap position and, therefore, can act as an attractive trapping center for free carriers and/or effective generation-recombination (G-R) center. This will impact the active carrier concentration as well as the transport mechanisms in the final devices built using similar Ge-rich SiGe/Ge heterostructures and should be taken into consideration during fabrication and simulation.

Moreover, the carrier trapping kinetics were recorded in order to distinguish between point and extended defects as origin of the observed defect state.[18] The effect of filling pulse time $t_p$ on hole trapping at the peak temperature [$T = 225$ K in Fig. 5(a)] is displayed in Fig. 5(b). The continuous trapping of carriers up to 10 $\mu$s is typical of single localized point defects, which can be filled only up to their complete occupation.[18,29] However, the subsequent b1 signal increases when longer filling pulses are applied. Such logarithmic trap filling is characteristic for extended defects like TDs, as the responsible band-like states mutually affect the carrier trapping by creating a Coulombic potential barrier.[18,29]

As reported by Schröter *et al.*,[30] defect states associated with dislocations can be localized when interacting with point defects or of

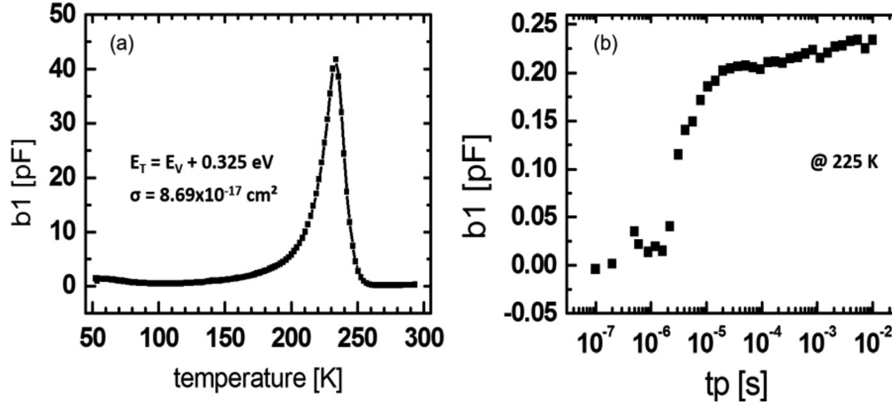


FIG. 5. (a) DLTS temperature scan and (b) isothermal DLTS measurements at 225 K. The axis of ordinates represents the first sine coefficient b1 of the Fourier transform of the measured capacitance transient.

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band-like character if the dislocations are clean (not decorated with other defects). Threading dislocations occurring during plastic relaxation in Ge/Si heterostructures give rise to deep defect states inside the Ge bandgap.[27,28] Such deep defect states may indicate an impurity decoration along the dislocation line or point defect clusters left behind dislocation movement.[27] Two hole traps at $E_V + 0.156\,eV$ and $E_V + 0.183\,eV$ have been ascribed to TDs in Ge/Si photodiodes,[28] one hole trap located at $E_V + 0.15\,eV$ has been observed in strained $Ge_{0.93}Sn_{0.07}$/Ge/Si heterostructures where it has been attributed to clean TDs based on the sole logarithmic trap filling,[18] and acceptor states located at $E_C$ - 0.33–0.4 eV have been found in Ge junctions selectively grown on STI Si substrates.[27] Accordingly, we correlate the observed acceptor-type bulk defects at $E_V + 0.325\,eV$ with native point defects introduced during epitaxial growth of the $Si_{0.06}Ge_{0.94}$/Ge heterostructure that accumulates in the long range strain field around TDs (Cottrell atmosphere[31]).[14,27,30–32] One origin for these point defects can be vacancies, since they create acceptor states in Ge crystals and can easily form during the epitaxial growth.[12]

In conclusion, we investigated the effective carrier concentration in intrinsic $Si_{0.06}Ge_{0.94}$/Ge heterostructures integrated on Si(001). By using the differential Hall approach, we found an effective hole concentration of $4–5 \times 10^{15}\,cm^{-3}$ in the $Si_{0.06}Ge_{0.94}$ epilayer in a temperature regime between 100 and 200 K. A corresponding hole mobility of $2800\,cm^2/V\,s$ was extracted at 150 K. By C–V measurements at MOS capacitors, it became possible to probe the carrier concentration along the growth direction of the whole $Si_{0.06}Ge_{0.94}$/Ge heterostructure, with the exclusion of a near surface region. For $50 < T < 200\,K$, we observed a background hole concentration of $5–6 \times 10^{15}\,cm^{-3}$ in the $Si_{0.06}Ge_{0.94}$ layer and of $1 \times 10^{15}\,cm^{-3}$ in the Ge buffer underneath. A carrier freeze out below 50 K obtained by Hall effect measurements implied shallow acceptor-like states possibly responsible for the unintentional p-type doping that we attribute to the presence of dislocation in the Ge/Si heterostructure. One dominant hole trap is found at midgap position ($E_V + 0.325\,eV$) using DLTS. Based on our results on hole trapping kinetics, we associate this acceptor-like defect level with point defects that are trapped in the strain field around threading dislocations.

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## AUTHOR DECLARATIONS

### Conflict of Interest

The authors have no conflicts to disclose.

### Author Contributions

**Henriette Tetzner:** Conceptualization (lead); Formal analysis (equal); Investigation (equal); Visualization (lead); Writing – original draft (lead). **Giovanni Capellini:** Conceptualization (equal); Project administration (equal); Supervision (lead); Writing – original draft (equal); Writing – review & editing (lead). **Winfried Seifert:** Data curation (equal); Formal analysis (equal); Investigation (equal). **Oliver Skibitzki:** Methodology (equal); Writing – review & editing (equal). **Yuji Yamamoto:** Methodology (equal); Writing – review & editing (equal). **Marco Lisker:** Methodology (equal); Writing – review & editing (equal). **Muhammad Mirza:** Methodology (equal); Writing – review & editing (equal). **Inga Anita Fischer:** Formal analysis (equal); Supervision (lead); Writing – review & editing (lead). **Douglas J. Paul:** Methodology (equal); Project administration (equal); Writing – review & editing (equal). **Monica De Seta:** Funding acquisition (lead); Project administration (lead); Writing – review & editing (equal).

## DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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