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Effect of passivation on selectively grown sub-μm Ge-on-Si single photon avalanche diode detectors

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***Abstract*—Ge-on-SOI (silicon-on-insulator) single photon avalanche diodes (SPADs) have been fabricated with exposed sidewalls allowing variation of passivation techniques. Reduced dark currents and density of surface states are demonstrated with thermal oxide passivation, demonstrating the benefit of optimal passivation of low aspect ratio selectively grown Ge.**

***Index Terms*—germanium-on-silicon, single photon avalanche diode detector, passivation, selectively grown**

I. Introduction

Recently there has been increasing interest in developing single photon detectors operating in short-wave infrared (SWIR) wavelengths [1], defined as operating beyond the band edge of Si of about 1000 nm. Numerous quantum technology applications such as light detection and ranging (LIDAR) [2], imaging through obscurants [3] and quantum communications [1] require such single photon sensitivity at these wavelengths. For example, LIDAR applications improvements can be made by moving to the SWIR due to lower solar background radiation and increased laser safety eye thresholds. In quantum communications, low loss optical fibre wavelengths of 1310 nm and 1550 nm require any single photon detector to detect at these wavelengths. While superconducting nanowire detectors [4] and InGaAS/InP SPADs [5] are readily available single photon detection technologies, Ge-on-Si SPADs offer potential for lower afterpulsing and high single photon detection efficiencies. [6]

In this study, Ge-on-Si SPADs are fabricated on 260 nm silicon-on-insulator (SOI) wafers, with a separate absorption, charge and multiplication layer geometry (SACM) and with a lateral Si multiplication layer, in a fully CMOS compatible process. With this geometry, integration with Si waveguides and optical fibres can be readily achieved [7], realising its potential for quantum communications applications. The Ge is selectively grown inside SiO_2 trenches, reducing the threading dislocation density (TDD) in comparison with bulk Ge growths. Dark current characteristics of these devices are investigated, as are the effect of different Ge passivation techniques on the sidewalls.

II. Design and Fabrication

The SOI substrate consisted of 150 mm diameter wafers with a 260 nm lightly doped p-Si (100) top layer, followed by a 2 μm SiO_2 layer, followed by a lightly doped p-Si substrate.

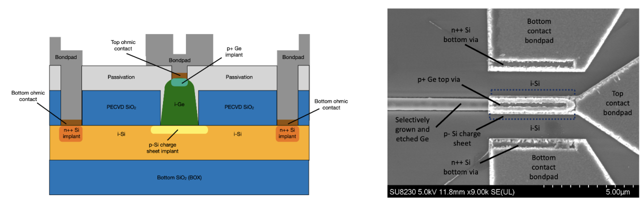

Fig. 1. Schematic and SEM image of selectively grown Ge-on-Si SPAD.

The top Si was selectively implanted with As and BF_2 to form the n^{++} contacts and charge sheet layer respectively. After dopant activation, PECVD SiO_2 was deposited on top, followed by dry etching down to the top Si layer. Ge was selectively grown in this region, overflowing from the top SiO_2 layer before being etched back. The etch back was performed as distinct from a chemical mechanical polishing (CMP) process to expose and allow passivation of the Ge sidewalls. Ensuing implantation and activation of the Ge with boron for the top contact, the Ge was passivated, either with thermal oxidation, a PECVD Si_3N_4 deposition and anneal or with a simple PECVD SiO_2 deposition without any thermal oxidation. Vias were etched and metal contacts were defined on the implanted n^{++} regions in Si and p^+ region in Ge. Finally, bond pads were defined to allow electrical bias. Figure 1 shows the completed device, and the size of the Ge was 0.8 μm x 5 μm, with an i-Si lateral multiplication region width of 1.5 μm.

III. Results

Dark current-voltage (IV) measurements of the SPADs were conducted on a Lakeshore Cryotronics cryogenic probe station, using a Keysight B1500a semiconductor parameter analyser. Figure 2 shows the IV comparison of two passivation techniques, one with thermal oxidation followed by 200 nm PECVD Si_3N_4 deposition and anneal and the other with no thermal oxidation and 200 nm PECVD SiO_2 deposition. For thermal oxidation, a sharp breakdown in current is observed at 45-50 V caused by the breakdown in the Si multiplication region. With no thermal oxidation and SiO_2 deposition, a shallower breakdown is present, preceded by a large rise in current at 30 V. This rise is due to the increased presence of traps on the Ge surface when the oxidation is not performed, leading to a greater number of surface recombination sites by which electron hole pairs may recombine.

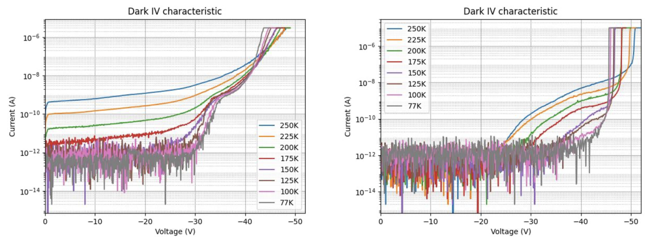

Fig. 2. Temperature dependent IVs on Ge-on-Si SPADs passivated with PECVD SiO_2 (left) and thermal oxidation and PECVD Si_3N_4 (right).

Photoresponse measurements show punch-through at 10 V reverse bias (figure 3 (left)) , and the activation energy was extracted from the dark IV measurements via Shockley-Read-Hall (SRH) mechanisms of trap recombination (figure 3 (right)). The extracted activation energy for both passivations are shown, as a function of the voltage below the breakdown voltage (V_{bd}) of the device at that particular temperature. The activation energy remains below $E_g/2$ of Ge (0.33 eV) consistently before V_{bd}, indicating a form of trap-assisted-tunnelling (TAT) mechanism. At less than 7.5 V before V_{bd} however, thermally passivated SPADs remain at 0.15 eV, while non-thermally passivated SPADs decline in activation energy towards breakdown, indicating an increase in recombination with higher electric field. This highlights further the effect of higher surface trap states on device IV performance, leading to a higher degree of TAT within the surface traps.

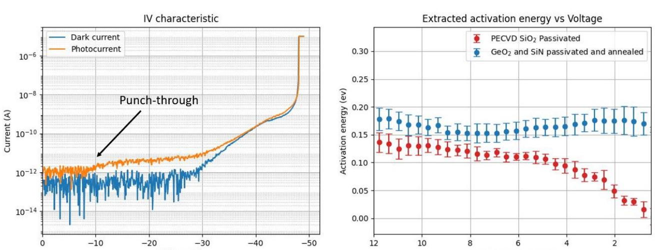

Fig. 3. Photocurrent and dark current comparison at 175K (left) and extracted activation energy dark IVs between 250 K and 175 K assuming Shockley Read Hall recombination for both passivation techniques (right).

Capacitors on Ge substrates were fabricated with the aforementioned passivation to extract the density of interface trap densities D_{it}. By analysing capacitance-voltage (CV) and conductance-voltage (GV) characteristics as a function of temperature, D_{it} versus bandgap energy from the valence band were extracted via the conductance method. Figure 4 shows the calculated D_{it} values for both passivation techniques, presenting the reduction in surface trap states when thermal oxidation is performed, and thermal passivation showing similarity with previously reported Germanium oxide passivation. [8]

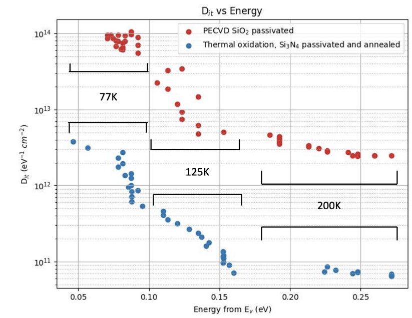

Fig. 4. D_{it} values for both passivation techniques calculated from CV and GV measurements at 77 K, 125 K and 200 K.

IV. Conclusions

Selectively-grown Ge-on-SOI SPADs were fabricated with exposed Ge sidewalls allowing for passivation characterisation. IV measurements were performed as a function of temperature and passivation technique, and activation energies were extracted assuming Shockley-Read-Hall recombination. These devices exhibited superior device IV performance when thermally passivated relative to PECVD SiO_2. CV and GV measurements of Ge capacitors of the same passivation techniques indicates dramatically lower D_{it} values when thermally oxidised, supporting the hypothesis that reduced surface traps will lower dark current and improve device performance. Future work will seek to identify the dependency on dark count rate (DCR), single photon detection efficiency (SPDE), and optimising charge sheet parameters.

Acknowledgments

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