Breakdown Mechanisms Limiting the Operation of Double Doped PHEMTs Scaled into sub-100 nm Dimensions

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The breakdown limit of pseudomorphic high electron mobility transistors (PHEMTs) with double delta-doping structure scaled down into sub-100 nm dimensions is extensively investigated by Monte Carlo device simulations. The two mechanisms responsible for breakdown are channel impact ionization and tunnelling from the gate. The double doped PHEMTs may have two possible placements of the second delta doping layer: either below the channel or between the gate and the first delta doping layer. Quantum mechanical tunnelling starts at very low drain voltages but quickly saturates, having a greater effect on those PHEMTs with the second doping layer placed above the original doping. The threshold for impact ionization occurs at larger drain voltages which should assure the reliable operation voltage scale of double doped PHEMTs. Those double doped PHEMTs with the second delta doping layer placed below the channel deteriorate faster with the reduction of the channel length due to impact ionization than those devices with the second doping layer above the original doping.

l. Introduction

The performance of pseudomorphic high electron mobility transistors (PHEMTs) with low indium content channel can be steadily improved when these devices are scaled into deep sub-100 nm dimensions. To benefit from the improvement a full scaling approach has to be employed in which the devices are scaled down in both lateral and vertical dimensions in respect to gate lengths of 120, 70, 50, and 30 nm [1,2]. If the scaling is applied only in the lateral PHEMT dimensions then the performance of the sub-100 nm gate length devices deteriorates [1,3,4]. However, the carrier density in the channel drops because of the reduction of the gate-to-channel distance in the proportional scaling process. The reduction in the carrier density, which affects the power handling capability of the devices, may be compensated for when an additional delta doping layer is placed into the PHEMT structure [5] in order to increase the drive current. If the second delta doping layer is placed below the channel, the transconductance peak broadens resulting in large improvement in the device linearity, although the maximum transconductances remain close to the corresponding values in single delta doped devices [6]. If the second delta doping layer is placed above the original delta doping, near to the gate, the maximum transconductance increases by up to 80% for the 70 nm device as shown in Fig. 1. This effect is however reduced when the PHEMT is scaled to 50 nm and below [6]. The reduction of the gate to channel separation in the proportional scaling increases the probability of electron tunnelling from the gate, which may trigger breakdown. Also because the carrier density in the channel substantially increases with additional delta doping the device becomes more sensitive to channel impact ionization. In this work we have investigated two concurrent breakdown mechanisms; channel impact ionization which

first occurs around the gate corner on the drain side of the channel due to a fringing electric field [7] and gate tunnelling which causes gate current leakage and may itself trigger avalanche breakdown [8].

2. Monte Carlo device simulator

The study has been carried out with our Monte Carlo (MC) device simulator MC/H2F [1]. The device simulator has been carefully calibrated against a 120 nm gate length PHEMT fabricated at University of Glasgow. The typical PHEMT under investigation has a T-shape gate; a 30 nm heavily doped (4×10¹⁸ cm⁻³)

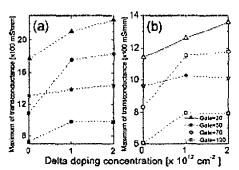


Figure 1: Maximum of transconductance as a function of the delta doping concentration in the second doping layer placed above the channel for intrinsic devices (a) and with external resistance included (b). The zero concentration refers to the single doped structure.

n+ GaAs cap; an Al_{0.3} Ga_{0.7}As etchstop; a 7×10¹² cm⁻² Si delta doping; an Al_{0.3} Ga_{0.7}As spacer and a 10 nm In_{0.2}Ga_{0.8}As channel. The whole device structure is grown on top of a 50 nm thick GaAs buffer. To compare the simulated intrinsic device I-V characteristics with experimental data, the effect of external resistances is included at a post-processing stage [9].

Impact ionization is included in the device simulator MC/H2F as an additional scattering mechanism. Let assume that impact ionization starts at a threshold energy E_{th} then the electron scattering rate reads [10]

$$\Gamma(E) = P \left[\left(E - E_{th} \right) / E_{th} \right]^{A} \tag{1}$$

where P and A are parameters which must be fitted to experimental data. We have used A=4 for GaAs suggested in Ref. 10 and A=14 for $\ln_{0.53}Ga_{0.47}As$ which is more difficult to simulate at a very high electric field. Bulk simulations of the impact ionization coefficient can satisfactorily reproduce measured data for GaAs and $\ln_{0.53}Ga_{0.47}As$ in the range of electric fields of interest [11] Since hole dynamics and the corresponding bipolar effects are not included in the H2F/MC, the experimentally observed increase in the drain current at breakdown cannot be reproduced. Instead, we calculate the impact ionization assisted increase in the electron current of the devices. This allows us to define the bias conditions corresponding to the onset of impact ionization which is determined only by the electron dynamics.

Thermionic tunnelling is incorporated into the MC/H2F as an additional simulation procedure during each time step and proceeds as follows: a number of particles (representing the electron density in the metal) is obtained after integration over the Fermi-Dirac distribution. An energy at which the particle may tunnel into the device is randomly selected from the Fermi-Dirac distribution. The tunnelling probability, T, is calculated from the WKB approximation [12] as

$$T(E) = \exp\left\{-2\frac{\sqrt{2m}}{\hbar} \int_{0}^{w} [V(x) - E]^{1/2} dx\right\},\tag{2}$$

where m is the electron effective mass in the device; w is the path along which the electron should tunnel through and V(x) is the potential. This probability is used in a standard rejection technique to accept or reject the tunnelling event. This process is repeated for each particle

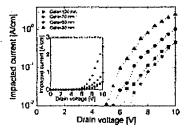


Figure 2: Impact ionization assisted drain current versus the drain voltage at V_G=-1.0 V for double doped scaled PHEMTs with the second delta doping layer below the channel.

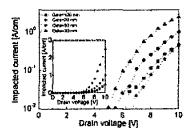


Figure 3: Impact ionization assisted drain current versus the drain voltage at V_C=-1.0 V for double doped scaled PHEMTs with the second delta doping layer above the original doping.

and at each mesh cell around the gate. The number of tunnelling particles is then used to calculate the gate tunnelling current.

4. Impact ionization assisted and tunnelling currents

The corresponding threshold drain voltage for both breakdown mechanisms is calculated from the number, N, of impacted or, respectively, tunnelled particles during the simulation time, t, as

$$I_D^{assist} = N e_s / t, (3)$$

where e_S is the superparticle charge. These assisted drain currents are examined in double doped scaled PHEMTs with the two placements of the second delta doping layer. Figs. 2 and 3 show the impact ionization assisted drain current as a function of the drain voltage at a gate bias of -1.0 V. Impact ionization quickly starts to increase the drain current which could lead to complete device breakdown. Figs. 4 and 5 show the thermionic tunnelling assisted gate current versus drain voltage at the same gate bias. The current due to thermionic tunnelling has a different drain voltage dependence compared to the impact ionisation current, increasing relatively sharply at lower drain voltages [13] but then saturates at larger drain voltages. The thresholds for both impact ionization and thermionic tunnelling decrease with device scaling. The threshold for the impact ionization assisted drain current in Fig. 3 starts at slightly lower drain voltages compared to the single doped devices. This is due to the screening of the gate fringing fields in the channel by second delta doping at the drain corner. This is also supported by the fact that the threshold of the impact ionization assisted drain current in Fig. 2 is larger than those in Fig. 3. Figs. 4 and 5 show that although the thermionic tunnelling assisted gate current starts at a very low drain voltage, it rapidly saturates at large drain voltages even for devices with very small gate-to-channel separation. Therefore it should not be of great concern for the scaling process. The gate tunnelling current in Fig. 4 also increases with scaling while the current in Fig. 5 remains practically constant in the 70, 50 and 30 nm double doped PHEMTs with the second delta doping layer placed below the channel.

5. Conclusion

Using MC device simulations we have evaluated two possible breakdown mechanisms, channel impact ionization and gate thermionic tunnelling. Two placements of the second delta doping layer in the double doped PHEMTs have been considered following our previous work on PHEMT scaling [6]. When the second delta doping layer is placed above the original delta doping, near to the gate, the device exhibits an improvement in transconductance compared to

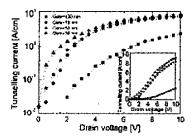


Figure 4: Thermionic tunnelling assisted gate current versus the drain voltage at V_G=-1.0 V for double doped scaled PHEMTs with the second delta doping layer below the channel.

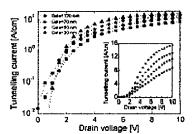


Figure 5: Thermionic tunnelling assisted gate current versus the drain voltage at V_G=1.0 V for double doped scaled PHEMTs with the second delta doping layer above the original doping.

the respective single doped PHEMTs. Nevertheless, this type of the design has larger leakage due to gate tunnelling. The effect of impact ionization is slightly smaller than in the other type of the double doped design. When the second delta doping layer is placed below the channel, device transconductance slightly deteriorates but the device linearity substantially improves [6]. This placement of the second delta doping does not affect the thermionic tunnelling assisted gate current which remains virtually the same as for the single doped PHEMTs. This double doped design causes a small increase in the impact ionization assisted drain current due to the higher electric fringing field compared to the former design. However, impact ionization always increases so dramatically that the crucial task in PHEMT design is to make the impact ionization threshold as high as possible.

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