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The Impact of Random Doping Effects on CMOS SRAM Cell

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Abstract:

SRAM has very constrained cell area and is consequently sensitive to the intrinsic parameter fluctuations ubiquitous in decananometer scale MOSFETs. Using a statistical circuit simulation methodology which can fully collate intrinsic parameter fluctuation information into compact model sets, the impact of random device doping on 6-T SRAM static noise margins, read and write characteristics are investigated in detail for well-scaled 35 nm physical gate length devices. We conclude that intrinsic parameter fluctuations will become a major limitation to further conventional MOSFET SRAM scaling.

1. Introduction

Integrated memory is crucial to modern System on Chip (SoC) design. It is claimed that 80% of an SoC die area will be occupied by memory in 2008, and therefore memory implementation and scaling will become increasingly important in high performance SoC design. There are several types of memory element available for SoC applications, with 6-T SRAM the safest in respect to noise margin and process compatibility. As such, it is often found in integrated systems such as high performance processors [1].

In order to achieve high integration density, SRAM has a constrained area, and minimum width/length ratio devices are normal in SRAM cell design. However the magnitude of intrinsic parameter fluctuations between macroscopically identical devices caused by the underlying granularity of matter steadily increases as device dimensions shrink. It will become the main source of device mismatch in the decanano regime [2], and is exacerbated at small width/length ratios. New generations of SRAM will inevitably be sensitive to such atomic-level fluctuations.

The stability of an SRAM cell can be expressed through the static-noise margin (SNM), defined as the minimum dc noise voltage needed to flip the cell state. SNM optimisation is a matter of major concern in memory cell design, and considerable efforts – both analytic and through device simulation – have been made to investigate the impact of intrinsic parameter fluctuations on SNM performance [3-4]. However, these studies have been limited to the effects of threshold voltage mismatch, whilst device characteristic variations caused by intrinsic parameter fluctuations are more complex. For example, the granularity of MOSFET channel doping will be important in sub-threshold, but less unimportant in saturation due to increased screening. It is impossible to fully map circuit behaviour by considering the mismatch of a single device parameter. Therefore it is critical to assess the impact of intrinsic parameter fluctuations on realistic device characteristics.

In this work, based on a well-scaled 35 nm gate length technology with 1.2 V supply voltage [5], a statistical circuit simulation methodology [6] is used to assess the impact of random doping effects on SRAM. In section 2, the simulation methodology is briefly described. Section 3, the impact of such intrinsic parameter fluctuations on the SNMs of different SRAM cells is discussed in detail. In section 4, the impact of random doping on SRAM read/write performance is investigated. Conclusions are drawn in section 5.

2. Simulation methodology

Fig. 1 illustrates potential variations due to random dopant positions in channel, source and drain of the 35 nm MOSFET which corresponds to advanced 90nm technology node, and the corresponding spread in the device characteristics obtained using comprehensive 3D 'atomistic' simulations. A two-stage statistical compact model parameter extraction procedure [6] is employed to transform all the device fluctuation information obtained from above 3D 'atomistic' simulations into a representative set of BSIM3v3 compact models. Seven key BSIM3v3 parameters are chosen to map random doping effects based on physical insight, the set may not be completely orthogonal when applied to a particular device, as shown in fig.2. It does however form an adequate basis set for statistical compact modelling.

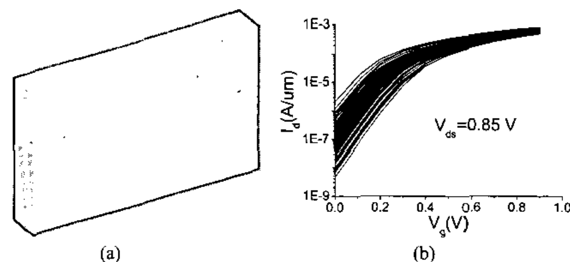

Fig. 1 (a) Potential distribution in a 35 nm MOSFET in which the detailed positions of dopants are considered. (b) Gate Characteristics from 200 macroscopically identical 35 nm MOSFETs, obtained by 'atomistic' device simulation.

Statistical compact model sets, or card libraries, are built for HSPICE simulation, and we assume that both PMOS

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and NMOS devices have similar statistical distribution of characteristics due to random doping, with average PMOS drive half that of NMOS.

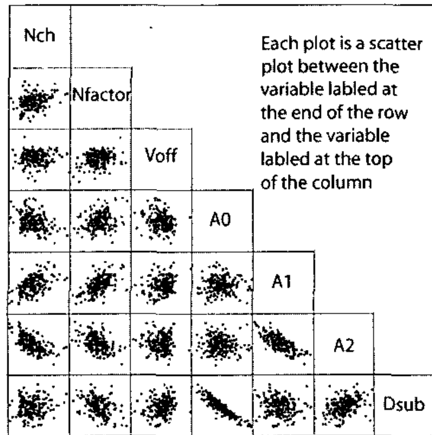

Fig. 2 Scatter plots between two mapped parameters

3. Impact of random doping on SNM

Fig. 3 (a) shows the schematic of 6-T SRAM cell, with M2, M4 driver transistors and M5, M6 access transistors. Because PMOS load transistors M1 and M3 have generally low driving ability, and the NMOS transistor is not good at passing 1, the bit line needs to be charged to 1 before a read operation. Design optimisation of an SRAM circuit concentrates on pulling the bit line from 1 to 0, and the cell is most vulnerable to noise at the initiation of this operation.

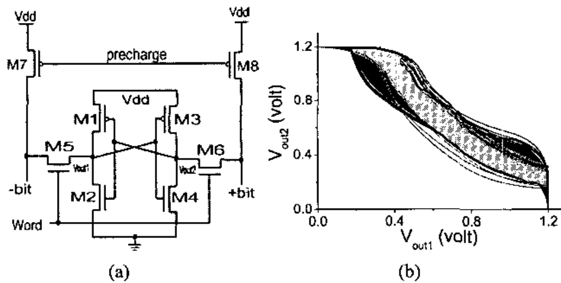

Fig.3 (a) Circuit schematics of CMOS SRAM. (b) The static transfer characteristics of 200 statistical SRAM circuit simulations.

In SRAM cell design, the width/length ratios of the load transistors and access transistors are often as close to 1.0 as possible. The ratio of the driver transistor's W/L to the access transistor's W/L is called the *cell ratio*; it determines the cell stability as well as cell size [7]. Initially, a cell ratio of 1 is assumed. As shown in fig. 3 (b), large fluctuations occur in static transfer characteristics due to random doping effects. An extreme example is shown in fig. 4 (a), and in this case, the SNM is reduced to zero and the SRAM cannot operate correctly even under ideal conditions.

Fig.4 (b) further shows the read behaviour of the device in this extreme case. Before the read, 0 is stored on node *out1* and 1 is stored on node *out2*. Although we ignore circuit noise, the state of the cell begins to flip on initiation of the read operation. After 100 ps, the state of node *out1* node is changed from 0 to 1. For a cell ratio of 1, nearly 10% of cells will malfunction due to random doping effects.

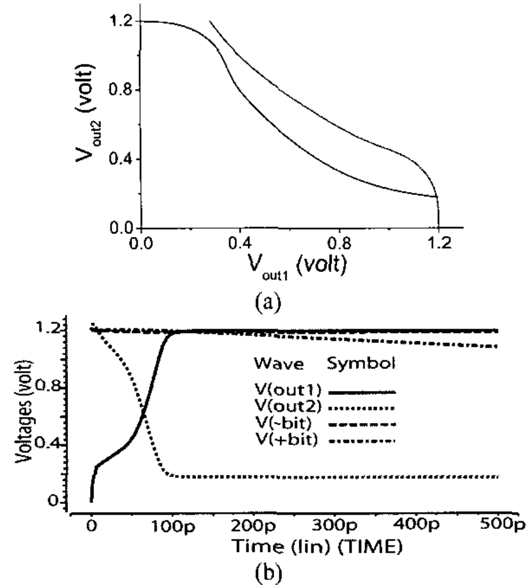

Fig.4 (a) Static transfer characteristics and (b) Read behaviour of an extreme case, cell ratio is 1

Increasing cell ratio has two benefits for improved SNM behaviour. Firstly, a larger cell ratio directly improves cell stability – reflected in the mean value of SNM, μ. Secondly, a larger W/L ratio will reduce the magnitude of the characteristic fluctuations caused by random doping effects, which is partly reflected in the normal standard deviation σ of SNM, σ/μ. Fig. 5 clearly shows these benefits from a larger cell ratio.

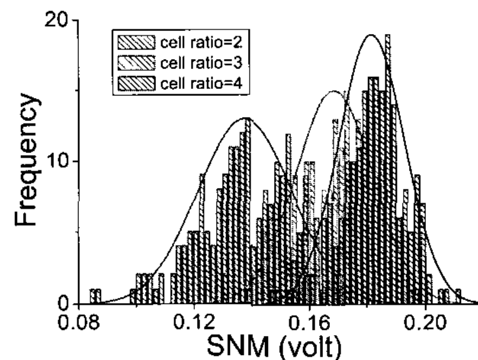

Fig.5 Distribution of SNM.

As a guideline, μ-6σ is required to exceed approximately 4% of the supply voltage to achieve 90% yield for 1Mbit SRAM's [8]. If we consider only the fluctuations caused by random doping effects (see table 1) the cell ratio should be at least 3, but if other intrinsic fluctuation sources are taken into account, a larger cell area will be required in order to achieve reasonable yield. This implies that SRAM may not gain all the benefits of further bulk CMOS scaling, from SNM point of view.

Table 1 SNM of different cell ratio SRAM

Cell ratio	Mean of SNM μ(mV)	SD of SNM σ(mV)	μ-6σ (mv)	σ/μ
2	137.69	16.28	40	11.8%
3	168.57	13.39	88.2	7.94%
4	181.59	11.32	113.6	6.23%

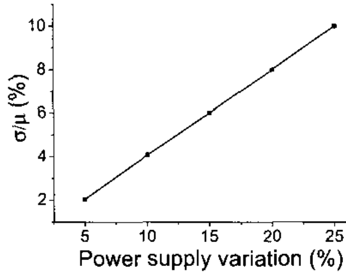

Fig. 6 Normalized standard deviation of SNM due to power supply variation

The normalized standard deviation of SNM caused by power supply instability and ignoring the fluctuations due to intrinsic parameter variations is shown in fig. 6, where the cell ratio is 3. For these devices, SNM fluctuaions caused by random doping effects are of the same level as the fluctuations caused by ±20% supply instability.

Although each individual transistor in the SRAM cell has a statistically identical characteristic fluctuation distribution, their contributions to the total SNM variation are different. For a cell ratio of 3, because of the larger W/L value, the driver transistors have a smaller absolute magnitude of characteristic fluctuations caused by random doping. However, fig. 7 shows that SNM is most sensitive to driver transistor variation, which will contribute about 70% of total SNM fluctuation, and is less sensitive to access and load transistor variations.

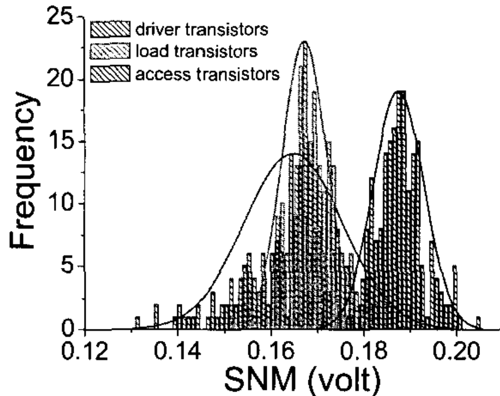

Fig. 7 SNM distributions due to random doping effects in different type of transistors

4. Impact of random doping on read/write performance

Depending on which type of sense amplifier is employed, there are two different modes of read operation for an SRAM cell: voltage or current mode. Although the issues associated with read time fluctuations are not as critical as SNMs for SRAM operation, they will determine the memory access speed and thus affect system performance. In the statistical circuit simulations, an 0.1 pF bit capacitance is assumed. In order to have sufficient noise margin, we also assume the threshold for the sense amplifier is 0.6 V for voltage mode, and that the read time is roughly the time taken for the bit line voltage to drop to the sense threshold. In current mode, the voltage swing is not critical for read operation; peak current is used as a probe to detect read time fluctuation. Figs. 8-9 and tables 2-3 show the impact of random dopant variation on both read modes.

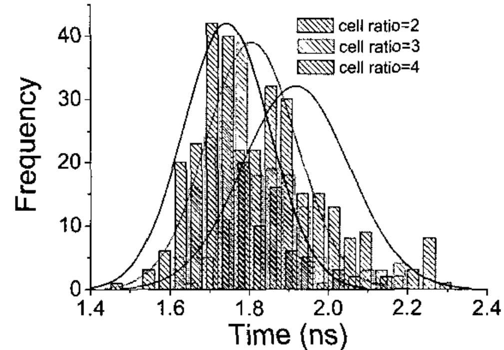

Fig. 8 Read time distribution for voltage mode

Table 2 Read time distribution for voltage mode

Cell ratio	Mean of Time μ(ns)	SD of Time σ(ns)	σ/μ
2	1.92	0.136	7.1%
3	1.81	0.113	6.3%
4	1.74	0.11	6.26%

For larger cell ratios, cell pull down resistance becomes smaller, which will help to improve general read access performance. Compared to the SNM case, the fluctuation behaviour of read operations are less sensitive to cell ratio. Roughly, random dopant effects will cause 40% performance difference between fastest and slowest memory accesses. In general, current mode is superior in all aspects of voltage swing and the sensitivity to bit capacitance, and as the impacts of random dopant effects on both modes are similar, current mode would still be a good choice for read operation even when intrinsic parameter fluctuations begin to play a greater role in device characteristic mismatch as devices shrink.

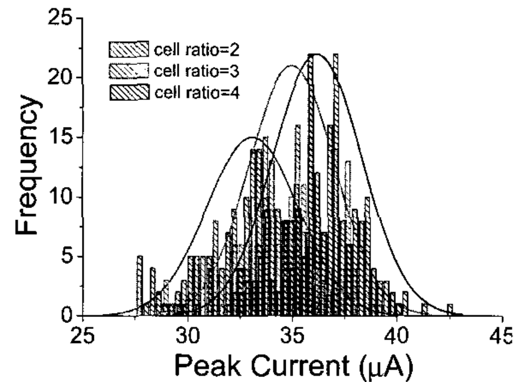

Fig.9 Peak current distribution for current mode

Table 3 Peak current distribution for current mode

Cell ratio	Mean of Current $\mu(\mu A)$	SD of Current $\sigma(\mu A)$	σ/μ
2	33.1	2.2	6.6%
3	35	2	5.8%
4	36.2	2.1	5.9%

During write operations, a full voltage swing on a bit line is often required to override the previous cell data. In reality, such signals are produced by peripheral circuitry. In order to clearly illustrate the impact of random dopant effects on the cell itself, the peripheral circuit is excluded in the circuit simulation and an ideal complementary write signal is directly applied on the bit lines.

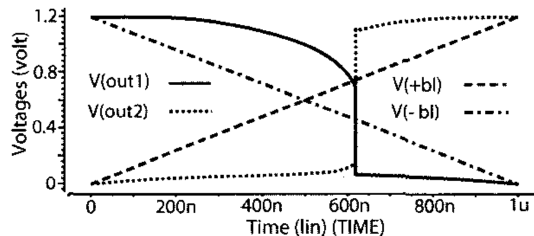

Fig. 10 HSPICE simulation result for a typical writing operation, cell ratio is 3

The switch point voltage is defined as the bit line voltage which will cause cell data to begin to change under a write operation. It is another important parameter in cell design, which, together with the SNM, will determine cell stability. Typical write behaviour is shown in fig. 10, where quasi-static operation is considered in order to clearly show the switch point voltage.

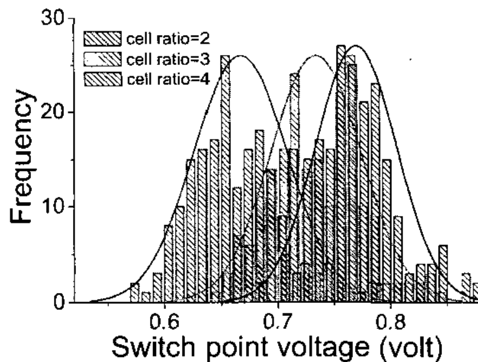

Fig. 11 Distribution of switch point voltage (+bl)

Table 4 Switch point voltage (+bl) distribution

Cell ratio	Mean of Voltage μ(volt)	SD of Voltage σ(volt)	σ/μ
2	0.67	0.041	6.1%
3	0.73	0.04	5.4%
4	0.77	0.036	4.7%

A larger cell ratio will give higher switch point voltage (shown in fig. 11 and table 4), which results in better noise immunity, in concert with the earlier results for SNM. When the cell ratio is increased from 2 to 4, the magnitude of the relative differences between the highest and lowest switch point voltages is also improved. Such quantitative results allow the circuit designer to trade off these benefits against the requirements of circuit speed, area and power dissipation for a given system application.

5. Conclusions

Intrinsic parameter fluctuations, such as those caused by random channel doping, will become a main source for device characteristic mismatch in the decanano regime. Using an 'atomistic' statistical circuit simulation methodology, the effect of random dopants on the operation of 6-T SRAM based on well-scaled 35 nm gate length devices has been studied in detail. Results show read/write variation caused by random dopant fluctuations will degrade overall SRAM speed, but SNM fluctuation caused by random dopants will become a fundamental limitation for further bulk SRAM scaling.

Acknowledgements

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