Scaling study of Si and strained Si *n*-MOSFETs with different high-κ gate stacks

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Abstract

Using Ensemble Monte Carlo device simulations this paper studies the impact of interface roughness and soft-optical phonon scattering on the performance of sub-100nm Si and strained Si MOSFETs with different high-κ gate stacks. Devices with gate lengths down to 25nm have been investigated.

Introduction

Strained Si (SSi) channel and high-κ gate dielectrics have both been considered as performance boosters for CMOS technology beyond the 90nm technology node [1]. The performance enhancement of SSi MOSFET devices comes from the strain induced mobility enhancement and possibly reduced interface roughness (IR) scattering [2]. Achieving high-quality high-κ dielectrics on top of Si is still problematic due to many technological issues. However, a fundamental drawback of MOSFETs with high-κ dielectrics is the mobility degradation due to soft optical (SO) phonon scattering [3,4,5,6]. In this work, we study the impact of IR and SO-phonon scattering on the performance of sub-100nm conventional Si and SSi *n*-MOSFETs with different gate dielectrics using self-consistent Poisson-Ensemble Monte Carlo (EMC) device simulations. We have studied devices with gate lengths from 80nm down to 25nm. The simulated device structures are illustrated in Fig. 1.

Interface roughness and soft-optical phonon scattering

Fig. 2 illustrates the electron mobility in SSi as a function of substrate Ge content obtained using our EMC simulator compared with data from [7]. The simulator includes our recently developed non-perturbative IR scattering model [8], incorporated as a boundary condition for the Boltzmann Transport Equation. The model provides the probability of specular and diffuse scattering as a function of the incident solid angle, carrier energy and the autocorrelation function of the rough interface. It has been validated in comparison with *ab initio* calculations based on the numerical solution of the time dependent Schrödinger equation for an incident wave-packet (particle) scattering from a rough surface [9], as illustrated in Fig. 3. The model has also been validated in comparison with 'universal' mobility results for Si and SSi with a SiO_2 gate stack [10,11,12], as shown in Fig. 4. A smoother interface for SSi, characterised by R.M.S. height (RMS)=0.5nm and correlation length (CL)=3.0nm (using an exponential autocorrelation function) is needed to match the experimental data, compared to RMS=0.5nm and CL=1.8nm for bulk Si.

The introduction of high-κ gate dielectrics reduces the gate leakage current typically by orders of magnitude. However, it also introduces strong soft optical phonon scattering [3]. The scattering results from the strong ionic polarisability of the high-κ material, which also determines the large value of the dielectric constant. Electrons scatter from these phonons via a Fröhlich interaction, which has an unscreened scattering field amplitude at the dielectric interface given by:

$$\phi_{\omega_{SO}} = \left\{ \frac{\hbar\omega_{SO}}{2q^2} \left[\frac{1}{\varepsilon_{Si}^{\infty} + \varepsilon_{ox}^{\infty}} - \frac{1}{\varepsilon_{Si}^{\infty} + \varepsilon_{ox}^{0}} \right] \right\}^{1/2} \qquad (1)$$

where $\varepsilon_{ox}^{\infty}, \varepsilon_{ox}^{0}$ and $\varepsilon_{Si}^{\infty}$ are the optical and static permittivities for the oxide and Si respectively and ω_{SO} is the soft-optical (SO) phonon energy, calculated from the two dominant transverse-optical (TO) phonon modes in the dielectric via the Lyddane-Sachs-Teller relationship. Table 1 lists the static and optical permittivities, along with the phonon energies for two TO modes, ω_{TO1} and ω_{TO2}, for the different dielectrics considered in this work. It can be seen from Table 1 and equation (1) that for low phonon energies, the larger difference between the static and optical permittivities for the high-κ dielectrics, HfO_2 and Al_2O_3, lead to strong scattering of carriers in the inversion layer.

Simulation of Si and SSi MOSFETs with SiO_2

The benchmark devices for our simulations are the 80nm gate length (67nm effective channel length) conventional Si and SSi *n*-MOSFETs with 2.2nm SiO_2 published by IBM [10] and a 35nm gate length *n*-MOSFET with 1.2nm SiON published by Toshiba [13]. The high-κ dielectric devices assume the same structures and equivalent oxide thickness (EOT) as the devices with SiO_2, as illustrated in Fig. 1. The test devices were carefully analyzed using the device simulators MEDICI and TAURUS [14] to deduce the device structures from published data, as illustrated in Figs 5 and 6. The reverse-engineered devices were then simulated using our EMC simulator. Using the IR parameters given

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above the EMC simulations were able to reproduce the experimental characteristics of the IBM devices (see Fig. 7), confirming that the smoother SSi/SiO_2 interface contributes to the observed performance enhancement of SSi MOSFETs. Fig. 8 shows the average carrier velocities in the channel of the IBM Si and SSi devices with and without interface roughness scattering.

We have also simulated a 35nm MOSFET published by Toshiba [13]. This structure is likely to exhibit a degree of process-induced strain. We have found that a strain equivalent to SSi (employing the IR parameters for Si) on a 5% Ge content SiGe buffer is necessary to reproduce the experimental data [13], as shown in Fig. 9. Fig. 9 also plots the simulated device characteristics for 35nm devices assuming differing amounts of strain within the channel. A strained channel MOSFET with an equivalent 20% Ge content buffer (employing the IR parameters for SSi) delivers ~41% drive current enhancement over the original design, in agreement with the recently observed 45% drive current enhancement for a 35nm Si/$Si_{0.8}Ge_{0.2}$ MOSFET [15]. The 35nm MOSFET was then scaled to 25nm using TAURUS process and device simulations and the device structure was simulated using the EMC simulator. Fig. 10 illustrates the simulated device characteristics of 25nm MOSFETs assuming different degrees of strain; the 25nm device with 20% Ge content equivalent strain delivers a ~37% drive current enhancement over the device with a 5% Ge content equivalent strain.

Simulation of Si and SSi MOSFETs with high-κ gate stacks

The SiO_2 used in the simulations of the 80nm and 35nm devices were then replaced by high-κ dielectrics: HfO_2 and Al_2O_3 with the same EOT as in the original devices. This leads to the same gate capacitances and provides almost identical electrostatic gate control for the devices with SiO_2 and high-κ gate stacks. However, in the presence of high-κ dielectrics the carriers within the inversion layer are subjected to significant SO phonon scattering, leading to a reduction in their mobility. Therefore a reduction in device-drive current is expected when high-κ dielectrics are introduced.

The EMC simulator includes SO phonon scattering [3] and the scattering rate for the absorption of one (SO) phonon mode in the X-valley of Si is illustrated for the Si/HfO_2 interface in Fig. 11. The scattering rate decreases with increasing energy (typical of a Fröhlich interaction) and drops exponentially as a function of the distance from the Si/HfO_2 interface.

Figs. 12 and 13 show the simulated I_D-V_G characteristics for 80nm Si and SSi MOSFETs with a 2.2nm EOT HfO_2. A drive current degradation, due to SO phonon scattering from the high-κ, of around 25% is observed for both Si and SSi devices. Such drive current reduction is around 10% in the Al_2O_3 case (see Fig. 14). The differences in current degradations due to SO phonon scattering can be explained by the larger phonon energies and reduction in the difference between the static and optical permittivities, as we move from HfO_2 to Al_2O_3. In high-κ gate dielectrics the large static dielectric constant arises from the highly polarized ionic bonds, which lead to lower phonon energy and smaller optical permittivity. Conventional SiO_2 has the lowest static dielectric constant, but harder bonds and thus higher phonon energy, which results in the small effect of SO phonon scattering in SiO_2 based devices. In this case we observe less than a 5% reduction in the drive current when applying SO phonon scattering for such devices.

Fig. 15 compares the average channel velocities with and without SO phonon scattering at the same gate overdrive for both Si and SSi devices, indicating that the introduction of high mobility strained channels can be used to counteract the performance degradation due to SO phonon scattering in devices with high-κ gate stacks. Fig. 16 illustrates the I_D-V_G characteristics for 35nm Si MOSFETs assuming 15% and 20% Ge content equivalent strain with an HfO_2 EOT, corresponding to a 1.2nm SiON. The drive current degradation due to SO phonon scattering in the 35nm devices is around 8%, which we may attribute to a reduction in SO phonon scattering rate with increasing carrier energy as might be expected in devices with shorter channels.

Conclusions

Reduced interface roughness scattering contributes to the observed performance enhancement of strained Si MOSFETs. Significant drive current degradation of around 25% at V_G-V_T=1.0V and V_D=1.2V is observed in equivalent oxide thickness conventional and strained Si devices with an HfO_2 gate stack. This compares to ~10% degradation arising from the introduction of an Al_2O_3 gate stack. As a reference, the current degradation associated with SO phonons in SiO_2 devices with identical structures is less than 5%. Our results also indicate that the inherent mobility degradation associated with the high-κ gate stack MOSFETs might be compensated by the introduction of strained Si channels. The infancy of high-κ gate fabrication techniques means that other performance degrading scattering mechanisms are likely to be present including a strong interface roughness contribution. Thus the overall performance degradation associated with high-κ gate dielectrics is expected to be worse than the predictions made in this paper.

Acknowledgements

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Table 1: Parameters used to calculate the electron soft-optical phonon coupling in high-κ gate dielectrics, reference [3].

	SiO_2	Al_2O_3	HfO_2
$\varepsilon_{ox}^{0}(\varepsilon_0)$	3.90	12.53	22.00
$\varepsilon_{ox}^{\infty}(\varepsilon_0)$	2.50	3.20	5.03
ω_{TO1} (meV)	55.60	48.18	12.40
ω_{TO2} (meV)	138.10	71.41	48.35
ω_{SO1} (meV)	57.14	53.19	16.79
ω_{SO2} (meV)	140.78	82.48	50.67

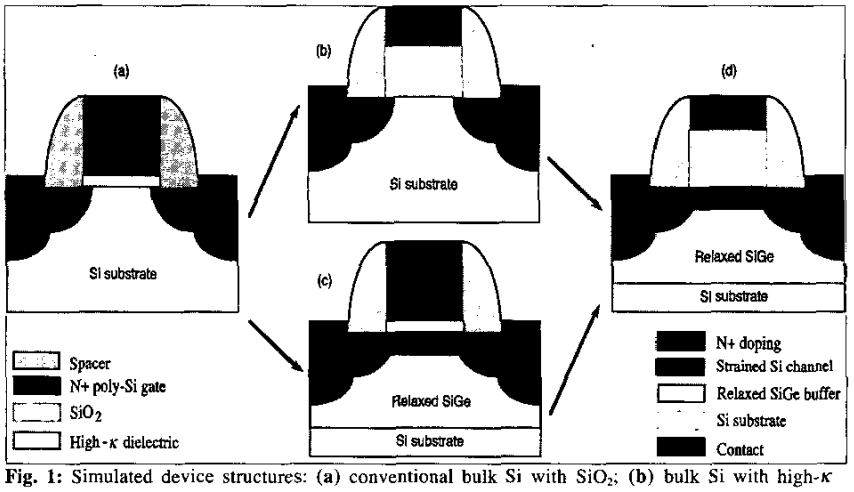

Fig. 1: Simulated device structures: (**a**) conventional bulk Si with SiO_2; (**b**) bulk Si with high-κ dielectric; (**c**) strained Si with SiO_2; (**d**) strained Si with high-κ dielectric.

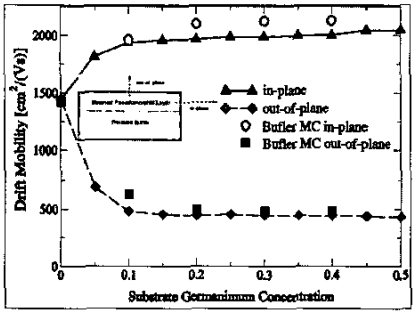

Fig. 2: In- and out-of-plane low-field electron mobilities for strained Si as a function of substrate Ge concentration. Inset shows the *in-* and *out-of-plane* directions.

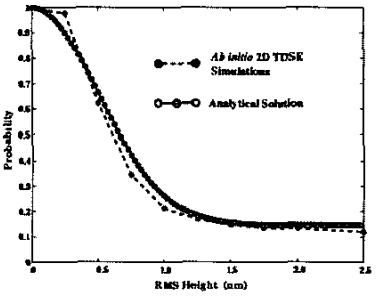

Fig. 3: Probability of specular reflection from a rough interface as function of the r.m.s height calculated analytically and via *ab initio* solutions of the 2D Time Dependent Schrödinger Equation (TDSE).

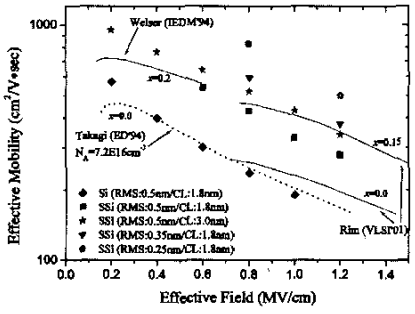

Fig. 4: Effective electron mobilities of bulk Si and strained Si by Monte Carlo.

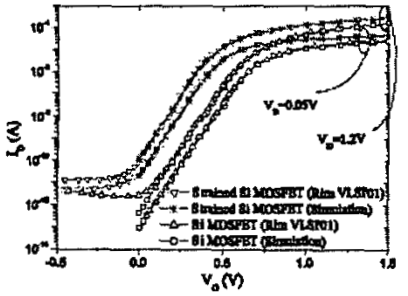

Fig. 5: MEDICI calibrated I_D-V_G characteristics of the IBM 80nm gate length Si and strained Si MOSFETs, for a 0.28μm device width.

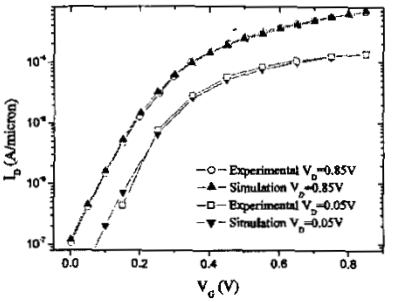

Fig. 6: TAURUS calibrated I_D-V_G characteristics of the Toshiba 35nm gate length Si MOSFET.

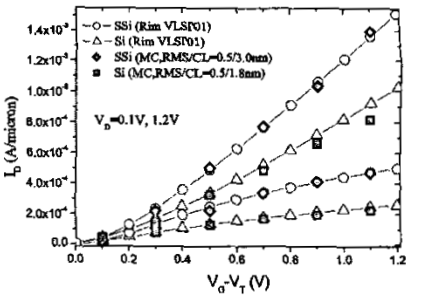

Fig. 7: I_D-V_G characteristics of the 80nm gate length Si and strained Si MOSFETs.

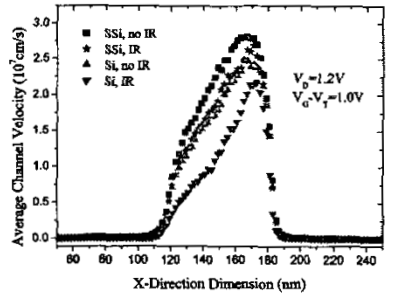

Fig. 8: Average channel velocities of the 80nm Si and strained Si MOSFETs with and without IR scattering.

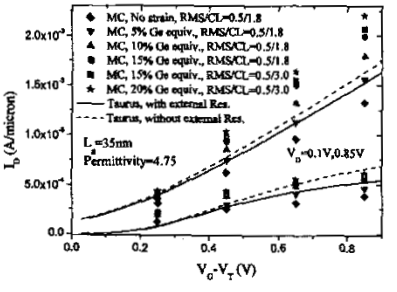

Fig. 9: I_D-V_G characteristics of 35nm gate length Si and strained Si MOSFETs

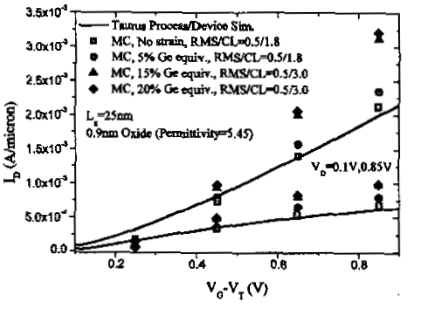

Fig. 10: I_D-V_G characteristics of 25nm gate length Si and strained Si MOSFETs

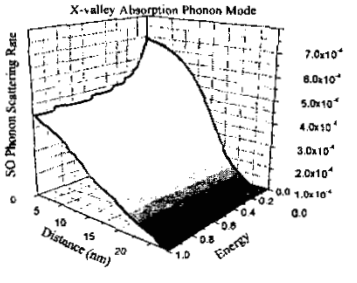

Fig. 11: Scattering rate of SO phonon scattering in a Si/HfO_2 system (absorption mode of one phonon mode in *X*-valley).

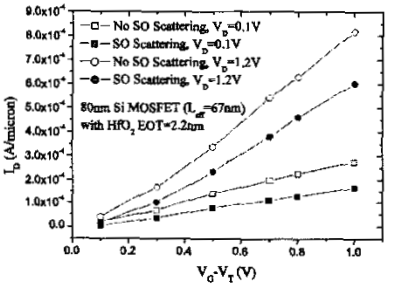

Fig. 12: I_D-V_G characteristics with and without SO phonon scattering of 80nm conventional Si MOSFET with HfO_2.

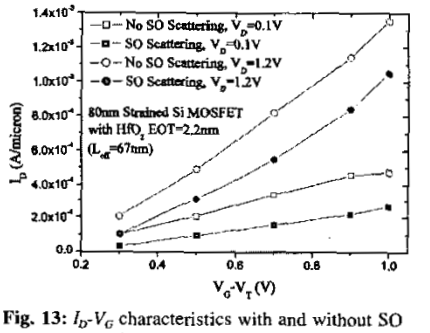

Fig. 13: I_D-V_G characteristics with and without SO phonon scattering of 80nm strained Si MOSFET with HfO_2.

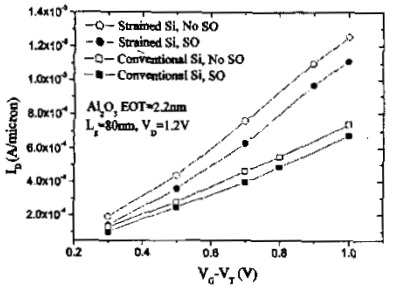

Fig. 14: I_D-V_G characteristics with and without SO phonon scattering of 80nm Si and strained Si MOSFETs with Al_2O_3.

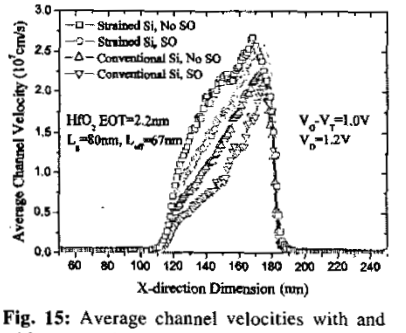

Fig. 15: Average channel velocities with and without SO phonon scattering in 80nm Si and SSi MOSFETs with HfO_2.

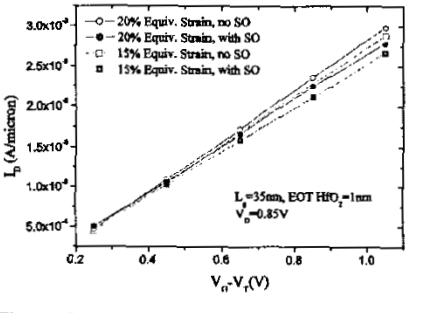

Fig. 16: I_D-V_G characteristics with and without SO phonon scattering of 35nm strained Si MOSFETs with HfO_2.