A Diode Device Combining Lateral Field-Effect Transport and Vertical Tunneling in a Multi-Quantum-Well Heterostructure

J. Marczewski, M. Zachau, A. Asenov, F. Koch, and D. Gruetzmacher

Abstract—**We discuss an electronic device with asymmetric contacts to a multilayer heterostructure. Current enters via an alloyed ohmic contact into the quantum wells (QW's) and flows laterally along capacitively coupled channels. It leaves via tunneling between the layers and through a forward-biased surface Schottky contact. A step-like $I-V$ dependence is observed and interpreted by a model calculation.**

I. Introduction

A NUMBER of devices based on semiconductor heterostructures have been realized. With few exceptions, they can be classified into those for which current flows parallel to the epitaxially grown layers (for example, the high electron mobility transistor (HEMT)) and those with vertical current flow (for example, the resonant tunneling diode (RTD)). The principle of electronic action is the field effect for the "lateral" devices. For the "vertical" structures it is the barrier principle.

The exception to the rule is devices like the monolithically integrated HEMT-RTD, in which gate-controlled lateral current enters a vertical RTD structure [1], [2]. Such devices have interesting modes of operation but represent nothing new in the sense that they just couple two well-studied devices in series.

We study here a novel diode structure in which the field-effect and barrier-transport principles are inextricably linked. We make use of a lightly n-doped, multi-quantum-well (MQW) heterostructure dimensioned to allow tunneling between the layers. By the use of asymmetric contacts, one of which is an in-diffused ohmic contact, the other a surface Schottky barrier positioned a short distance away from the ohmic one, we have achieved a stepped current–voltage relation with a very specific characteristic. The steps and other detailed features of the $I-V$ curve can be tailored by individually adjusting the well parameters. To explain the device we have modeled it.

Manuscript received February 28, 1992.

J. Marczewski is with the Physik Department, Technischen Universität Muenchen, 8046 Garching, Germany on leave from the Institute of Electron Technology, Warsaw, Poland.

M. Zachau and F. Koch are with the Physik Department, Technischen Universität Muenchen, 8046 Garching, Germany.

A. Asenov is with the Physik Department, Technischen Universität Muenchen, 8046 Garching, Germany on leave from the Institute of Microelectronics, 1784 Sofia, Bulgaria.

D. Gruetzmacher is with RWTH Aachen, Institut für Halbleitertechnik, 5100 Aachen, Germany.

IEEE Log Number 9201037.

II. Device Construction

The diode is fabricated on a lattice-matched, InGaAs–InP MQW heterostructure. The substrate is semi-insulating InP. The buffer layer is n-doped InP with a thickness of 500 nm. There follows 100-nm undoped InP and a sequence of 15 InGaAs 8-nm wells separated by 30-nm-thick barriers. The cap layer is 100 nm of InP. The heterostructure is lightly n-type ($N_D \approx 1 \times 10^{15}$ cm^{-3}) from unintentional background doping. This is known to provide each QW with something like $\approx 1 \times 10^{10}$ electrons cm^{-2}.

Fig. 1 shows the sequence of layers together with the contacts. Electrons enter via the alloyed Au–Ge region that makes a parallel connection to the QW's. The electron current then continues along the QW channel and leaves by tunneling through the barrier regions and the forward-biased Au Schottky surface contact. The distribution of currents among the parallel channels depends on the voltage, as well as on the electrical conductivities and barriers of the structure. In our case the alloyed Au–Ge reaches down into the n^+-buffer layer. The separation of the two contacts is approximately 1 mm. In principle the structure could have been defined by mesa etching. For simplicity, we have worked with a wafer containing many contacts that could be individually attached to the measuring circuit.

III. Experimental Results

Fig. 2 gives the current–voltage ($I-V$) characteristic at 77 and 4.2 K together with the conductance G at 77 K. After a threshold voltage of 1.6 V, the current increases in steps. Successive step increases become larger and larger while the plateaus become narrower.

The temperature plays a role. The step-like characteristic is best resolved in the 77-K range. At room temperature where thermally activated processes dominate the tunneling between wells, the current follows the characteristic of the Au–InP Schottky contact. At low temperatures in the liquid-helium range, independent measurements show that there is no conduction in the very lightly doped n-type QW's up to lateral fields of several tens of volts per centimeter. The

0741-3106/92$03.00

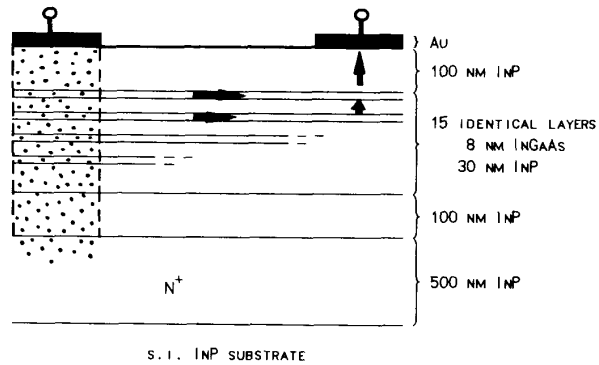

Fig. 1. Structure of the device integrating lateral field-effect conduction with vertical tunneling. Arrows indicate the electron current path in two conducting wells.

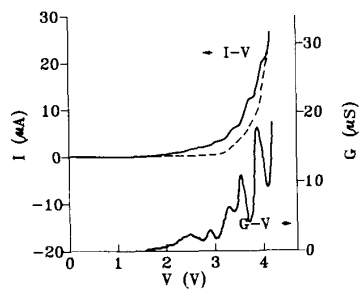

Fig. 2. Experimentally observed current-voltage and conductance-voltage characteristics of the device at 77 K. The dashed curve was measured at 4.2 K.

carriers are apparently trapped. The threshold voltage for current flow has shifted in Fig. 2 to near 3.0 V. At this value it rises steeply and without the steps.

This last observation provides the essential clue to understanding the steps. At 4.2 K there is only current flow from the buffer layer by vertical tunneling through the sequence of QW barriers. The steps at 77 K are an additional parallel current through the channels. Since the latter are capacitively coupled, a field-effect-transistor (FET)-like action results. The I–V characteristic is unlike that known from the literature [3], [4]. The decreasing plateau width together with the increasing step height is a specific feature of the FET type of action. The plateaus are the result of current saturation in FET conduction. Six steps are resolved in Fig. 2, which is less than the number of wells, which is 15. We believe that the others are masked by the steep rise of the current above 4.0 V.

IV. Discussion and Model Calculations

Lateral current flow along the capacitively coupled layers is governed by the principles of FET action. Each layer is a channel with two resistive gates formed by the QW's above and below. The layers have a common source contact (ohmic Au–Ge). Electron currents leave the layer by tunneling into the upper sheet where there is sufficient voltage drop near the end of the layer under the surface contact. The uppermost and lowest of the 15 layers are different. The InP layers act as gate insulators for the coupled FET's.

The barriers (30 nm thick) are traversed by Fowler–Nordheim tunneling in an electric field. The maximum barrier height is the difference between the band offset (220 meV) and the lowest energy level in the InGaAs well (55 meV). An exponentially rising current may be expected when the voltage between a pair of layers exceeds $\approx$ 165 meV. The rise in current will clamp the drain regions of the layers near this value of difference voltage. The topmost layer (100 nm thick) requires approximately three times more voltage. This leads one to expect that the sandwich of 15 consecutive layers between the buffer layer and surface contact will have an exponentially rising current starting at about $(14 + 3) \times 0.165 \approx 3$ V at low temperature.

At 77 K, conduction along the lightly doped parallel channels is possible. The I–V curve has additional currents which are successively switched on as Fowler–Nordheim breakdown between the layers becomes possible. One after another, parallel paths are added and cause a current increase. Conduction is governed by the field-effect action and has a characteristic current saturation. This is the essential element shaping the I–V curve.

We consider the kth QW with resistive-gate $k-1$ and $k+1$ QW's. Current I_k is a function of the voltages V_{k-1}, V_k, and V_{k+1} at the drain end of the QW's. In terms of the gradual channel approximation,

$$I_k = \frac{\mu 2CW}{L}\left(V_T V_k + \frac{1}{4}(V_{k-1} + V_{k+1})V_k - \frac{1}{2}V_k^2\right) \quad (1)$$

where $V_T = qN/2C$ is the threshold voltage, μ is the mobility, C is the capacitance of the barrier layer, and W and L are the width and length of the device, respectively. qN is the charge per unit area from the background dopants. The factor 2 in the numerator of (1) is because two gates control, each of them through capacitance C, the conduction of one channel. The middle term in parenthesis of (1) is for the case of resistive gates with current flow along them. It also reflects the assumption that the potential distributions along the channels are proportional to each other. The saturation voltage is

$$V_k^{\text{sat}} = V_T + \frac{V_{k-1} + V_{k+1}}{4}. \quad (2)$$

The voltage rise along the depleted part of the channel induces charge in the well immediately below it. As a result, for this lower FET channel, the effective drain contact extends into the channel. Whenever the voltage reaches a value sufficient to open the next diode, the voltage drop along the channel causes a carrier-density increase in the already conducting channels. Thus, the current–voltage characteristic of one channel is seen to depend on the on–off state of all the others (coupled FET's).

The Fowler–Nordheim characteristic that describes the tunneling at the drain end of the FET channels is

$$I_k = A(V_{k-1} - V_k)^2 \exp\left(\frac{-bd}{(V_{k-1} - V_k)}\right) \quad (3)$$

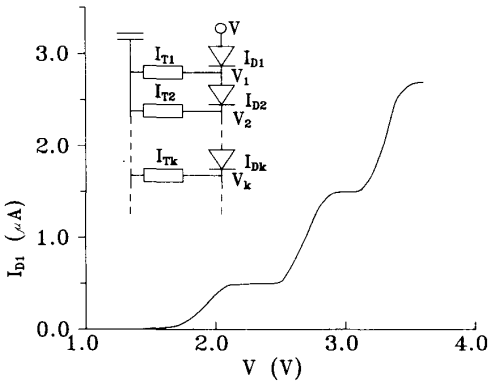

Fig. 3. Calculated current–voltage characteristic of a device consisting of three capacitively coupled layers (represented by the FET's and diodes in the equivalent circuit).

where A and b are fitted constants and d is the barrier thickness.

We simulate the device in terms of the circuit elements arranged as in Fig. 3. Elements $T_1, \cdots, T_k$ are identical FET channels with $\mu = 6 \times 10^4$ cm^2/V · s, $N = 2 \times 10^{10}$ cm^{-2}, $W = 1.5$ mm, and $L = 2$ mm. The set of coupled nonlinear equations for the currents in our device is

$$\begin{aligned} &I_{D1}(V - V_1) = I_{T1}(V_1) + I_{D2}(V_2 - V_1) \\ &\cdots \\ &I_{Dk}(V_{k-1} - V_k) = I_{Tk}(V_k) + I_{Dk+1}(V_{k-1} - V_k) \\ &\cdots \\ &I_{DM}(V_{M-1} - V_M) = I_{TM}(V_M). \end{aligned} \quad (4)$$

The solution for $M = 3$, $b = 3.0 \times 10^6$ V/cm, and $A = 1.6$ A/V^2 is given in Fig. 3. Diode D_1 has $d = 100$ nm, while D_2 and D_3 have $d = 30$ nm.

The simulation does reproduce essential characteristics of the experiment. The current onset is tied to the thickness of the surface tunneling layer. The first plateau represents saturation conditions in this first channel. The next current step represents an additional parallel path through T_2 and an increased I_{T1}. Along with the increased current step height, the plateau width is reduced.

For the low doping level of these wells, saturation is reached a short distance from the ohmic contact. The pinchoff region moves along the QW as more parallel channels start to conduct. The two-dimensional field distribution is not described properly by (1)–(4). The fact that we observe only six plateaus from the 15 QW's may be related to the fact that pinchoff is not achieved in the layers after $k = 6$. Not included in the simulation is the buffer layer.

In conclusion, we emphasize that the present device is an example of a structure that integrates field-effect action in lateral transport with vertical tunneling transport. The device functions in such a way as to deliver a multilevel digital current output for a continuous analog input voltage. By appropriate choice of doping, of barrier heights and widths, of various lengths, and of other relevant parameters, it could be designed to produce a very specific multilevel output to suit a particular purpose. As a diode the device will have a limited number of applications. In this presentation we wished to illustrate the principle of integrated lateral-vertical transport by the simple use of asymmetric surface contacts on a MQW heterostructure.

References

[1] T. K. Woodward and T. C. McGill, "Integration of a resonant-tunneling structure with a metal-semiconductor field-effect transistor," *Appl. Phys. Lett.*, vol. 51, pp. 1542–1544, 1987.

[2] W. De Raedt, M. Van Hove, C. Van Hoof, and M. Van Rossum, "Monolithic integration of pseudomorphic HEMT's and resonant tunneling devices," to be published in *Proc. Gallium Arsenide and Related Compounds* (Inst. Phys. Conf. Ser.), (Jersey, U.K.), 1990.

[3] K. Choi, B. F. Levine, C. G. Bethea, J. Walker, and R. J. Malik, "Photoexcited coherent tunneling in a double-barrier superlattices," *Phys. Rev. Lett.*, vol. 59, pp. 2459–2462, 1987.

[4] J. Allam, F. Capasso, M. B. Panish, and A. L. Hutchinson, "Observation of novel step-like structure in the photocurrent and dark current of a superlattice: Charge collection by successive depletion of quantum wells," *Appl. Phys. Lett.*, vol. 49, pp. 707–709, 1986.