Cryo-CMOS Mixed-Signal Circuits for Scalable Quantum Computing: Challenges and Future Steps

Stavroula Kapoulea, Meraj Ahmad, Martin Weides, and Hadi Heidari

James Watt School of Engineering,University of Glasgow

Glagsow G12 8QQ, UK

Email: {Stavroula.Kapoulea, Meraj.Ahmad, Martin.Weides, Hadi.Heidari}@glasgow.ac.uk

***Abstract*—A systematic research on the development of cryogenic complementary metal-oxide semiconductor (cryo-CMOS) circuits, for implementing the required control electronics to manipulate the quantum bit (qubit) state, is performed over the last few years. Scalability constitutes a key term regarding the evolution of quantum computing from theory to practical application and CMOS technology has been proven to be a promising candidate for implementing the coveted scalable next-generation quantum computers (QCs). Mixed-signal blocks, used for uniting the analog and digital domains, play a key role in the efficient functionality of the qubit control/readout system, thus there is an ever-increasing interest in their high-performance circuit realization. The critical challenge in this venture is to achieve efficient cryogenic operation at low temperatures, i.e., close to the qubit around 4 K, simultaneously keeping power requirements at low values. An overview and comparison of the cryo-CMOS Digital-to-Analog converter (DAC) and Analog-to-Digital converter (ADC) circuit implementations for quantum computing applications that heretofore have been proposed in the literature is presented in this work. A discussion on the challenges and future strategic steps that are henceforth required to proceed toward the development of a functional scalable quantum computer is also conducted.**

Keywords—quantum computing, quantum control, cryogenic electronics, cryogenic CMOS circuits, mixed-signal circuits, analog-to-digital converters, digital-to-analog converters

I. Introduction

Interest in the practical implementation of future scalable quantum computers (QCs) has enriched the literature with a wealth of work on the challenges and potentials of designing complementary metal-oxide semiconductor (CMOS)-based circuits capable of operating at deep cryogenic temperatures [1−8]. The requirement for such circuits was generated from the necessity to gradually move the qubit control/readout unit from room temperatures (RT), and the restrictions of a bulky, delay-generating coupling between the quantum processor and the external environment, to lower temperatures closer to the qubits. The long-term objective of this method is to attain an integrated quantum computing System-on-Chip (SoC), which will comprise the quantum processor and the required control electronics at temperatures around 10 mK. Currently, such low-temperature operation is not practically feasible due to the limited cooling power of the available dilution refrigerators and the unavailability of reliable deep cryogenic device models. A provisional solution to overcome these drawbacks is to put the control/readout unit at the lowest possible temperature, i.e., around 4 K in close proximity to the qubits at 10 mK, in order to limit the high-speed interconnect to the external environment.

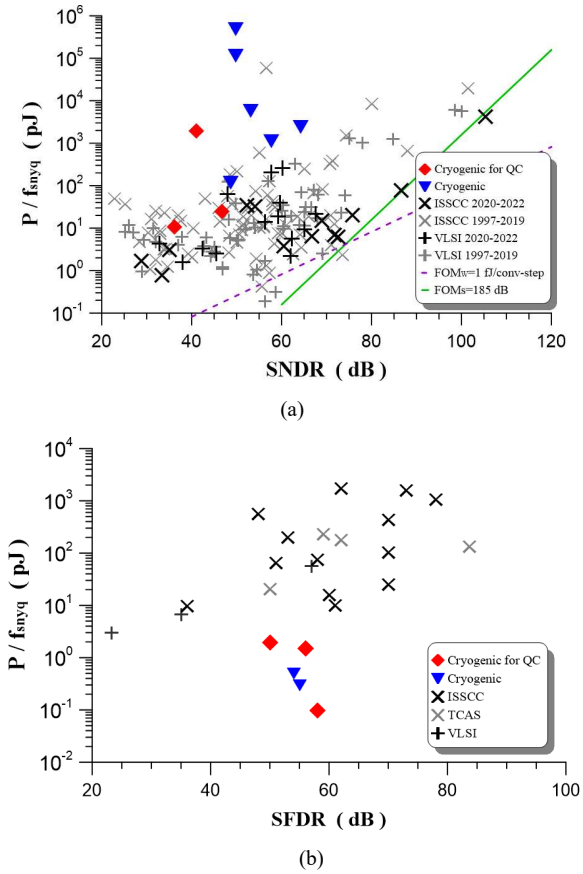

Fig. 1. Energy diagram for state-of-the-art (a) ADCs and (b) DACs. Blue triangle represents cryogenic ADCs/DACs, red rhombus cryogenic ADCs/DACs for quantum computing applications, whereas black and grey symbols correspond to room-temperature SAR ADS [14] and current-steering DACs.

The efficacy of the qubit control/readout system relies heavily on two fundamental mixed-signal blocks, the Analog-to-Digital converter (ADC) and Digital-to-Analog converter (DAC), thus significant research steps towards their cryogenic CMOS-based implementation have been taken in recent years [9−27]. A survey on the state-of-the-art literature for both types of converters is demonstrated in Fig. 1, highlighting the cryogenic and cryogenic quantum computing related works. More details for each type are provided in Sections II and III for ADCs and DACs, respectively.

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As expected, there are important variations in the performance characteristics of solid-state electronics at such low temperatures compared to the conventional room-temperature performance. Hence, the main obstacle in the cryo-CMOS circuit design process is the unavailability of cryogenic MOS transistor models that would directly achieve an efficient operation of the circuit at the desired low temperature. Characterization of the current transistor models of different nanoscale technologies at cryogenic temperatures has shown that the most critical performance features are importantly affected while approaching values of liquid Helium temperature and lower, i.e., increase in threshold voltage, charge mobility and transistor mismatch, a fact that demonstrates the emerging need for generating accurate cryo-CMOS models [27−35]. Exploiting the results obtained by the characterization process, the currently available room-temperature models have been used as a tentative solution for building cryogenic circuitry for quantum computing purposes.

The paper is structured as follows: Section II summarizes the steps taken up to this point to implement a cryo-CMOS ADC, whereas Section III provides the corresponding information about its inverse counterpart, i.e., a cryo-CMOS DAC. Concluding, existing challenges in the field and future directions towards the development of progressively more advanced cryogenic quantum circuits are discussed in Section IV.

II. Analog-To-Digital Converters

A. Architecture Techniques

Quantum readout operations require fast sampling rates (~GHz), wide bandwidth (~MHz−GHz), and low power consumption (~mW). Though, reading the state of one qubit requires a few tens of MHz sampling frequency, so why to use such a higher speed after all? The answer is: scalability! Combining the individual qubit signals utilizing the frequency-division multiplexing (FDM) technique, the required circuitry for their digitalization can be considerably simplified, allowing the simultaneous readout of multiple qubits, and reducing the power requirements of the system. To make this point clear, let us consider a sampling rate (f_s) of 2 GHz and a qubit frequency of 20 MHz. The efficient bandwidth will be approximately $f_s/2$=1 GHz, which means that the readout of ~50 qubits is attainable.

ADCs constitute fundamental building blocks of the frequency-multiplexed qubit readout process, down sampling the (amplified) analog I/Q signals to "read" the qubit state. Among the commonly used ADC architectures are the direct-conversion (or flash), the conventional successive-approximation register (SAR), and enhanced versions of SAR to achieve even higher speed. The main building block of all these architectures is the comparator, which along with a sample-and-hold circuit turns the continuous input signal into digital bits. SAR ADCs also use internal DACs, commonly formed by charge-scaling capacitive structures (CDACs), avoiding resistive reference ladders.

Even though flash architecture provides a simultaneous high-speed conversion, its performance in terms of power and efficient resolution at higher sampling rates makes it a non-ideal option for quantum computing applications [9]. On the other hand, SAR architecture has been proven to be a suitable candidate, due to its robustness against the effects caused by temperature fluctuations and its high energy efficiency. A critical part of the SAR ADC's functionality is the synchronization of its individual blocks' operations. The asynchronous operation, demonstrated in functional block diagram form in Fig. 2, can offer around 50% higher sampling rate than the synchronous one at the cost of a more complicated structure [15]. The key point in this architecture is the substitution of the sequential bit decision for the parallel execution of the SAR operations, thus reducing the time required for a complete comparison cycle, which becomes equal to the sum of the comparator decision time and the DAC settling time. An important feature of this configuration is that the additional comparator stages do not considerably affect the total power requirement, as each stage is activated once per cycle.

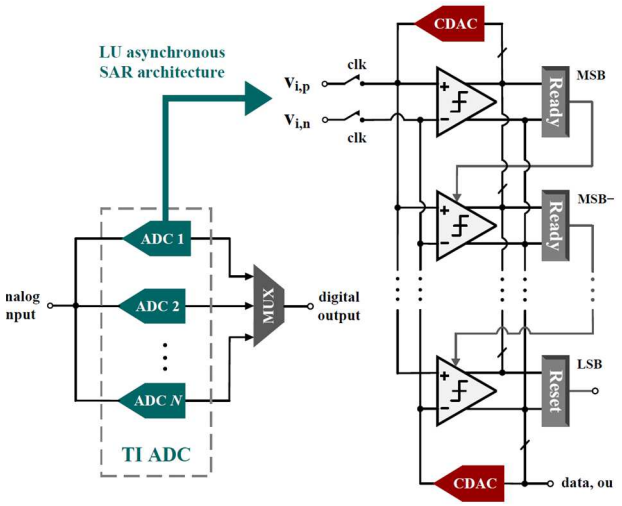

Fig. 2. Time-interleaved (TI) loop-unrolled (LU) successive-approximation register (SAR) ADC architecture.

Enhanced performance of the asynchronous SAR ADC, to meet the quantum computing requirements in terms of speed and power, can be achieved by exploiting two techniques: loop unrolling and time-interleaving sampling. Applying the loop-unrolling method, the obtained data are directly stored at the comparator, thus reducing the required iterations for decision, and simplifying the digital logic stage. Considering that the desired sampling rate is in the order of GHz, an impractical resolution reduction is required to reach such high values of speed. To maintain the desired resolution and simultaneously achieve GHz-level of sampling rate, time-interleaved (TI) loop-unrolled (LU) asynchronous SAR ADC architecture can be utilized, achieving an ideal trade-off between resolution and speed [11,12].

B. Cryogenic CMOS-based ADCs

A comprehensive guide regarding the ADC publications in the literature over the past 25 years is provided by Murmann's ADC overview table, which is available online [14]. A review of this table and the rest of the literature shows that although cryogenic ADC designs have already been proposed over the past decade, only in the last two years have detailed works been published on cryo-CMOS ADC design for quantum computing applications [10−12]. The energy diagram in Fig. 1(a) provides a clear picture of the state-of-the-art room-temperature (black/grey symbols), cryogenic (blue tringles) and cryogenic for quantum computing applications (red rhombus) ADCs over the past 25 years.

TABLE I. CRYOGENIC ADC PERFORMANCE COMPARISON

Parameter	Value			
	[12]		*[11]*	*[10]*
Temperature (K)	300	4.2	4.2	3
Technology (nm)	40 CMOS		40 CMOS	22 FinFET
Architecture	TI-LU-SAR		TI-LU-SAR	SAR
Resolution (bit)	7		6-8	N/A
ENOB (bit)	6.5		5.7	7.5
Sampling rate (MS/s)	1000		1000	400
Area (mm^2)	0.042[a]		0.045[a]	N/A
Supply (V)	1.1		1.1 (core) 2.5 (clk)	N/A
Input range (Vpp)	0.6		0.7	N/A
DNL (LSB)	<0.55		<1.5	N/A
INL (LSB)	<0.55		<1.2	N/A
SNDR@Nyquist (dB)	38.2	41.1	36.2	46.8
SFDR (dB)	>50[b]		48.5	N/A
FoM_W (fJ/c.step)	29.2[a, b]	20.9[a, b]	200[a, b]	N/A
Power (mW)	1.94[a]		10.6[a]	38[c]

[a.] ADC core + clock receiver, [b.] Typical sample, [c.] Total receiver

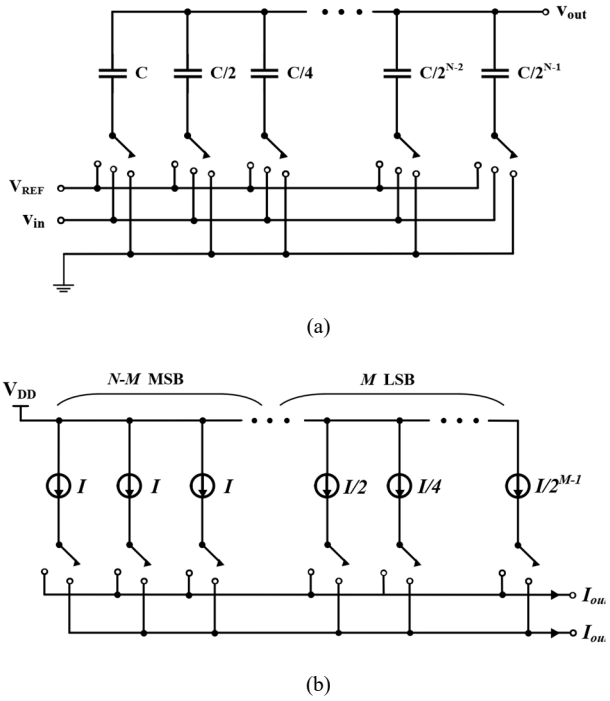

Fig. 3. DAC architectures: (a) capacitive (CDAC), and (b) segmented current steering (CS). *N* indicates the number of bits.

One of the first attempts to bring ADCs closer to the qubit temperature was based on a Xilinx Artix 7 FPGA cooled down to 15 K [13]. Despite the full programmability and low cost, the critical parameters' variation caused by the cryogenic-temperature environment, and the increased power consumption (850 mW for the whole system) render this option impractical for implementing scalable quantum computers. The situation is quite the opposite in the case of cryogenic ADCs based on nanoscale integrated circuits, where the typical power dissipation is less than 1 mW in most cases [10−12].

To perform a fair comparison, but also demonstrate the variations between different architectures, the room-temperature and cryogenic performance characteristics of the most recently published TI LU-SAR ADC in [12] are tabulated along with the corresponding cryogenic ones presented in [10] and [11], and the results are summarized in Table I. Comparing the work in [10] with the one in [12], the sampling rate, a critical feature for achieving scalability, tremendously increases (×2 times) in the case of TI LU-SAR ADC compared to the SAR ADC with the efficient number of bits (ENOB) being slightly decreased. Impressive is also the power reduction that the authors achieved in [12] compared to their work in [11], utilizing a latching comparator optimized for cryogenic temperatures. This demonstrates the critical role of the comparator in the ADC performance, guiding the future research directions towards the further optimization of this fundamental block.

III. DIGITAL-TO-ANALOG CONVERTERS

A. Architecture Techniques

DACs are utilized in both qubit control and readout operations, and for implementing SAR ADCs as mentioned in the previous Section, transforming the digitized signals to the real-world analog domain. DACs have garnered great research interest, which is reflected in the number of related publications in the literature [16−28]. Depending on the type of qubit, DC/Bias, Pulse and/or Intermediate Frequency (IF) signal DACs may be required for generating the bias DC voltages that form the qubit potential wells, gate pulse voltage and IF frequency after up modulation to perform qubit gate operations, respectively. Gate pulsing has only been discussed in [10], where a complete system-on-chip is presented, including the control and readout of a 7-qubit processor, focusing on a system level and not specifically on the DAC operation. The main difference between bias and IF-signal DACs is the required sampling rate. In the first case, it is around the qubit frequency, i.e., in the order of MHz, whereas in the second case high sampling rates in the order of GHz are required, due to the multiple IF frequencies that an up-scaled quantum control circuitry demands.

Three typical configurations used to construct a DAC are: (i) resistive-ladder, (ii) capacitive, or charge-redistribution (CDAC) and (iii) current-steering (CS) DACs. Resistive DAC is inappropriate for high-speed applications, due to the large area requirements and the low power efficiency. On the other hand, capacitive, also known as charge-redistribution, DACs constitute a fair solution, due to the advantages of high-speed operation and low power consumption. As demonstrated in Fig. 3(a), their structure is based on well-matched capacitances, whose terminal connections are adjusted through digitally controlled switches. The main advantages of this configuration, regarding its cryogenic temperature performance, are the decreased total thermal noise power of the signal (kT/C) and the limited effect on CMOS transistors, when operating as transmission gates or digital control logic [16]. The last type, and most promising

for GHz-frequency qubit control operations, is the current-steering DAC shown in Fig. 3(b).

Among the advantages of the current-steering structure, that make it appropriate for quantum computing applications, are high speed (much higher than the other two types), differential signal operation, and better linearity [36]. In addition, in many cases, even at high sampling rates, there is no requirement for an output buffer stage, thus reducing the circuit complexity. The unit element of the current-steering DAC can be arranged in both binary and unary-weighted, also known as thermometer-decoded, fashion. However, to get the best of both types, segmented CS DACs, i.e., a combination of binary and unary-weighted structures, are preferred in most cases to achieve trade-off between monotonicity and area/routing challenges. The main drawback of both charge-redistribution and current-steering DACs, which should always be carefully considered, is the capacitor and current source mismatches, respectively, caused by the cryogenic temperature environment. This is also the main source for nonlinearity effects.

B. Cryogenic CMOS-based DACs

Current-steering architecture has proven to be an ideal candidate in all types of DACs, thus dominates in the literature. A preliminary state-of-the-art survey is demonstrated in Fig. 1(b), including cryogenic CS DACs for quantum computing (red rhombus) and for other applications (blue tringles), along with the most cited room-temperature CS DAC publications (black/grey symbols) over the past 20 years.

For comparison purposes, four of the most recent and complete works of this survey are presented in Table II [19,21,24,27]. As it is expected, the requirement for higher sampling rate induces higher resolution and power demand. For cryogenic DACs used for generating solid-state qubit bias voltages and sample at a speed of MS/s, 8-bit resolution is an efficient option, while the power consumption for these specifications is in the order of some μW [19,27]. DACs used for IF signal generation purposes, where the speed is greater than 1 GS/s, 10-bit resolution is a typical choice, whereas the consumed power is about some mW [21,24]. Another important characteristic in this case is the spurious-free dynamic range (SFDR), whose value should exceed the limit of 45 to achieve IF frequency >1 GHz.

The following points should be considered, when evaluating the performance of a DAC through the characteristics tabulated above. Resolution is a critical feature for the signal conversion that should be up to 8 bits to ensure a high-fidelity drive of the qubit state [16]. Power consumption also depends on the utilized CMOS technology, thus, even though the specifications in [19] and [27] are of similar values, the power required in [27], where 40-nm technology is used, is almost double than the power consumed in [19], where the DAC circuitry is built using 28-nm technology. As long as the sampling rate concerned, the higher it is, the greater the number of the manipulated qubits are, and this is the objective for attaining large-scale quantum computing systems. The critical point is to achieve a good balance between all these characteristics, while simultaneously ensuring an efficient DAC performance, and current-steering architecture has proven to be the best choice.

TABLE II. CRYOGENIC DAC PERFORMANCE COMPARISON

Parameter	Value			
	[24]	*[21]*	*[27]*	*[19]*
Temperature (K)	3	3	10	4.2
Function	IF signal	IF signal	Bias	Bias
Technology (nm)	14 FinFET	22 FinFET	40 CMOS	28 FDSOI
Architecture	CS	CS	CS	CS
Resolution (bits)	10	10	8	8
Sampling rate (GS/s)	1	2.5	0.14	0.1
Area (mm^2)	1.61[a]	4[b]	0.0074[a]	0.04[a]
Output range (mV)	N/A	N/A	6	6.6
DNL (LSB)	N/A	2	0.18	0.64
INL (LSB)	N/A	0.5	0.61	2.96
SFDR (dB)	50	56	58	N/A
Power (mW)	1.92[a]	1.5[a]	0.0138[a]	0.0073[a]

[a.] DAC core, [b.] Total TX

IV. DISCUSSION

Control electronics for the state manipulation and readout of an upscaled number of physical qubits should meet two main requirements: (i) high speed, and (ii) low power consumption. No access to cryogenic electronic device models and dilution refrigerators of limited cooling power are at the core of the insurmountable scalability problem in the development of quantum computers. To accomplish this goal, the establishment of well-founded cryogenic transistor and passive components' models, based on contemporary advanced nanoscale CMOS technologies, is urgently needed. Nevertheless, exploiting the tools available at this point to set the foundations in the development of qubit control electronics is dominant to enable large-scale quantum computers in the future. Speed and robustness enhancement against the variations of the CMOS device characteristics, when cooled down at cryogenic temperatures, is required at this intermediate research stage. Based on that, future steps should focus on more stable structures and calibration techniques to efficiently eliminate the effects of sub-Kelvin temperatures on the CMOS circuitry until appropriate models are developed.

The up-to-date literature on the chief mixed-signal building blocks, i.e., ADCs and DACs, presented in this work demonstrates the great interest in this field and the significant leaps that have been achieved up to the present. Academic and industrial research worlds have joined forces to shape the future of quantum computing. Among the pioneers of the next-generation data revolution are names of big companies and universities around the world, like IBM, Google, Rigetti, Quantum Motion, University of Waterloo, MIT, Harvard University, University of Oxford, TU Delft and recently the University of Glasgow. The collaboration between leading groups in the field and the development of a protocol will define a common path for the quantum computing community and accelerate the evolution of scalable quantum computers.

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