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Printed n- and p-Channel Transistors using Silicon Nanoribbons Enduring Electrical, Thermal, and Mechanical Stress

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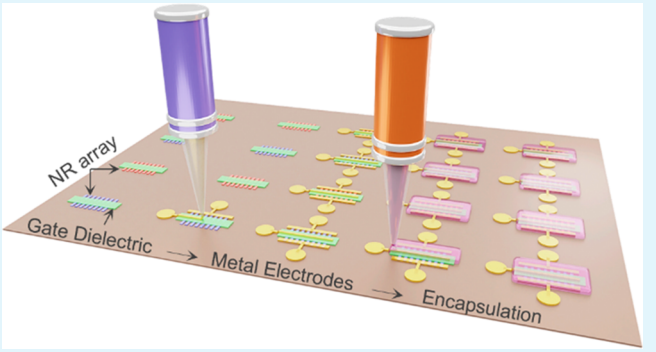
ABSTRACT: Printing technologies are changing the face of electronics with features such as resource-efficiency, low-cost, and novel form factors. While significant advances have been made in terms of organic electronics, the high-performance and stable transistors by printing, and their large-scale integration leading to fast integrated circuits remains a major challenge. This is because of the difficulties to print high-mobility semiconducting materials and the lack of high-resolution printing techniques. Herein, we present silicon based printed n- and p-channel transistors to demonstrate the possibility of developing high-performance complementary metal−oxide−semiconductor (CMOS) computing architecture. The direct roll transfer printing is used here for deterministic assembly of high-mobility single crystal silicon nanoribbons arrays on a flexible polyimide substrate. This is followed by high-resolution electrohydrodynamic printing to define source/drain/gate electrodes and to encapsulate, thus leading to printed devices. The printed transistors show effective peak mobilities of 15 $cm^2/(V\ s)$ (n-channel) and 5 $cm^2/(V\ s)$ (p-channel) at low 1 V drain bias. Furthermore, the effect of electrical, mechanical, and thermal stress on the performance and stability of the encapsulated transistors is investigated. The transistors showed stable transfer characteristics even after: (i) continuous 4000 transfer cycles, (ii) excruciating 10000 bending cycles at different bending radii (40, 25, and 15 mm), and (iii) between 15 and 60 °C temperatures.



KEYWORDS: *printed electronics, flexible electronics, transistors, silicon nanoribbons, endurance*

1. INTRODUCTION

Over the last 60 years, the miniaturization of integrated circuits (ICs) has revolutionized computing and communication capabilities. The phenomenal progress achieved through large scale integration of miniaturized high-speed devices has enabled fast digital technologies touching life in almost all traditional sectors today (e.g., health, aerospace, manufacturing, retail displays, robotics, wearable systems, etc.).[1−9] Yet, as revolutionary as this miniaturization trend has been, in its current form, the production processes it follows are inherently and unavoidably wasteful. For instance, IC fabrications rely almost entirely on subtractive manufacturing methods (sequence of photolithographic and chemical processing steps), leading to large material wastages, and high levels of anions and organic pollutants.[10−12] Such methods are not suitable for large area flexible electronics that can bend, flex, and twist. Even if advances with silicon-based technologies continue to be made, there is need for alternative technology offering resource-efficient and environment friendly routes for manufacturing electronics without losing its transformative power.

Printed electronics is rapidly changing the way electronics is manufactured and used.[13−16] With resource-efficient and low-cost fabrication of electronics over large areas (larger than the commercially available wafers) and flexible and stretchable substrates, the printed electronics is advancing several applications.[13,17−22] Efficient use of various materials also makes printing attractive in terms of lower electronic waste (e-waste) and better environment friendliness.[11−13,23−25] As a result, the printing technologies have been explored for devices such as artificial thermoreceptors,[26] touch sensors,[27] synaptic transistors,[28] energy harvesters,[29−31] radio frequency identification (RFID) tags,[32] and interconnects,[33] etc. needed in conformable and interactive electronic systems.[26,28,34] However, the nonavailability of high-performance (i.e., low power, fast speed) processing units has restricted the utility of printed electronics to low-end applications.

Transistors form the basic building blocks for any processing unit, and several research groups are working toward the

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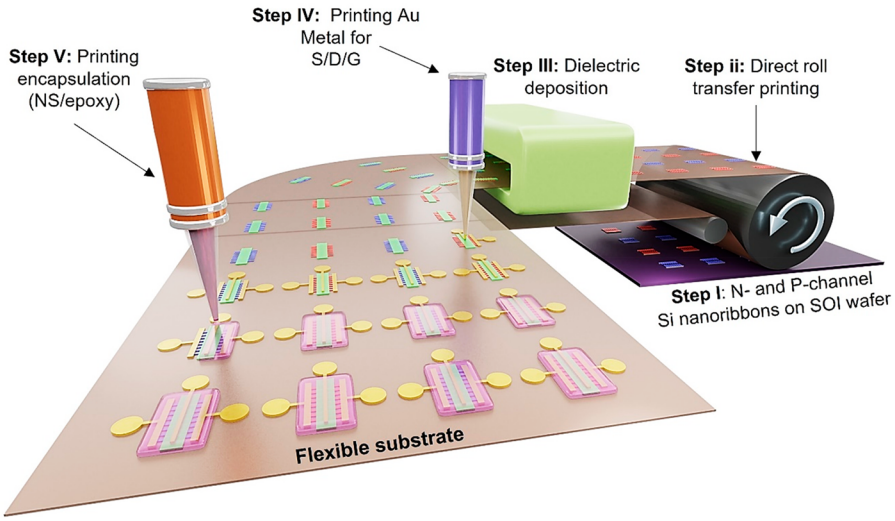

Figure 1. Schematic of the fabrication process steps for printed n- and p-channel transistors. (i) n- and p-type NRs fabricated and anchored to the donor wafer. (ii) Direct roll transfer printing of NRs on a semicured flexible polyimide substrate. (iii) PECVD deposition of SiN_x at room temperature over the transferred NRs. (iv) EHD printing of Au metallic ink over the drain/source and gate regions. (v) EHD patterned printing of NS/Epoxy encapsulant over the fabricated transistors.

development of high-performance printed transistors. For example, significant advances have been made by depositing thin films of organic and metal oxide materials and employing variety of printers such as gravure,[17,35] inkjet,[18] etc. The thin-film transistors can be lightweight, flexible, and conformal and they can be manufactured on large substrates at low-cost per unit area.[36−40] However, high operating voltages (up to 50 V), low mobility (<1 $cm^2/(V\ s)$), poor current injection, and low integration density remain challenges for organic thin-film transistors (OTFTs). The current benchmark is a flexible microprocessor based on indium−gallium−zinc oxide (IGZO) TFTs developed using conventional microfabrication processes.[37] However, due to availability of n-channel transistors only, the circuits based on this technology are more complicated and power-hungry.[41,42] Further, the obtained n-channel device mobility (<10 $cm^2/(V\ s)$) is insufficient for high-speed applications. Transfer printing of ultrathinned chips (UTCs) over flexible substrates can provide short-term practical solutions to satisfy the need of high performance, but the technology has its own limitations such as high fabrication cost, and limited flexibility.[33,43,44] To overcome these bottlenecks, printing of high carrier mobility electronic layers and the optimization of high-resolution printing technologies is required.

Driven by these challenges, our approach is to develop printed transistors on flexible substrates employing high intrinsic mobility Si nanoribbons (NRs) and a high-resolution drop-on-demand (DoD) printer. To integrate Si NR arrays, single-step direct roll transfer printing method is used which has shown potential for large area electronics.[45−47] This newly developed printing technique avoids the use of elastomeric stamps (typically employed in transfer printing) and thus, reduces the number of fabrication steps. Using the direct roll transfer approach, arrays of both n- and p-channel Si NRs are printed over flexible polyimide (PI) substrates. Next, high-resolution DoD electrohydrodynamic (EHD) printing was utilized to print Au source/drain/gate (S/D/G) metal electrodes. EHD offers excellent possibilities such as high-resolution patterning (≈1 μm) needed to reduce the channel length of transistors, substrate independent patterning, and the potential for low-cost operation.[48−50] Moreover, it shows a better compatibility with automated control, potentially leading to resource-efficient "digital manufacturing". The developed transistors show moderately high effective mobilities (n_e = 15; n_p = 5 $cm^2/(V\ s)$) at low drain bias (≈1 V). Furthermore, EHD was employed to encapsulate the printed transistors with nanosilica/epoxy (NS/epoxy) dielectric material. The encapsulated transistors showed stable response even after excruciating 10000 bending cycles at different bending radii (40, 25, 15, and 5 mm) and at both low (15 °C) and high (60 °C) temperatures. Through these proof-of-concept devices, this work provides new resource-efficient route for printed electronics and flexible low-power complementary metal−oxide−semiconductor (CMOS) logic circuits.

2. RESULT AND DISCUSSIONS

2.1. Fabrication of Printed n- and p-Channel Transistors. Figure 1 schematically shows the developed fabrication process flow of printed transistors on flexible substrates. The details of the materials and process conditions are given in the "Methods" section. The process starts with the fabrication of intrinsically high mobility Si NRs arrays on a rigid silicon-on-insulator (SOI) wafer (step i, Figure 1). The NR's dimensions were defined using conventional nanofabrication processes including photolithography and etching, as described in our previous works.[59] The selective doping step was performed using spin-on-dopant (SoD) technique on NRs arrays to realize n- and p-channel devices (see methods for details). The horizontally aligned, suspended arrays of doped NRs over SOI source wafers are then transfer printed on to flexible receiver substrates. There are different routes to execute transfer printing of NRs. In the present work, we have employed single-step 'direct roll transfer printing' method to transfer n- and p-type doped NRs (step ii, Figure 1).[46] The printing technique has shown potential for large area electronics by avoiding the use of elastomeric stamps. The use of such stamps during transfer printing methods generally leads to low transfer yield, and registration issues. The direct roll transfer printing employed here not only reduces the number of fabrication steps with respect to the conventional

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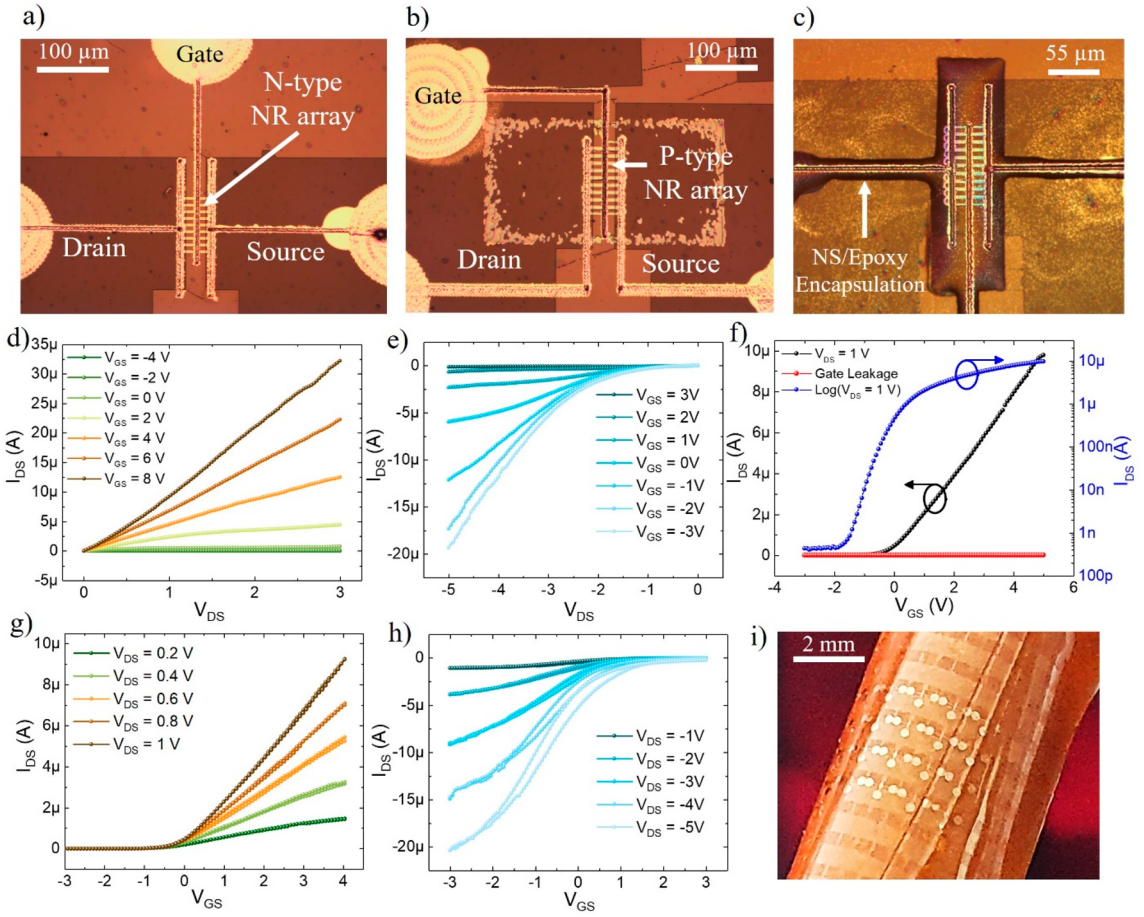

Figure 2. Electrical characteristics of printed n- and p-channel transistors. (a–c) Optical micrograph of the printed transistor (scale bar, 100 μm). (d) Output characteristics of n-channel printed transistor. (e) Output characteristics of p-channel printed transistor. (f) Transfer characteristics with V_{DS} = 1 V in logarithmic and linear scales. The graph also shows the gate leakage current. (g) Transfer characteristics of n-channel transistor with V_{DS} varying from 0.2 to 1 V with the step of 0.2 V. (h) Transfer characteristics of p-channel transistor with V_{DS} varying from −1 V to −5 V with the step of −1 V. (i) Optical picture of printed transistors while placed on a cylindrical tube.

transfer printing approach but also offers opportunity for roll-to-roll (R2R) manufacturing. In this method, suspended arrays of NRs over the SOI substrate are brought into direct physical contact with the spun semicured PI layer over the receiver substrate. The semicured PI layer helps to attain a high transfer yield. The printed Si NR arrays were then processed to realize flexible transistors. As a high-quality dielectric layer, we deposited silicon nitride (SiN_x) at room temperature (RT) using plasma-enhanced chemical vapor deposition (PECVD). Using photolithography and dry etching we then opened the regions for metal contacts on NRs (step iii, Figure 1). The doping was performed to (i) have p- and n-channel devices using single source SOI wafer, and (ii) achieve low-contact resistance metal semiconductor (MS) contacts to nanostructures. The diffusive gold (Au) metal is then printed by employing high-resolution EHD printer (step iv, Figure 1) to define S/D/G electrodes. An optimized Ar plasma treatment was performed before printing Au metal to remove any organic residues and to improve the wettability of the Au ink with the substrate. Further, we believe that the plasma treatment can help to remove any insulating layer existing on the surface of NRs and thus to achieve high quality interface between Au and heavily doped silicon. It is to note that the plasma unit is installed within the EHD printing chamber. The Au ink was cured at 250 °C for 2h to improve the conductance of the printed structures. Finally, the transistors were encapsulated by printing NS/epoxy layer using EHD printer (step v, Figure 1). The optimization of the EHD printing for Au and NS/epoxy inks is described elsewhere[26] and details are provided in "Methods" section.

2.2. Electrical Characterization of Printed n- and p-Channel Transistors. Figure 2 depicts the electrical characterization results and optical image of a typically fabricated and best performing n- and p-channel printed transistor. The statistical data from five different devices for each n- and p-channel is shown in Figures S1 and S2, respectively. The Figure 2a–c show optical images of fabricated n-channel and p-channel printed transistors. The typical channel length (L_{ch}) and width (W_{ch}) of the fabricated transistors (both n- and p-channel) are ∼5 and ∼45 μm (9 NRs of 5 μm wide), respectively. Figure 2c represents optical image of a n-channel encapsulated device. Representative output curves for n- and p-channel transistors are shown in Figure 2d,e, respectively. The data evidently shows good linearity in the output curve for n-channel devices at low drain bias, indicating that the ohmic nature of source and drain contacts. However, presence of crowding behavior in the output curve at low drain bias (n-channel) suggests the presence of an injection barrier at the MS contacts which is comparatively higher than the conventional devices (where

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Table 1. Comparison of the Printed n- and p-Channel NR Transistors with Other State-of-the-Art Printed Transistors[a]

channel material (printing method)	dielectric (deposition method)	S/D contacts (printing method)	mobility ($cm^2/(V\ s)$)	current on/off ratio	flexible	bending cycles (radius)	ref
SWCNT (inkjet)	HfO_2 (ALD)	Au (evaporation)	p-type: 10−30 n-type: 10−30	10^6	no	N/A	51
SWCNT (inkjet)	HfO_2 (ALD)	Au (evaporation)	17.6−37.7	10^4−10^7	no	N/A	52
SWCNT (aerosol)	SiO_2	CNT (aerosol)	7	10^6	no	N/A	53
SWCNT (inkjet)	PMMA (spin-coated)	GO (inkjet)	8	10^4	yes	N/A	54
IrGO (rod)	SiO_2	GO (inkjet)	4.37		yes	N/A	55
MoS_2 (inkjet)	Electrolyte (inkjet)	Cr/Au (evaporation)		10^6	no	N/A	56
MoS_2 (spin-coating)	SiO_2/Si (deposition)	Pt	7−11	10^6	no	N/A	57
SnO_2 (inkjet)	Al_2O_3 (inkjet precursor)	ITO (inkjet precursor)	13.3	10^5	yes	1000 (5 mm)	58
Si NR (transfer printing)	SiN_x (PECVD)	Au (inkjet)	n-type: 15 p-type: 5	10^4	yes	10k (45−25 −15 mm)	this work

[a]ALD: atomic layer deposition; CNT: carbon nanotubes; GO: graphene oxide; ITO: indium tin oxide; Pt: platinum; and N/A: data not available.

Table 2. Summary of the Key Performance Metrics for the Fabricated Flexible Printed n- and p-Channel Transistor Device[a]

channel type	V_{DS}	I_{on} (A)	I_{off} (A)	$I_{on/off}$ ratio	hysteresis (ΔV)	μ_{eff} ($cm^2/V\ s$)	S−S (V/dec)	V_T (V)
n-type	1 V	9 μ	400p	10^4	0.15	15	0.4	−0.2
p-type	−4 V	18 μ	200n	10^2	0.2	5	2 V	0.8

[a]The data is shown for the best obtained device for each type.

metal is defined using evaporation method under high vacuum conditions).[46] The presence of extra resistances in series degrades the transistor performance.

The critical transistor performance metrics include on-state current (I_{on}), off-state current (I_{off}), current on/off ratio (I_{on}/I_{off}), transconductance (g_m), effective device mobility (μ_{eff}), and subthreshold slope (S−S).[60] These parameters are important as they help to benchmark the transistors developed using low-dimensional materials and novel fabrication technique. Along with the performance metrics, transistor structural parameters that influence device performance include L_{ch}, W_{ch}, gate insulator thickness and permittivity, contact metal types (ohmic/Schottky), the thickness of the channel material, contact resistance (R_c) etc. The performance metrics were extracted using the transfer characteristics (I_{DS}−V_{GS}) performed with V_{DS} = 1 V for a transistor with L_{ch}/W_{ch} ratio ≈5/45, channel thickness ≈70 nm, and gate insulator thickness and permittivity of 100 nm and ∼7, respectively. Figure 2f shows the plot in logarithmic and linear scales. The measured devices showed typical I_{on} (∼10 μA)/I_{off} (<1 nA) current ratio of $>10^4$ suggesting an excellent gate-channel control. The extracted S−S from the logarithm transfer plot is 0.4 V/decade. Next, threshold voltage (V_T) was extracted using the linear extrapolation method. For this, the linear extrapolation of I_{DS}−V_{GS} graph, intercepting the I_d = 0 at x-axis (V_{GS}) gives the V_T value (−0.2 V). This was followed by the calculation of transconductance (g_m), as per eq 1 below:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} | V_{DS} = \text{constant} \quad (1)$$

The calculated peak g_m is ∼2.5 μS at V_{DS} = 1 V. Next, the field-effect (effective) device mobility was extracted using the conventional MOSFET model in the linear regime:[46,47,61]

$$\mu_{eff} = \frac{L}{W} \frac{g_m}{C_{ox} V_{DS}} \quad (2)$$

The extracted effective mobility was found to be ∼15 $cm^2/(V\ s)$. Depending on the structural device parameters such as R_c values, μ_{eff} can be underestimated or sometimes overestimated relative to the drift mobility of the channel material.[62] For instance, substantial R_c which is typical to low-dimensional materials−metal interfaces pose major challenge in understanding intrinsic charge transport properties. In past, few methods have been proposed to make μ_{eff} less dependent on these factors but none of them is sufficiently general enough to be widely adopted. Further, it is hard to extract the R_c values in the present case as widely adopted transfer length method (TLM) requires a series of transistors with different channel lengths having consistent contact and gating configurations. It is challenging to have consistent MS contact configuration to extract near-ideal R_c for printed transistors. Likewise, in this work, we have used the often-used approach to extract field effect mobility (eq 1) and compared it with the state-of-the-art printed transistors. Although the obtained mobility value compares well with the state-of-the-art n-channel printed transistors (Table 1), it is 2 orders of magnitude lower than its intrinsic value (μ_n = 1500 $cm^2/(V\ s)$) and ∼40 times lower than flexible Si transistors (≈650 $cm^2/(V\ s)$) realized using conventional microfabrication approach.[46] This could be attributed to the high R_c of the printed transistors compared to the conventionally made devices where the metal is deposited under ultrahigh vacuum conditions.

Further, transfer characteristics with V_{DS} varying from 0.2 to 1 V with the step of 0.2 V is performed (Figure 2g). As shown in this figure, there is a constant increase in the output current with increase of V_{DS} while no change in threshold voltage was observed. Like the n-channel devices, the p-channel transistors were electrically characterized under similar condition. Representative output curves (Figure 2e) clearly show nonlinearity in the output curves at the low drain bias, indicating existence of a larger injection barrier as compared to n-channel transistors. Consequently, as explained above the effect of R_c on device mobility, extracted mobility using the transfer scan (Figure 2h) is lower (5 $cm^2/(V\ s)$) than the n-channel transistors. For the n-channel devices, almost no hysteresis was observed (Figure 2g). Like n-channel devices, negligible hysteresis was observed for p-channel devices at lower V_{DS} confirming the good quality of the gate dielectric

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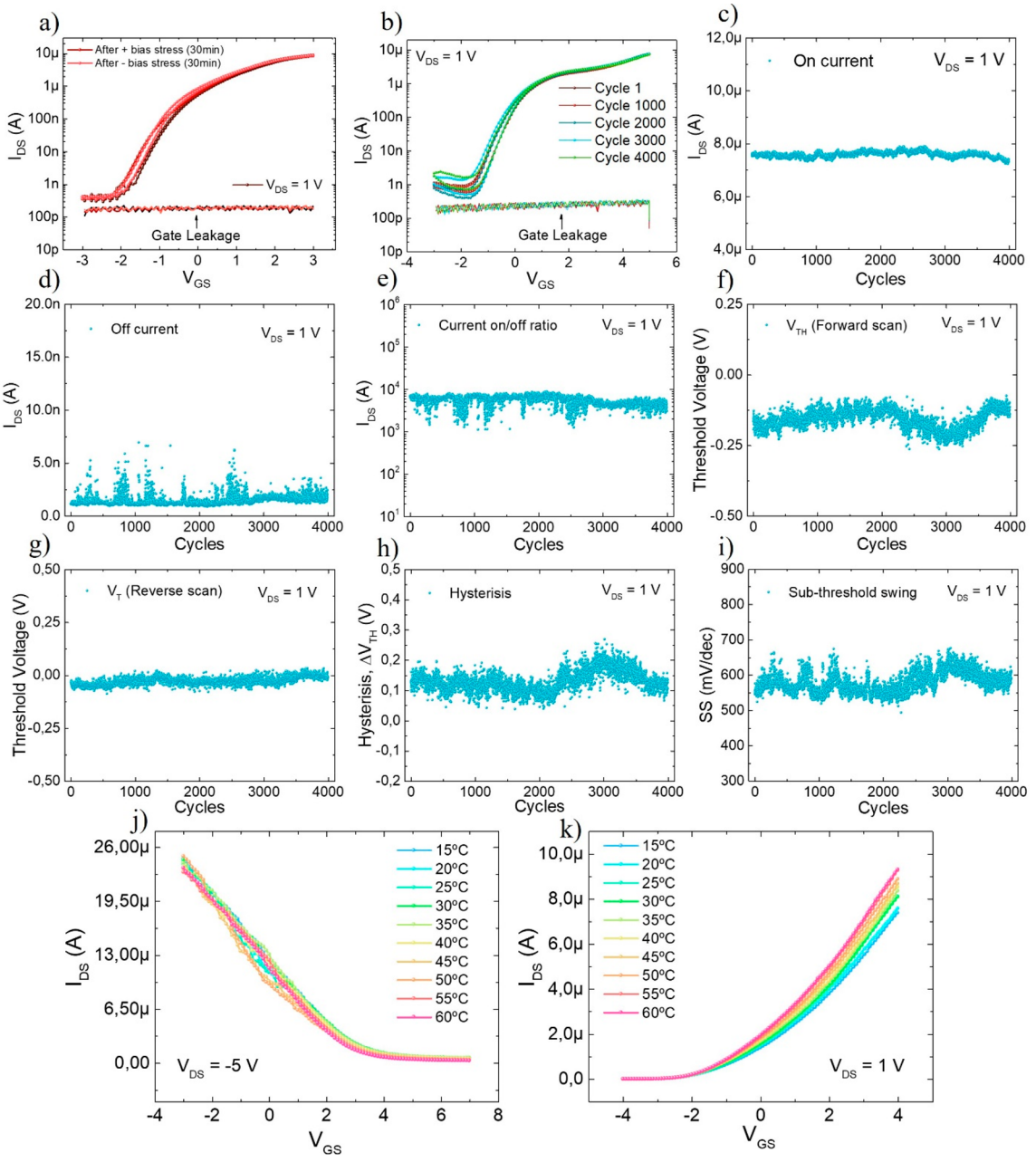

Figure 3. Electrical bias and thermal stress performance evaluation of printed transistors. a) Transfer curves with gate leakage after positive and negative gate bias stress of 30 min. b) 4000 transfer scan measurements with gate leakage at V_{DS} = 1 V. (c–i) Extracted key transistor parameters from the cyclic transfer scan regarding the device performance stability: c) on-current, d) off-current, e) current on/off ratio, f) threshold voltage (forward scan), g) threshold voltage (reverse scan), h) hysteresis, and i) subthreshold swing. j, k) Transfer scans with a temperature range of 15–60 °C with 5 °C step for both p- and n-type devices.

(Figure 2h), but at higher V_{DS} (−5 V_{DS}), the hysteresis is ∼0.4 V which is still lower than the reported nanoscale transistors.[63] There are various factors related to the hysteresis width such as device geometry (dielectric thickness, etc.), environmental conditions (temperature and humidity), and measurement parameters (gate sweeping rate, etc.).[64] The observed small hysteresis in p-channel devices could be possibly because of the charges injected onto trap sites (surface traps, interface traps and dielectric traps) at higher electrical field. The extracted performance metrics for both n- and p-channel transistors are shown in Table 2.

It is to note that the fabricated transistors (both n- and p-channel) showed some device-to-device performance variations including field-effect mobility, S–S etc. We have characterized five devices of each n- and p-channel printed NRFET, and a statistical device variation is included in Figures S1 (n-channel) and S2 (p-channel) and summarized in table S1. To improve the uniformity of device response from single batch or from different batches, many aspects need attention. First, the uniform, and controlled doping of the donor substrate need to be ensured. The doping step in this work is performed using the spin-on-dopant approach under ambient pressure which was not an ideal approach and could lead to nonuniformity in the devices. Second, highly controlled NR printing approach is needed to have uniform electronic layer. The direct roll transfer printing approach has shown very

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good transfer yield of ∼95% but there is still room for improvements. Last, the performance of printed NRFETs is influenced by the quality of metal−semiconductor contact interface and the dielectric/semiconductor interface. Because of the low dimensionality of NRs and adopted printed route to realize metal contacts, it is challenging to realize high quality contacts primarily due to the electrostatics involved at nanocontact interfaces. Currently, we are working on these aspects to further reduce the batch-to-batch performance variations of devices and will present the advances in our future works.

To evaluate the potential of the fabricated printed transistors in the development of high-speed circuits, the theoretical cutoff frequency f_T is extracted using the following equation:[65]

$$f_T = \frac{\mu_{eff} V_{DS}}{2\pi L(L + L_{ov,GS} + L_{ov,GD})} \quad (3)$$

where $L_{ov,GS}$ is the parasitic gate-to-source overlap and $L_{ov,GD}$ is the parasitic gate-to-drain overlap. Neglecting the parasitic capacitances, the f_T of n-channel transient transistor with a channel length of 5 μm and mobility of 15 $cm^2/(V\ s)$ is estimated to be more than 19 MHz, while for p-channel transistor it is 9.5 MHz which can be further enhanced by reducing the channel length and contact resistance in future optimized design. Nevertheless, it is still higher than the state-of-the-art printed transistor devices based on organics and metal oxides.[37]

2.3. Reliability Studies of Printed Transistors. *2.3.1. Electrical Bias Stability.* Stable transistor operation is required for any practical application. The stability of device operation could be affected during continuous gate electrical bias stress, temperature change, mechanical loadings, etc.[60,66] Further, exposure of active channel to ambient atmosphere could lead to interactions with water and oxygen molecules, and thus to the charge trapping at the surface states, which eventually lead to surface band bending and shift in the threshold voltage, on-current, etc.[28] These factors are more dominant in nanoscale transistors due to the high surface to volume ratio of nanomaterials. These drawbacks could be carefully utilized to develop novel devices such as printed synaptic transistor-based electronic skin allowing robots to feel and learn;[28] they should be minimal when it comes to ICs. Therefore, we encapsulated the printed transistors using NS/epoxy of thickness ∼2−3 μm to reduce the influence of environment on NR channel (Figure 2c). To evaluate the stability of printed transistors, we performed the following electrical tests: (i) gate bias stress, (ii) continuous device operation up to 4000 cycles, (iii) transfer scans at wide range of temperatures, (iv) and transfer scans to evaluate the degradation of devices performance after applying stringent mechanical bending loadings. The results from the first three stability tests are shown in Figure 3. First, positive bias stress (PBS), and negative bias stress (NBS) stability tests were performed (Figure 3a). The transfer scan was performed under no stress condition by sweeping the V_{GS} from −3 to +3 V at a fixed 1 V_{DS}. Both for PBS and NBS test, transfer scans were performed immediately after applying the bias for 30 min. As shown in Figure 3a, the printed transistors under NBS and PBS exhibits negligible drift of the transfer curves, and threshold voltage shifts (ΔV_T) after 30 min stress time. The presented data hints presence of a high-quality of deposited gate dielectric, gate dielectric (SiN_x)-semiconductor (Si NR) interface of the fabricated transistor and no influence of ambient condition on the performance degradation. This is critical because poor interface quality could lead to V_T shift and thus, changes in the I_{on} of the device.[60] In our previous works we have confirmed the high electrical quality of the RT deposited SiN_x as gate dielectric.[59] However, unlike the previous case where conventional manufacturing process was adopted, in the present case all printed route is employed to also deposit the metal tracks which can bring additional challenges. For instance, the RT deposition could lead to a porous dielectric layer and thus, there is a possibility of the liquid printed Au ink, over the deposited SiN_x film, to flow through the pores during the curing process and short circuit the channel with the printed top gate. If not short-circuit, then such infiltration of Au ink inside the dielectric could also lower the effective thickness of the dielectric leading to lower breakdown voltages.[58] To have a good quality dielectric layer, we performed the annealing step at 250 °C for 2h in a conventional oven before printing the top-gate electrode. The annealing time and temperature were chosen in accordance with the curing conditions of printed Au ink. The excellent gate coupling and gate bias stability seen in the presented results hints that the deposited room temperature SiN_x after thermal annealing is dense enough to prevent the ink from infiltrating.

To further confirm the high stability, we have carried out electric bias stress where the transfer scans were performed continuously up to 4000 cycles (>24 h). The I_{DS} was monitored by sweeping the V_{GS} from −5 to +5 V (forward voltage sweep) and from +5 to −5 V (reverse voltage sweep) at a constant V_{DS} = 1 V (classified as one stress cycle). This is because the presence of any hysteresis due to charge trapping can further provide information on the quality of interfaces and dielectric. Figure 3b shows five transfer scans corresponding to cycles 1, 1000, 2000, 3000, and 4000. From this data it appears that the device remained stable when they were operated for more than a day. To have further insights into all 4000 cycles, the performed transfer scans were used to extract the key transistor performance metrics, namely, I_{on}, I_{off}, $I_{on/off}$ ratio, hysteresis (from the V_T value of forward and reverse scan), and S−S. Throughout the 4000 electrical cycles, the I_{on} (Figure 3c) showed stable values (change of ∼4%); however, few cycles have shown significant increase in I_{off} by 100% (Figure 3d) leading to a decrease in I_{on}/I_{off} (Figure 3e) ratio to $\approx 10^3$ for those particular cycles. However, on average, only 28% decrease in the I_{on}/I_{off} current ratio was observed.

Next, hysteresis (Figure 3h) is calculated based on the difference in V_T value for forward (Figure 3f) and reverse (Figure 3g) transfer scans. For forward scan there is small V_T shift (±0.1 V) with the stress time whereas reverse scans showed negligible V_T shift. This value is lower, when compared with the reported transistors-based metal oxides.[60,67] Using the V_T values, a maximum of ∼25% change in hysteresis values was obtained. Finally, S−S values were obtained from the subthreshold region of the transfer curve and plotted in Figure 3i. The data shows ∼8% change in S−S value after 24 h of continuous operation.

In addition to the electrical stress, nanoscale transistors are known to be susceptible to thermal stress.[68,69] To evaluate the performance degradation while varying the ambient temperature, we performed transfer scans in forward direction (−4 to +4 V_{GS}) for n-channel (Figure 3j) and +7 to −3 V_{GS} for p-channel transistors (Figure 3k) at different temperatures (15 to

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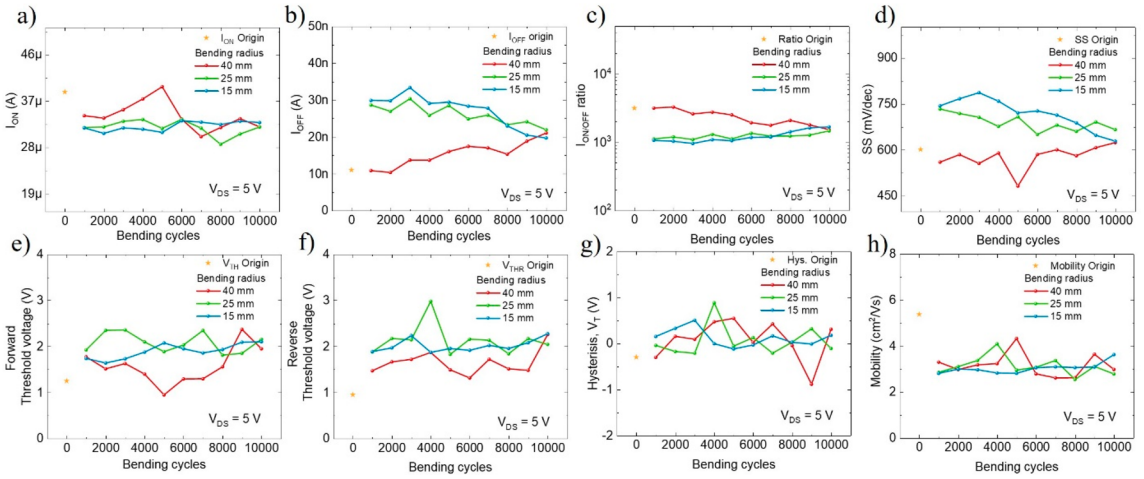

Figure 4. Extracted transistor parameters before (data shown for zero bending cycle) and after mechanical bending at various radii (from 40 mm to 25-, 15- and 5 mm). a) on-current, b) off-current, c) current on/off ratio, d) Subthreshold swing, e) threshold voltage (forward scan), f) threshold voltage, g) Hysteresis and h) mobility.

60 °C with a step of 5 °C). The I_{on} of the device (n-channel) shows slight but consistent increase in values with temperature increase. Thanks to the PI substrate, which has a very wide operation temperature range, the stable electrical performance was observed. The Si NRs as semiconductor channel and SiN_x as dielectric can also endure the experimented temperature range. The slight increase in the on-current of the n-channel device with increasing temperatures is owing to the presence of charge injection barrier at the MS interface. At higher temperature, the charge carriers acquire more kinetic energy to cross over the present barrier at the MS interface.[68,69] Interestingly, despite observed increase in the on-current, there is no change in V_T values, which further confirms the high quality of dielectric and semiconductor-dielectric interfaces. For p-channel transistors, there is no change in I_{on} as well as V_T.

The performance degradation of devices was also observed under mechanical loadings, as flexible ICs need to remain stable, while under bending/twisting conditions. As shown in Figure 2i, the free-standing flexible printed transistors can be conformably placed on cylindrical objects such as Lab Vials etc. Static direct current (dc) measurements were carried out after 10000 bending cycles at different bending radius (ranging from 40 to 15 mm). The electrical characteristics after bending up to 10000 cycles (carried out after every 1000 cycles) at each bending radius are shown in Figure S3 (transfer curves) and Figure S4 (gate leakage). Like electric bias stability, the performed transfer scans were used to extract the key transistor performance metrics and shown in Figure 4. It is to note that the device performance metrics before bending is also displayed in the Figure 4 (data at zero bending cycle). Up to 7000−8000 bending cycles performed at 40 mm bending, the extracted data shows some variations. Such a small variation in extracted data could be attributed to the experimental errors arising from the placement of metal probes as measurement are performed after every 1000 bending cycles. Under ambient conditions, it is highly challenging to achieve exactly same interface quality between metal probe tips and the printed metal pads. However, after 8000 bending cycles at 40 mm radius, it is evident that the device showed small decrease in I_{on} (Figure 4a) and slight increase in I_{off} (Figure 4b). This leads to a small decrease in the I_{on}/I_{off} ratio (Figure 4c) i.e., down from 3×10^3 to $\sim 2 \times 10^3$. After 8000 bending cycles, the increase in I_{off} could be due to the deterioration of SiN_x layer after bending induced stress. This can be further confirmed by the SS (Figure 4d) and hysteresis (Figure 4g) trend. There is increase in both SS and hysteresis after the device has undergone bending at 40 mm. Because of the deterioration of the dielectric gate, we assume that charges start to leak from gate electrodes onto trap sites (surface traps, interface traps, and dielectric traps). Further, after performing similar number of bending cycles at lower radius (25, and 15 mm), the I_{on} further decreased and the I_{on}/I_{off} ratio reduced to $\approx 10^3$. The large reduction in device on-current after bending at lower bending radii (i.e., 25 mm and 15 mm) could be because of the strain experienced by the channel (Si NRs) as there was no further reduction in SS. The mechanical bending and the resulting strain are known to affect the semiconducting material's band structure, which affects the effective mass and hence the mobility of the charge carriers.[70,71] The change in the mobility has a direct effect over the source current of the transistor. The peak values of the device mobility after every 1000 cycles of bending were obtained for each bending radius (Figure 4h). It is evident from this set of data, the mobility decreased to around 3 $cm^2/(V\ s)$ (from 5 $cm^2/(V\ s)$ before bending). Nevertheless, the device operation was preserved despite the small decrease in the I_{on} and mobility.

Two of the straightforward approaches to minimize the impact of strain on flexible devices are to (i) minimize the substrate thickness and (ii) place the active electronic layers at neutral plane axis by using suitable encapsulation. Applying the first condition, taking the substrate thickness of ~30 μm (including printed NS/epoxy), the strain at bending radii as low as 15 mm is minimized (~0.1% at 15 mm bending).[72,73] Further, the device stability was enhanced by exploring the second condition via printing a patterned encapsulation layer on top of the active channel and electrodes on the transistors. The deterioration of nanoscale device performance (large hysteresis in case of transistors) is expected when they are exposed to ambient environment mainly due to the infusion of humidity and/or adsorption of oxygen molecules.[61,63,64] The solutions that have been explored to develop hysteresis-free devices include encapsulation and deposition of conformal dielectrics.[64] The encapsulation layer can also enhance the

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mechanical endurance of the device by allowing the positioning of the most critical device layer in a neutral mechanical plane and also preventing the delamination of electronic materials. The delamination issue is more critical when inkjet printing is used to define the metal electrodes. The inkjet-based printed metals make heterogeneous contact interfaces and may experience the thermoelastic and mechanical stresses due to thermal mismatch,[74] and elastic modulus mismatch respectively.[75] While typical temperature conditions during device operation are low, high-temperature processing may be required during device fabrication, to cure the PI or to sinter the metallic Au ink (~250 °C). We experienced the delamination of the printed metal pads for nonencapsulated devices when slight mechanical bending was applied (even when unintentionally applied while peeling off from the carrier glass substrate). As a result, we could not compare the nonencapsulated and encapsulated devices. Nevertheless, after encapsulation no delamination of metal pads was observed. Such a device configuration enables high flexibility along with stable electrical properties by bringing the devices at the neutral mechanical plane and prevents the device from experiencing any strain induced variations during cyclic bending. In the present case, the thickness of the printed dielectric is around 2−3 μm. Further increase in the thickness could possibly enhance the device stability and further reduce the variation of the output under bending conditions as shown in Figure 4.[76]

3. CONCLUSIONS

In summary, we have presented a printed route for development of high-performance n-and p-channel transistors on a flexible substrate. A roll-to-roll (R2R) compatible direct roll printing technique was employed to transfer silicon nanoribbons (Si NRs) and realize high mobility electronic layers from them. Instead of using the conventional metal deposition steps (photolithography, metal deposition and lift-off etc.), we used high resolution electrohydrodynamic based jet printing to deposit diffusive Au metal contacts for the first time on Si NRs. The scaled n-channel devices show high drain current and on/off ratio at small V_{DS} = 1 V. The investigated DC performance of transistors exhibits excellent electrical, thermal, and mechanical stability. Particularly, mobility of the devices remained stable after 10000 bending cycles at each bending radius of 40, 25, and 15 mm. In addition, the temperature-dependent dc measurements performed between 15 and 60 °C, demonstrate the stable device performance under extreme environments. Thus, the printed devices could provide a new route for the development of flexible, and robust complementary metal−oxide−semiconductor compatible printed logic circuits.

4. METHODS

4.1. Silicon Nanoribbon Fabrication. The active channel of the printed transistors (i.e., Si NRs) are fabricated using a commercial silicon-on-insulator (SOI) wafer with a 70 nm thick Si (100) layer over 2 μm of buried oxide (B_{OX}) purchased from the University Wafer, Inc. The as-received wafer first undergoes standard cleaning process (i.e., sequential ultrasonication in acetone, isopropyl alcohol (IPA), and deionized (DI) water for 5 min each). After cleaning, the lateral dimensions of NRs are defined following conventional photolithography and etching processes. First, S1805 photoresist is spun at 4000 rpm for 30 s followed by soft baking at 115 °C for 1 min. The resist is exposed to UV light through a photomask defining NRs array after developing in Microposit MF-319. Each NR is 55 μm in length and 5 μm in width (9NR in an array). The wafer is then laterally dry etched on the exposed regions by reactive ion etching (CHF_3/O_2, 50 sccm, 55 mTorr, 5 min). After the Si NR arrays are defined, the resist is removed, and 250 nm thick SiO_2 is deposited using PECVD. A doping mask is patterned on the deposited oxide by dry etching, resulting in a 5 μm (undoped) channel length pattern on the NRs. The doping step is performed using spin-on dopants (SOD). n-Type doping is performed by diffusing phosphorus (Filmtronics, P451) at 1050 °C on the drain and source regions, whereas p-type doping is carried out by diffusing boron using (Filmtronics, P451) at 1050 °C. To achieve printable NRs arrays, the wafer is dipped on a buffered oxide etchant (BOE 5:1) to etch the mask and the underlying oxide. This results in suspension of the fabricated NRs anchored on the two extremities.

The nanoribbon (NR) structure has been selected here as it leads to higher the transfer yield, it is faster to underetch the NR (in width direction), and hence the overall process can be faster. The frame structure plays a critical role in defining the transfer yield particularly when it comes to transfer of nanoscale structures onto flexible substrates.[77] The optimization study of the dependency of Si frame architectures on the transfer yield has been demonstrated in past works, where the resultant transfer yield was found to be the highest for structures with the frames that have densely spaced strips with 1:1 spacing ratio (NR width/NRs spacing).[77,78] The aim of selecting multiple Si NRs connected in a single frame (single array) is to enhance the device on-current and reduce the device-to-device performance variation which is critical for realizing high performance transistors over large area.

4.2. Direct Roll Transfer Printing of Si NRs. The NRs are transfer-printed on to a flexible polyimide (PI) substrate using a custom-made direct roll setup. First, a layer of spin-on polyimide (PI-2545 from HD microsystems) is spun over a PI sheet of 25 μm thickness at 2000 rpm for 60 s. The spun PI is semicured at 120 °C for 2 min leading to a sticky adhesive layer. The prepared NR donor substrate is then placed to the roll printing setup (at the planar stage), and the PI substrate is placed on to the roller and brought into a direct physical contact with the donor substrate. This resulted into the detachment of NRs from the anchor points and lead to transfer on to the flexible PI substrate. The transfer process is completed by fully curing the spun PI at 250 °C for 2 h enhancing the adhesion of the NRs to the substrate.

4.3. Electrohydrodynamic (EHD) Printing. The PI substrate with printed NRs is gently attached on to a glass carrier substrate to have a flat and smooth surface. This is critical for EHD printing systems as the nozzle is brought in proximity of the substrate surface (<40 μm). Significant variation in the surface topography of the substrate will lead to variations in the nozzle−substrate separation distance and this, changes the effective electric field between the nozzle and substrate. This will have an impact on the amount of ejected ink and in an extreme case (±35 μm) the nozzle might touch the substrate and get broke. Before printing, a thermal treatment is performed at 120 °C to remove any remaining organic contaminant, followed by 1 min of plasma treatment inside (in situ) the high-resolution EHD printing system. The metal electrodes (drain/source/gate) were defined by printing five layers (passes) of commercial gold ink (CAu-2000 from ULVAC inc.). The ink is then cured at 250 °C for 2 h. The printing parameters are as follows: 75% sign wave, 300 V amplitude, 0 dc bias, 90 Hz frequency and stage speed of 0.5 mm/s. The device is finalised by printing the encapsulation layer based on a nanosilica/epoxy (NS/epoxy) dielectric ink from UTDots, Inc. The printing parameters used to print the dielectric ink are 50% sign wave, 250 V amplitude, 0 dc bias, 300 Hz frequency and stage speed of 0.75 mm/s. The encapsulation is cured at 150 °C for 30 min.

4.4. Electrical Characterization (Also Describing the Mechanical and Peltier System). The electrical characterizations of the fabricated printed transistors were conducted using a Cascade Microtech Autoguard probe station connected to a semiconductor parameter analyzer (B1500A, Agilent) in dark conditions. The performance stability under wide temperature range (5−50 °C) was performed by placing the sample with devices on a Linkam PE120

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Peltier system. The mechanical bending stress was applied on the sample using a commercial setup (Yuasa System DMLHP-TW).

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsami.2c20569.

Statistical data obtained for printed n-channel transistors from 5 NRFET devices: a) threshold voltage; b) Ion/off ratio, c) subthreshold swing; and d) peak field effect mobility. Statistical data obtained for printed p-channel transistors from 5 NRFET devices: a) threshold voltage; b) Ion/off ratio, c) subthreshold swing; and d) peak field effect mobility. Table S1 shows key performance metrics summarised for the fabricated flexible printed n- and pchannel transistor device. The statistical data (mean and standard deviation) is shown for each type of device. Transfer characteristics of the n-channel transistor performed after every 1000 bending cycles up to 10000 cycles: (a) bending at 40mm radius, (b) bending at 25mm radius, and (c) bending at 15mm radius. (PDF)

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Notes

The authors declare no competing financial interest.

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