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Growth of type I superlattice III-V heterostructure in horizontal nanowires enclosed in a silicon oxide template

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ABSTRACT

Template assisted selective epitaxy (TASE) offers an attractive monolithic integration route for III-V semiconductors on Si, benefitting from reduced defect density and versatility in its employment to create various electronic and photonic devices. This work achieves compositional and morphological control of lattice matched InGaAs quantum wells embedded in a horizontal InP nanowire grown directly from a Si seed and of the respective heterointerfaces. A series of growth experiments introducing variations of the precursor switching sequence in the growth recipe, and a subsequent scanning transmission electron microscopy and energy dispersive X-ray spectroscopy analysis, were employed to create and characterize a type I superlattice enclosed in a silicon oxide template.

1. Introduction

Owing to their direct band gap, III-V semiconductors form a well-established material class for light generation and absorption, finding one of their main applications in the transmission and processing of information [1]. The miniaturization of active optical components on silicon (Si) has raised interest in photonic circuitry for short range interconnects using light for instead of traditional electric signals [2–4]. The most mature integration routes for III-V semiconductor material on Si substrate involve the transfer of the grown crystal from a lattice matched substrate onto Si. Already employed in industry, these integration routes bypass the issue of lattice mismatch between III and V and Si but become difficult to implement at 8'' wafer sizes [5–7]. Conversely, any monolithic route involving the direct growth of III-V semiconductor material on Si has to contend with lattice mismatch between the Si substrate and the epitaxially grown III-V layer as a source of defects [8]. Simultaneously, the monolithic route allows for direct and precise integration of III-V material independently from substrate wafer size.

Template assisted selective epitaxy (TASE) is a versatile and CMOS-compatible method for the monolithic integration of III-V semiconductors on Si. It allows the fabrication of microstructures of a wide range of shapes and materials without detrimental defects [9–11]. It can represent a single solution for the integration of all major photonic components [12,13] such as, photodetectors [12,14], emitters [15,16], modulators, and waveguides. While TASE structures grown with a single growth facet have been reported on III-V substrates [17,18], a multi-faceted end surface is the most common situation for structures grown on Si [9,11,19–21]. This is not inherently an issue for binary III-V microstructures. It, however, leads to loss of composition control in ternary III-V systems [22], and complicates the fabrication of heterointerfaces [14] and process reproducibility.

This work builds upon the research conducted in our laboratory [14] regarding the creation of PIN photodiodes. At that time, the various heterointerfaces present in the wire, particularly those defining the intrinsic region, were identified as an issue that, if solved, would increase device performance. Therefore, we aimed to achieve compositionally sharp single facet heterointerfaces. Taking the impact of the diffusion mechanisms inside the template into account [20], the growth of thin heterolayers of alternating III-V compounds is explored. A method to improve the heterointerfaces in terms of morphology and compositional sharpness is developed, setting a basis for the direct integration of III-V superlattices on Si.

The InP/InGaAs heterointerface, grown with metal organic chemical vapor deposition (MOCVD) is studied. Here, four chemical elements

Abbreviations: TASE, template assisted selective epitaxy; MOCVD, metal organic chemical vapor deposition; STEM, scanning transmission electron microscopy; EDS, energy dispersive x-ray spectroscopy; SOI, silicon on insulator; FIB, focussed ion beam.

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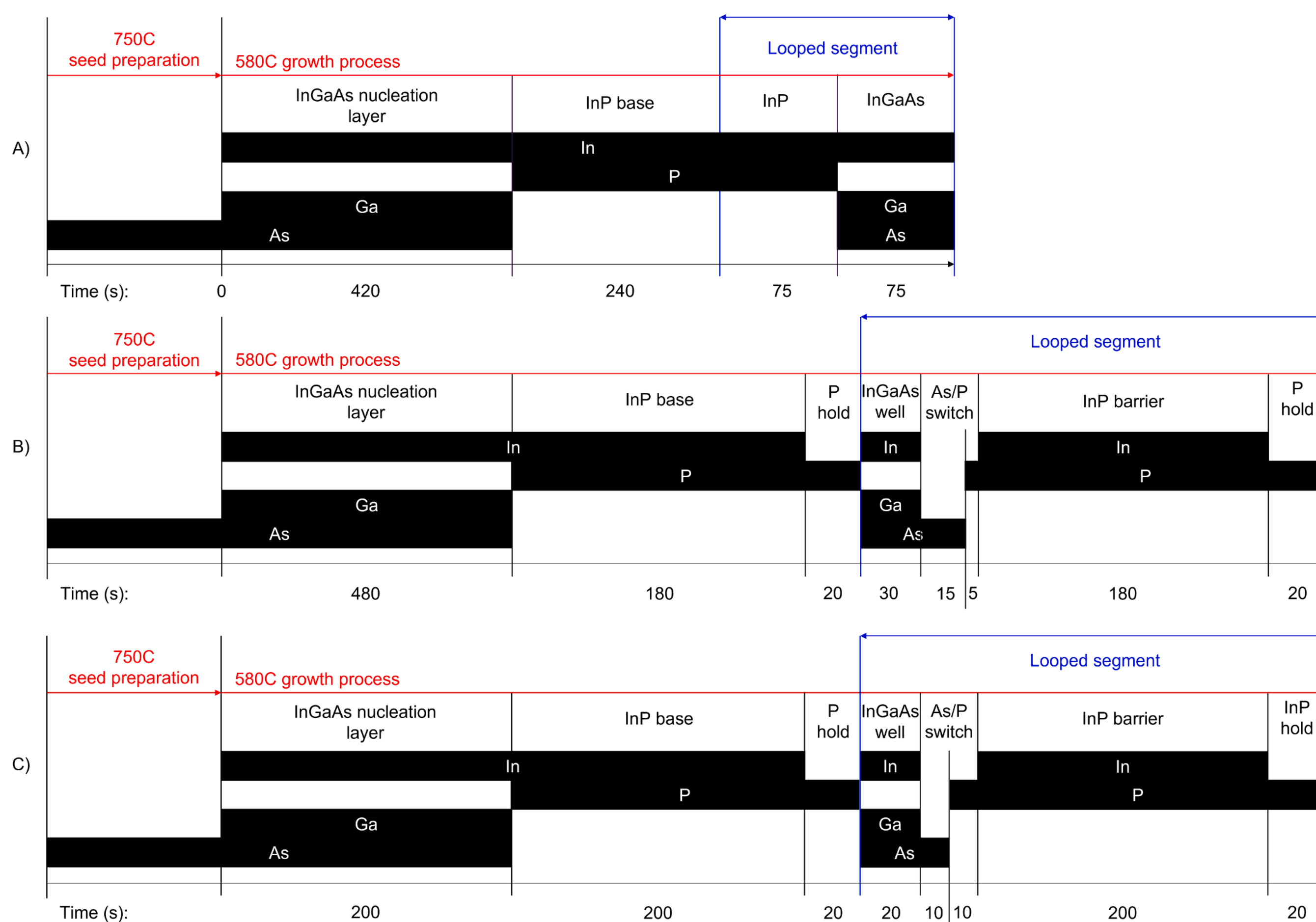

Fig. 1. Precursor switching sequences used in this study The dark blocks correspond to the introduction of the respective precursors into the reactor. The process temperature is shown in red, clearly showing the two temperatures employed: the 750 °C oxygen desorption step and the 580 °C growth process. The looped segments are highlighted in blue, and the length of each step is specified at the bottom of each sequence. A) Sequence used to study composition bleed through the heterointerfaces due to diffusional effects. B) Sequence used to perfect composition control in the nanowires. V-group precursor hold segments are introduced at every material layer switch after the first InP segment. C) Sequence used in the growth of vertical heterointerfaces. The main difference with (B) is the P/As switch sequence after the InGaAs growth step, which employs a shorter As hold and a longer P pre-flow.

have to be switched during the growth process. The quality of the III-V material and the various interfaces is assessed by scanning transmission electron microscopy (STEM) and energy dispersive X-ray spectroscopy (EDS).

2. Nanofabrication and growth

Substrates were prepared from a ⟨001⟩ silicon-on-insulator (SOI) wafer with a Si device layer thickness of 220 nm. The TASE templates were designed so that the growth direction of the III-V material coincided with the in-plane ⟨110⟩ direction of the device Si crystal. The results from experiments on this substrate were then used on a ⟨110⟩ SOI wafer with a 70 nm-thick device Si layer: the nanowires were defined with a growth direction parallel to the in-plane ⟨111⟩ direction.

2.1. Template fabrication

The shape of the microstructures comprising the individual nanowires and Si seeds was defined on a spin-coated layer of hydrogen silsesquioxane (HSQ) negative resist using e-beam lithography. The Si parts not covered by HSQ after development were etched away using hydrobromic acid (HBr) inductively coupled plasma (ICP) etching. The resulting Si structures of 50 nm to 500 nm width were covered with a 100-nm-thick atomic layer deposition (ALD)-grown silicon oxide (SiO_2) layer.

The position and size of the openings in the SiO_2 layer was defined on a spin-coated layer of CSAR62 AR-P 6200.09 (AllResist) by e-beam lithography. After development, the substrate was etched using reactive ion etching (RIE) down to the Si device layer. HBr-ICP etching was then employed to selectively remove the device-layer Si directly below the template opening.

The device-layer Si is laterally etched using a 2,5%$_{v/v}$ tetramethylammonium hydroxide (TMAH) aqueous solution at 80 °C, leaving a tilted (relative to the growth direction) {111} Si facet as a seed interface inside a hollow SiO_2 template. Pre-growth surface treatments include a cleaning step with a sulfuric acid – peroxide 2:1 mixture to remove any organic contamination, followed by a 10 s dip in a diluted hydrofluoric acid (HF) aqueous solution to remove the native SiO_2. This allows for the nucleation of the III-V material on the exposed Si surface in the MOCVD reactor.

2.2. Material growth

All nanowires discussed in this work were grown in a 3x2″ MOCVD system operating at 60 Torr using trimethylindium, trimethylgallium, *tert*-butylarsine, and *tert*-butylphosphine, transported in a hydrogen flow, as precursors for the III- and V-group elements. The vertical growth reactor is equipped with a showerheadand a rotating susceptor.

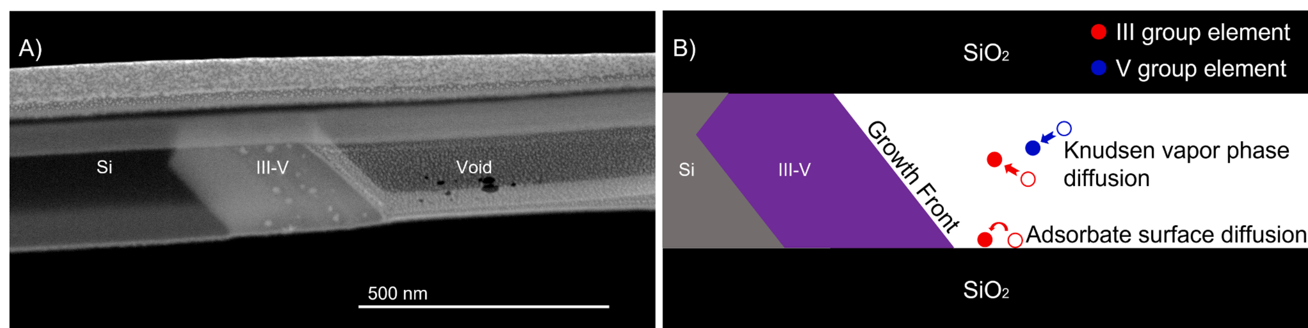

Fig. 2. A) SEM image of a TASE-grown nanowire taken during FIB thinning. The sample is tilted 52° with respect to the ⟨0 0 1⟩ vector defining the wafer plane. The dots visible in the area marked as void are due to platinum deposition employed during FIB preparation. B) Schematic drawing of the various diffusion mechanisms available to III and V precursors, colored in red and in blue respectively.

All the samples were grown on a chip size of 2 cm × 2 cm. The V/III ratios were 45 and 234 during InGaAs and InP deposition respectively, and the In molar flow ratio during InGaAs deposition was 0.3.

2.2.1. *Heterostructure growth*

A first set of samples was grown using the precursor switching sequence illustrated in Fig. 1.A, where each precursor flow is identified by the corresponding III or V species. The dark blocks illustrate the elements introduced in the reactor at any given time. A first high temperature oxygen desorption step takes place at 750 °C in a mixed hydrogen and arsenic atmosphere. Then, the substrate is cooled down to the growth temperature of 580 °C, starting with the deposition of an InGaAs nucleation layer that was chosen as it is lattice-matched to the following InP base layer. A sequence consisting of a series of precursor switches, intended to form thin heterolayers of InGaAs and InP, follows and is repeated twice.

It is important to consider the effect of the template geometry on the diffusion of the precursors towards the growth front when optimizing the growth recipe in selective area growth and TASE. A scanning electron microscopy (SEM) image taken during focused ion beam (FIB) thinning of a nanowire cross section (Fig. 2.A) serves to illustrate a typical geometry with the Si seed on the left and the TASE-grown III-V wire in the center. The precursor diffusion routes are shown schematically in Fig. 2.B, indicating that III-group elements (red) can diffuse both in the vapor phase, through Knudsen diffusion, and inside the confined space of the template on the SiO_2 surface as adsorbates. This means that one slow extra diffusional route is available for them compared to the fast vapor phase diffusion mechanism that is predominantly available to the V-group precursors and atoms [20] represented in blue in Fig. 2.B. These different transport channels can lead to loss of interface sharpness and composition control of III-V heterostructures and need to be accounted for.

2.2.2. *Heterointerface optimization*

A modified precursor switching sequence is introduced in Fig. 1.B, with the aim to better control the heterolayer thicknesses and heterointerface definition. This is implemented by minimizing the compositional gradient through the interfaces themselves. By employing hold steps additional time becomes available to the III group precursors to diffuse to or escape from the growth interface. More specifically, each InP deposition step is followed by a 20-s-long hold of the P precursor flow. Conversely, each InGaAs deposition step is followed by stopping the flow of group III precursors to the reaction chamber for 15 s. A subsequent InP segment is preceded with a 5 s P flow, to favor the exchange of the As precursor in the template. A further objective of this experiment was to create a type I superlattice consisting of InGaAs quantum wells inside the InP layer. Therefore, the final growth section was repeated twice by adding 30-s-long InGaAs deposition and 200-s-long InP steps.

2.2.3. *Vertical heterointerfaces*

A final goal is to substitute the ⟨0 0 1⟩ SOI wafer (220 nm thick device layer) with a ⟨1 1 0⟩ SOI wafer (70 nm thick device layer) for the growth of vertical quantum wells. Ritter et al. demonstrated a high yield of

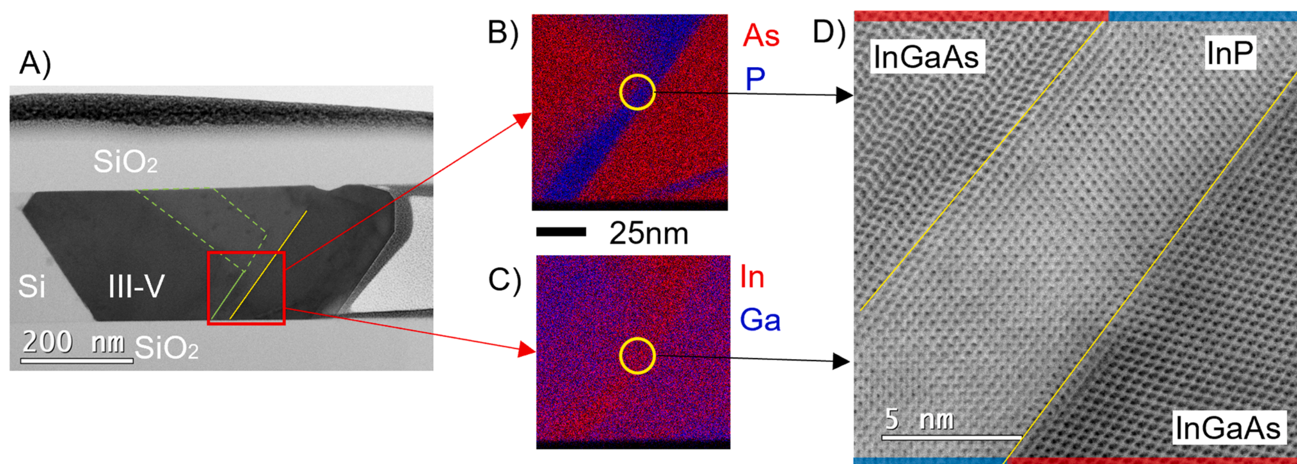

Fig. 3. STEM image and EDS maps of a lamella cut from the growth experiments carried out with the recipe shown in Fig. 1.A. A) Overview bright field STEM image of the nanowire. The growth front for the InGaAs layer is highlighted in green, with the dashed line indicating one of the (tilted) {1 1 0} planes and the solid line indicating the {1 1 1} plane. The {1 1 1} growth front for the InP layer is highlighted in yellow. B) EDS map of the region highlighted by the red square in (A), red As, blue P concentration. C) Corresponding EDS map with red In, blue Ga concentration. D) High-resolution image of the heterostructure region.

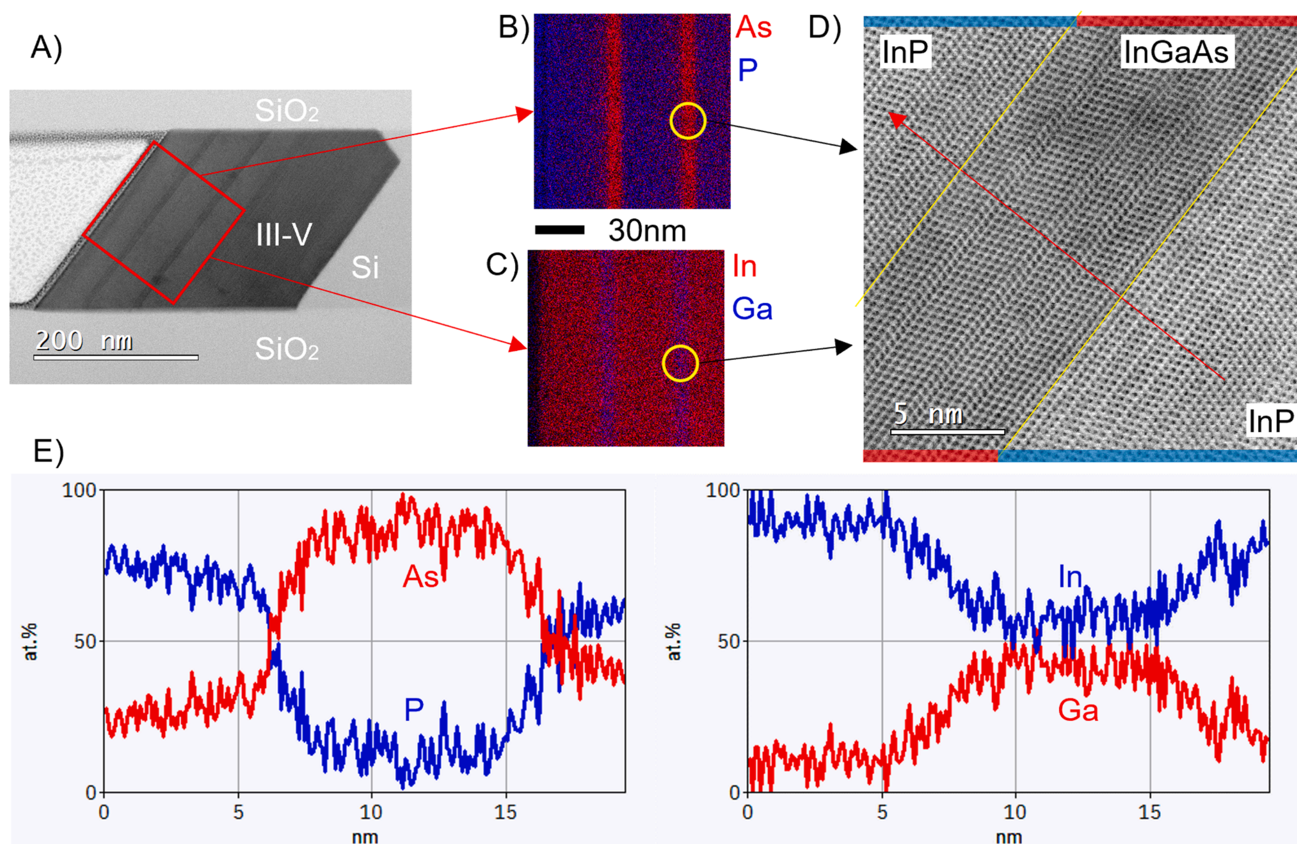

Fig. 4. STEM image and EDS maps and line scan of the growth experiments carried out with the recipe in Fig. 2. A) Overview BF-STEM image of the nanowire. B) Color-coded EDS map of the region highlighted by the red square in (A), red As, blue P concentration, respectively. C) Color-coded EDS map of the region highlighted by the red square in (A), red In, blue Ga concentration, respectively. D) BF-STEM detail of the 10-nm-thick InGaAs heterolayer marked by the yellow circle in (B,C). E) EDS line-scan spectra recorded across the InGaAs well as highlighted in (D) by the red arrow showing scan direction.

vertical Si seed facet and corresponding InAs nanowire termination grown along the in-plane ⟨1 1 1⟩ direction [23].

Fig. 1.C shows the slightly modified growth recipe for this experiment. The nucleation step was shortened, and the purge step after InGaAs was split equally with 10 s of As flow and 10 s of P flow, with all other growth step times slightly modified as well. The final quantum well segment was repeated three times.

2.3. Structural and chemical characterization

An in-depth structural, crystallographic, and compositional analysis was performed using STEM and EDS.

Electron transparent lamellae of selected nanowires were cut out of the 2 cm × 2 cm chip and thinned using the FEI Helios NanoLab 450S FIB. Each cut was executed to expose a cross section along the growth direction. The STEM and EDS study was carried out using a double-corrected JEOL ARM-200F microscope operating with a beam energy of (200 ± 0.3) keV and equipped with a JED-2300 T EDS detector. Data from both STEM images and EDS line-scans was processed using the Gatan microscopy suite 3.0 (GMS3).

3. Results and discussion

3.1. Heterostructure growth

The first sample was grown using the precursor sequence shown in Fig. 1.A which serves as reference structure for the growth optimization study. Fig. 3.A shows the bright field (BF-)STEM image of the cross section of a nanowire grown from left to right. The silicon seed on the left side has two {1 1 1} facets on which the III-V material nucleated and grew into an InGaAs segment, with InP in between. The small size of the P atoms compared to the As atoms, make the InP region appear lighter than the InGaAs region because of channeling contrast. The InGaAs is terminating in a multi-faceted front, with two inclined {1 1 0} facets at the top and one {1 1 1} facet at the bottom. This is a common growth front morphology for InGaAs nanowires along the in-plane ⟨1 1 0⟩ direction and originates from the availability of five energetically equivalent {1 1 0} facets and two polar $\{111\}_A$ or $\{111\}_B$ facets. The growth rates of the low index facets depend on the specific growth conditions and varies with T and V/III ratio [24]. In contrast, the InP base layer grows much faster using high V/III ratios in the ⟨1 1 0⟩ direction compared to the ⟨1 1 1⟩ direction, leading to a large, single $\{111\}_B$ facet as the evolving growth front, as indicated by the yellow line in Fig. 3.A. Therefore, an InP segment is preferred as starting point for the growth of well-defined heterostructures in this geometry.

The compositional transition profiles of the heterostructures resulting from the reference recipe are evaluated using high-resolution EDS maps, shown in Fig. 3.B,C. Comparing the group V map (Fig. 3B) with the group III map (Fig. 3C), reveals that the group V (As, P) are confined in the respective layers with well-defined interfaces, while group III elements (In, Ga) show intermixing. This intermixing is particularly visible in the bottom right corner of the EDS maps, where the thin (75 s long pulse) phosphide layer does not have a corresponding In rich (Ga-free) signal. This indicates that diffusion effects in the template channels strongly affect the group-III precursor distribution, causing extensive alloying when the growth step time is similar to the timescale of the diffusive processes. An atomic resolution image of the InP layer indicated in Fig. 3B, C is presented in Fig. 3.D, with the yellow lines highlighting the heterointerfaces, and the red and blue lines identify the InGaAs and InP segments, respectively.

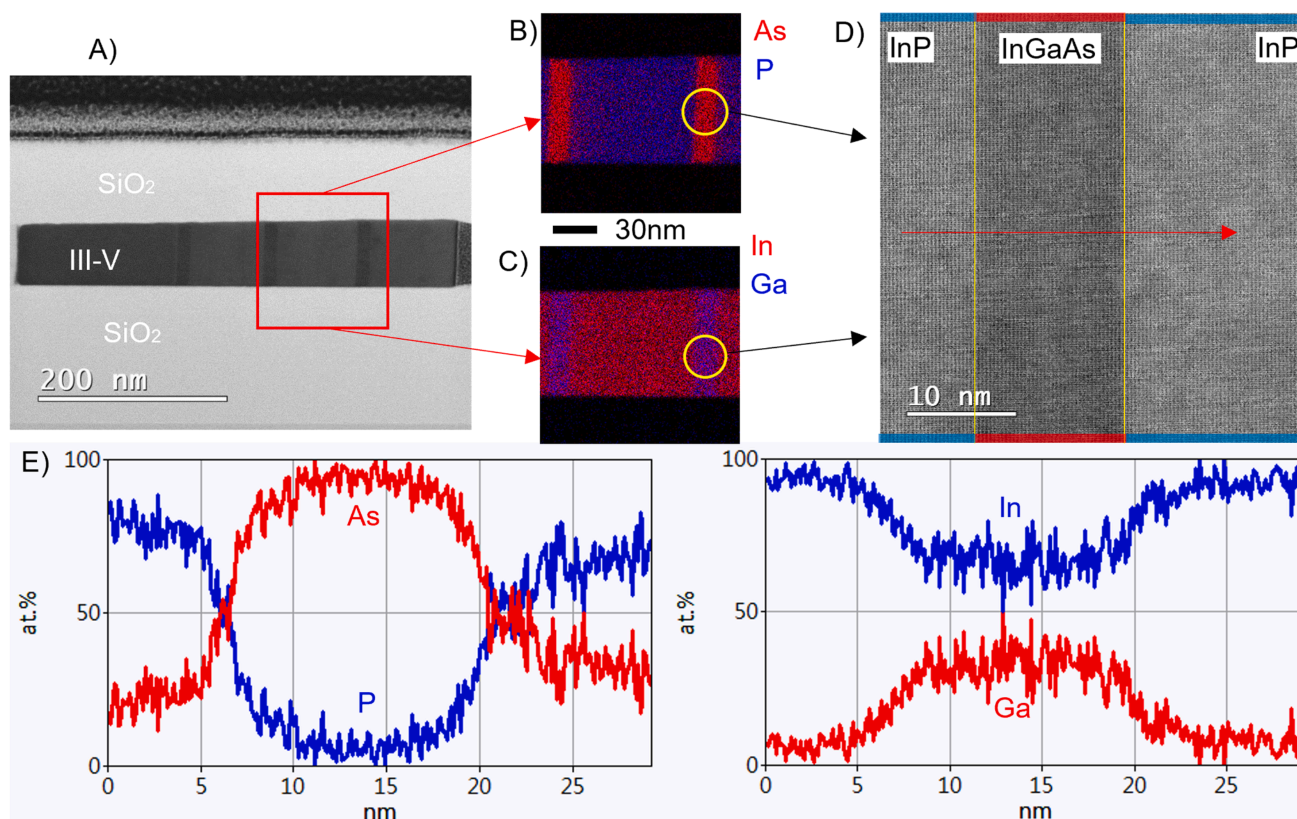

Fig. 5. STEM image and EDS maps of a lamella cut from one of the nanowires grown on a ⟨1 1 0⟩ SOI. A) Overview BF-STEM image of the nanowire. The silicon seed is on the left and silicon oxide is on the top and bottom. The entire heterostructure stack is visible due to channeling contrast: InGaAs appears darker than InP. B) Color-coded EDS map of the region highlighted by the red square in (A): in red In concentration and in blue Ga concentration. C) Color-coded EDS map of the region highlighted by the red square in (A): in red As concentration and in blue P concentration. D) High resolution BF-STEM detail of the 10-nm-thick InGaAs well. E) EDS line-scan spectra recorded across the InGaAs well as highlighted in (D) by the red arrow showing scan direction.

3.2. Heterointerface optimization

Based on the previous results, an optimized recipe sequence including purge steps was implemented, as indicated in Fig. 1.B. The experimental result is shown in a BF-STEM cross section image in Fig. 4.A. The sample is recorded with the Si seed on the right-hand side of the image, from which a first InGaAs nucleation layer is grown, followed by a first InP layer, similarly to the procedure that was followed in the growth of the sample in Fig. 3.

The stabilization of the growth front into a single {1 1 1} facet during InP growth is accomplished once again. However, first differences can be readily observed in the sample. Owing to the introduction of hold steps in the growth recipe, this {111} growth front is maintained throughout the quantum well region, resulting in the creation of well-defined, flat, and reproducible heterolayers. The single facet growth front avoids issues related to different incorporation rates and thickness variations that are present with a multi-faceted growth front [22]. The change in InGaAs and InP deposition time to 30 s and 180 s respectively creates 9-nm-wide InGaAs quantum wells evenly spaced between 41-nm-wide InP base layers. The $\langle 1 1 1\rangle_B$ growth rates extracted are 13.9 nm/min for InP and 18.5 nm/min for InGaAs, respectively. The chemical composition of the heterointerface was investigated by EDS. The V-group and III-group element concentration maps are shown in Fig. 4.B and 6.C, respectively indicating the suppression of intermixing between the two III-V materials. A high resolution ADF-STEM image of the first InGaAs well is presented in Fig. 4.D and shows that the only defects present are twin planes consistent with growth along the $\langle 1 1 1\rangle_B$ direction [22]. The difference in channeling contrast in the InP region at the top left and bottom right of Fig. 4.D, together with the red background in InGaAs layers in Fig. 4.B are indications of small amount of As in the InP region. This is further supported by the EDS line-scan across the InGaAs quantum well shown in Fig. 4E.

Here, the atomic percentage of each group-V element is calculated from the characteristic K lines in the EDS spectra at 10.5 keV for As and at 2 keV for P. The higher As level observed in the InP layer after the second interface indicates As carry-over contamination, which is not found after the first heterointerface. A qualitative composition of the $In_xGa_{1-x}As$ layer was obtained using the relative intensities of the L lines of In and Ga, at 3.3 keV and 1.1 keV respectively, as the In K line is not in the detector spectral range (Fig. 4.E, right side). Given the high noise fluctuations of the concentration profiles, a value of $x = 0.55$ of the $In_xGa_{1-x}As$ is extracted. This molar fraction, as discussed, represents an indicative data point, not only because of the noise but also because the calculation uses the standard EDS cross sections available with the Gatan Microscopy suite and there has not been a further in-house calibration.

3.3. Vertical heterointerfaces (orthogonal to the wafer plane)

In the previous examples, a ⟨001⟩ device layer SOI was used as growth substrate, where a multi-facetted growth front can develop leading to poor geometric control, composition variations for ternaries, and in any case a heterointerface which is not perpendicular to the growth direction, which is clearly an undesirable situation for device fabrication. This can be circumvented by using a Si wafer orientation having vertical {1 1 1} crystal planes as available on an ⟨1 1 0⟩ SOI wafer. Fig. 5.A shows a BF-STEM image of a nanowire with vertical and well-defined hetero-interfaces.

A similar level of As background impurities is present after each InGaAs segment, as is evident from Fig. 5.B, while Fig. 5.C shows how Ga is well confined to the respective layer. The high-resolution BF-STEM

image in Fig. 5.D shows the heterointerface between the 85-nm-thick InP, on the left- and right-hand side of the image, and the 14-nm-thick InGaAs quantum well structure that appears as a dark layer in the middle of the image. The extracted $\langle 111 \rangle_B$ growth rates are 25.5 nm/min for InP and 42.9 nm/min for InGaAs, respectively. This marks an increase in growth rate that can be attributed to the different template shape, as template height was reduced from 220 nm to 70 nm. Fig. 5.E shows the composition profiles for the III- and V- group elements across the quantum well region. The presence of As impurities immediately after the quantum well layer is once again noticeable on the right hand side of the V element graph, as the As and P concentration profiles are asymmetric. This asymmetry is evident when compared with the symmetric composition profiles for the III-group elements, which maintain the interface quality observed in the sample shown in Fig. 4. The III composition profile Fig. 5.E highlights how the $In_xGa_{1-x}As$ composition is more rich in Indium, having an $x = 0.60$. As the flows into the reactor were not altered from the sample shown in Fig. 4, this composition change can also be attributed to the different template geometry.

4. Conclusions

In this work, we have demonstrated how TASE can be used to create a heteroepitaxial structure consisting of lattice matched InP and InGaAs layers grown on Si, with high control on both heterointerfaces and heterolayer morphology and composition. An in-depth STEM and EDS analysis of nanowires containing InGaAs and InP layers gave insight on the diffusion and growth mechanisms inside a TASE template, highlighting the beneficial effect of introducing hold steps. We have achieved vertical (perpendicular to the growth direction) single facet heterointerfaces with limited cross contamination across them for growth on $<110>$ SOI templates. Finally, the incorporation of vertical QW structures into our recent devices [14] is expected to significantly improve the photon emission properties.

CRediT authorship contribution statement

Enrico Brugnolotto: Conceptualization, Methodology, Formal analysis, Investigation, Data curation, Writing – original draft, Visualization. **Markus Scherrer:** Investigation, Writing – review & editing. **Heinz Schmid:** Methodology, Resources, Writing – review & editing. **Vihar Georgiev:** Writing – review & editing, Supervision, Project administration, Funding acquisition. **Marilyne Sousa:** Methodology, Writing – review & editing, Supervision, Funding acquisition.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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