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Investigation of Geometrical Impact on a P+ Buried Negative Capacitance - SOI FET

Toushik Santra[1], Ankit Dixit[2], Saheli Sarkhel[1], Navjeet Bagga[3]

[1] Netaji Subhas Engineering College, Kolkata, West Bengal, India
[2] University of Glasgow, Glasgow, Scotland, United Kingdom
[3] PDPM IIITDM, Jabalpur, Madhya Pradesh, India

Abstract:

Through this paper, we have proposed and investigated the impacts of various device parameters on a novel p^+ buried negative capacitance (NC) silicon-on-insulator MOSFET. Introduction of the p^+ buried region below source/drain is to restrict electrons from conduction in the absence of a channel with least effect on the on-current of the device. Till date, at the channel length of 20 nm, thin channel based devices are more desirable. Thicker Silicon Film Thickness (T_{Si}) has not been reported in 20 nm channel length based devices due to the problem of high leakage current and higher dominance of short channel effects. The proposed device structure effectively reduces the leakage current and reduced gate capacitance therefore gives better DC and RF characteristics respectively. Ferroelectric based negative capacitance is included in the study along with the geometrical variation. With the simulation data extracted from Silvaco Atlas TCAD simulations, we have reported the impacts of structural parameters like variation in channel length (L_G), film thickness (T_{Si}), spacer extension length (L_{Ext}), NC included gate stack properties and the effect of the inherent impact ionization is also reported in this paper. The later part of the study focuses on the capacitance-voltage (C-V) curve for varying channel length along with the RF parameter analysis such as intrinsic gate delay, power and energy dissipation, and transconductance generation factor. Therefore, both DC and AC characteristics of the device have been extracted and reported in this paper, thereby substantiating the feasibility of our device.

Keywords: Silicon-on-Insulator, Short Channel Effects, Film Thickness, Spacer Extension Length, Impact Ionization, Negative Capacitance

I. Introduction

The high demand for performance improvements and efficiency in electronic devices is driving the need of improving the building blocks of these devices, the transistors. We know that Moore's Law [1] has already stimulated the scaling of transistors for more than half a century now, which has brought down the size of these transistors to sub-micron order. The device scaling in these dimensions is introducing new anomalies which is making the scaling increasingly difficult going forward. In the last decade, typical MOSFET has thus been replaced by new unconventional structures to keep the scaling trend predicted by Moore’s Law and performance improvements moving forward [2-3].

The MOSFET has always been prone to parasitic effects, known as latch-up effects, in the bulk substrate region, that interferes with the traditional MOSFET operations by introducing effects like delays due to the existence of capacitance between source/drain and substrate [4]. But due to the long channel length compared to the depletion width of source and drain and the sufficient thickness of the gate oxide, these effects were negligible. As the scaling moved forward and the channel length came down to micron and then to sub-micron order, the channel length is now comparable with the depletion widths. This has resulted in many effects that are adversely affecting the device performance, which are collectively known as short channel effects (SCEs) [5]. Therefore these inhibiting parameters are also reducing the performance and efficiency which is making the latch-up effects comparable to the functional parameters of the device and also due to the overall scaling, the latch-up effects have also increased significantly and have started to dominate over the MOSFET operations. Hence the primary structural modification that addressed this problem introduced a box oxide layer between substrate and the channel. This new device is called Silicon-on-Insulator (SOI) [6]. The box oxide isolates the substrate from the source, drain and channel so that the parasitic capacitance is not interfering with the MOSFET operations.

The sub-micron dimensions of the device has brought the channel length to be comparable to the drain depletion layer thickness and also the gate oxide (SiO_2) scaling is reaching its thickness limits. These changes are increasing the dominance of the SCEs, namely channel length modulation (CLM) [7], threshold voltage roll-off [8], drain induced barrier lowering (DIBL) [9-10], hot carrier effects [11], fringing fields [12] at the source and drain, and Subthreshold Leakage. All these effects have stimulated the research focus

towards mitigating these problems and have diverged the research focus on different sectors, namely gate material engineering (study how the gate metal properties impact the device), gate oxide engineering (study how gate oxide layer scaling moves forward) [13], device design engineering (newer structural modifications).

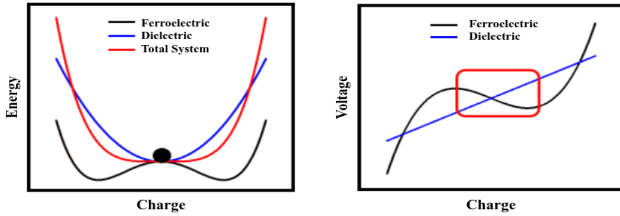

Fig. 1(a): Energy vs Charge characteristic for FE, DE and combined stack of FE + DE (**b**): Voltage vs Charge characteristic for FE, DE and combined stack of FE + DE [14].

Since the advent of low power applications like IOT and battery powered consumer electronic devices, the power efficiency has become an important factor for designing a device. This requires a steep switching capability and lower power requirement for operation, i.e., lower Subthreshold Slope. A traditional MOSFET operation imposes a boltzmann limit of 60 mV/dec. One modification in the gate oxide has proved itself to be potentially able to reduce the subthreshold slope beyond 60 mV/dec limit. To mitigate the limit, researchers proposed the concept of the negative capacitance in the gate oxide stack. There are some insulators which are categorized as ferroelectrics owing to their hysteresis formation during a certain range of charging and discharging. This region's property can be harnessed to introduce an internal amplification in the electric field. This phenomenon is called Negative Capacitance [14-17].

Fig. 1(a) and (b) displays the Energy-Charge profile and Voltage-Charge profile respectively [16]. The energy landscape of the ferroelectric insulator forms a 'W' like structure and quite evidently, a region exists where the energy/charge relation forms an inverse parabola, opposite to that obtained in the case of a dielectric. In an isolated operation, the negative capacitance region is highly unstable as there are two minima in the same level on either side of the NC region (the minima's of the 'W' like structure), but it has been found as in the literature that if a ferroelectric gate oxide is fabricated in series with a dielectric [16-18] in the Gate Oxide layer of the MOSFET, through an optimization called Capacitance Matching [19-20], it is possible to operate the device in the negative capacitance region of the ferroelectric oxide, i.e., stabilize the operating region of the oxide stack (Total System) and achieve a current amplification in the characteristic of the MOS operation [20-21]. This inverse of the DE function is cleared in Fig. 1(b). With linear stepping up of charge, the voltage does not show a linear relationship completely. The region marked by a red box shows the region where for the same charge step, there is a negative slope obtained. This is the negative capacitance region where charge concentration increases for the same voltage supply.

The scaling of transistors has brought down the device dimensions to sub-micron order, but to the best of our knowledge, there has not been a significant linear relativity with the wafer scaling, i.e., the wafer thickness used for fabrication is not following the scaling trend of the device in a linear manner. Thus, in our device we have introduced a novel structure which utilizes the vertical thickness of the wafer, with a channel of 20 nm, and is still producing better current on-off ratio, higher peak on-current, hence a better subthreshold slope compared to [21].

II. Device Structure and Simulation Framework

The schematic of our proposed P^+ Buried NC-SOI MOSFET device is shown in Fig. 2. A 20 nm channel is used in the device. The P^+ Buried Region is responsible for shielding the subthreshold conduction, i.e., it reduces the leakage current of the device. A 50 nm box oxide insulates the substrate from the rest of the device to shield the parasitic devices which would have become much more dominant compared to the device characteristics. The silicon thickness in the channel region is of 30 nm which utilizes the vertical thickness of the wafer into the device. Though the p^+ buried region takes up the responsibility of masking and reducing the leakage current, the overall device produces a better subthreshold slope and better $I_{ON\text{-}OFF}$ ratio. The Gate Stack of FE (Si: HfO_2), 1.7 nm thick, and DE (SiO_2), 0.6 nm thick, is used to utilize the advantages of NC properties in the device. The presence of DE is responsible for operating the MOS in the negative capacitance region of the FE layer. The Spacer region becomes very crucial in such short channel length, this buffer region plays a crucial role of shielding electrons from Source/Drain from entering the channel region at grounded gate bias, i.e., when there is no channel present for conduction. The dimensions of the device are shown in Table 1 in details.

We have used Silvaco Atlas TCAD [22] software for the Simulation of our device and Tonyplot for initial visualization [23] of the characteristics or the device structure itself. Besides the LK models for inclusion of the Negative Capacitance property, we have also used drift diffusion (DD),

schottky read hall (SRH) recombination field dependent mobility (FLDMOB), concentration dependent mobility (CONMOB), band gap narrowing (BGN) and trap assisted tunneling (trap.tunnel) models. The baseline structure has been calibrated with the device reported at [24-26] and shown in Fig. 3 (a) and (b).

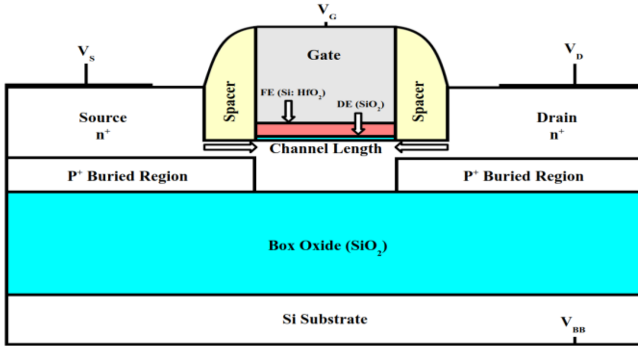

Fig. 2: Schematic Diagram of P+ Buried NC-SOI Devic.

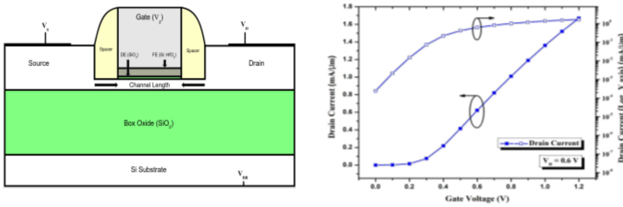

Fig. 3 (a): schematic for calibration of TCAD models against the baseline NC-FDSOI. **(b)** Input (I_D/V_G) characteristics of calibrated model of the baseline NC-FDSOI.

Table 1: Dimensions used to simulate our proposed device.

Device Parameters	Symbol	Value	Unit
Source Doping Concentration (n+)	N_D	$5x10^{20}$	cm-3
Drain Doping Concentration (n+)	N_D	$5x10^{20}$	cm-3
Channel Doping Concentration (p)	N_A	$5x10^{17}$	cm-3
P^+ Region Doping Concentration	N_A	$5x10^{19}$	cm-3
Substrate Doping Concentration (p)	N_A	$5x10^{17}$	cm-3
P^+ Buried Region Thickness	-	20	nm
Channel Length	L_G	20	nm
Si Thickness	T_{Si}	30	nm
Box Oxide Thickness	T_{Box}	50	nm
FE Layer Thickness (Si: HfO2)	T_{FE}	1.7	nm
SiO_2 Gate Oxide Layer Thickness	T_{DE}	0.6	nm
Gate Metal Work Function	WF	4.6	eV
Dielectric Constant of Spacer	$\varepsilon_{Spacer(SP)}$	$7.5\varepsilon_o$	F/m
Frequency	f	1	MHz

III. Results and Discussion

Using TCAD simulations, we have successfully simulated the aforementioned P^+ buried Negative Capacitance SOI MOSFET. The improvement provided by Negative Capacitance and Impact Ionization provides a much desirable characteristic to our device. Simulating and extracting a comparative study of the variation in different structural parameters on the device characteristics has been discussed as follows.

The Input characteristics are shown in both linear (left axis) and logarithmic (right axis) representation of the drain current (I_D) in Fig. 4(a) and (b) respectively. The output current crosses 1.6 mA (at 1.2 V of Gate Bias) and the leakage current goes as low as in the order of 10^{-8} mA (at 0 V of Gate Bias) at its normal operations. These results are much desirable and improved with respect to available NC-based devices presented in [19-20]. This device also produces a subthreshold swing of 69.4 mV/dec and a threshold voltage of 0.37 V which is addressed in a wider aspect later in the discussion. The output characteristics shown in Fig. 4(b) shows the combined effects of Impact Ionization, Negative Capacitance which causes a secondary kink at around 0.4 V of Drain Bias and the output current increases henceforth. This phenomenon can be incorporated in implementing Spiking Neural Networks for generation of sudden electrical signals similar to the synapse in biological neurons [26-27].

Though the NC inclusion causes a slight charge saturation in the ON-state (as seen in Fig. 5(a) (left Y axis), the peak output current is significantly better than that with NC properties not implemented. Fig. 5(a) (right Y axis) shows that there is a 4.4% deterioration in Subthreshold Swing (SS) due the omission of NC properties. Fig. 5(b) shows the output characteristics (I_D/V_D) with the NC properties enabled and disabled. Except for the saturation region between 0 and 0.2 V, the rest of the graph is almost parallel to each other. Hence, the saturation region is improved by 38% due to the implementation of NC properties. This higher on-current and nearly same off-current produces a better $I_{on\text{-}off}$ ratio which can serve an instrumental role in improving the analog or RF performance [28].

Fig. 6(a) and (b) show the input (I_D/V_G) and output (I_D/V_D) characteristics with the Impact Ionization (II) model enabled and disabled respectively. The presence of II is an unavoidable factor for our device at its dimensions. But it is important as part of our device characteristics to show the existence of impact ionization is not being harmful for the device. It causes a further increase in output current. The

input characteristics show a similar variation in characteristics as in Fig. 5(a). But the output characteristic shows a secondary jump (kink) in the slope of the output current with II implemented after current saturation at the drain terminal has been reached. This causes an increase in output current compared to a non-NC counterpart of this device. To the best of our knowledge, the impact-ionization effect is responsible for this kink occurring in the PDSOI characteristics [29-31].

In Fig. 7, we have compared the Input (I_D/V_G) characteristics of our device and varying the vertical thickness of the channel film (T_{Si}). It is clearly visible from Fig. 7(a) (left Y axis) that for lower thickness, better on-current and lower threshold voltage is observed. But in the logarithmic representation of the Drain Current (I_D) in Fig. 7(a) (right Y axis), 10 nm and 15 nm thicknesses have a significant rise in leakage current. Hence, even with slightly lower on-current, the on-off ratio is obtained as more desirable after 20 nm and stays almost constant. Our device has 30 nm film thickness so as not to place itself in the absolute edge of scalability. Since the subthreshold swing does not vary linearly with the change in film thickness, we have also compared the value of subthreshold slope with respect to film thickness variation in Fig. 7(b). Though it is already clear from other figures, it specifically touches the point that after 20 nm, the Subthreshold Swing is almost constant and there is negligible change. Hence there is no point in considering a device with higher film thickness.

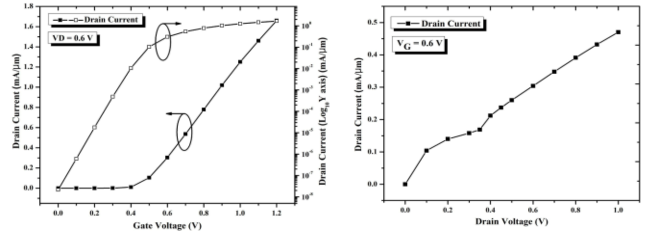

Fig. 4(a): Input (I_D/V_G) characteristics of proposed device Linear (left) and Logarithmic (right) representation. **(b)**: Output (I_D/V_D) characteristics of proposed device.

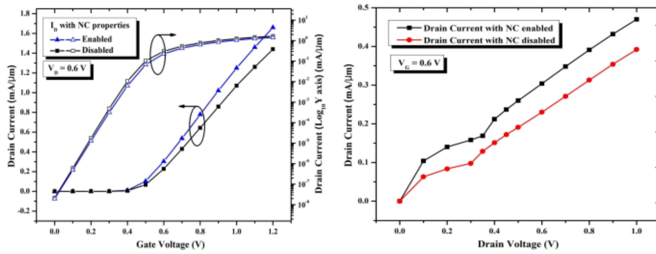

Fig. 5(a): Input (I_D/V_G) characteristics with and without NC properties in Linear (left) and Logarithmic (right) representation. **(b)**: Output (I_D/V_D) characteristics with and without implementing NC properties.

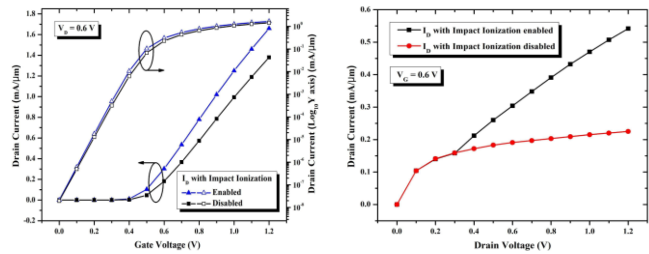

Fig. 6(a): Input (I_D/V_G) characteristics with and without considering Impact Ionization model in Linear (left) and Logarithmic (right) representation. **(b)**: Output (I_D/V_D) characteristics with and without considering Impact Ionization model.

The channel length has been a very crucial parameter in the scaling history of the transistor. But in the sub-micron order, the secondary or parasitic effects have started to interfere in the improvement of the device performance due to gate length scaling. In Fig. 8, we have shown the linear and logarithmic representation of the Input (I_D/V_G) characteristics recorded for different channel lengths. From these figures, we have extracted some key insights in the scaling of our device w.r.t. Channel Length. The increase in peak output current is more or less linear as shown in Fig. 8(a) (left Y axis), but the lowest leakage current obtained as shown in Fig. 8(a) (right Y axis) does not vary linearly with the change in Channel Length. Hence, it can be inferred that the Subthreshold Slope also is not changing linearly with the Channel Length. This result is visualized in Fig. 8(b), to show that after 30 nm channel, the Subthreshold Slope is almost constant, which can infer that scaling till 30 nm is directly proportional to the device parameters [32-33] and after that, further optimization is required to maintain the performance parameters of the device as per Moore's Law.

Spacer extension is the Silicon region between the channel and Source/Drain above which a very high-K dielectric is placed and this region is lightly doped with donor atoms so that it provides a connection between Source/Drain but acts as a buffer to stop the depletion layer of Source/Drain from encroaching into the channel which forms the basis of the reduction in Effective Channel Length or stop hot carriers to enter the channel. Therefore, it is quite significant that reducing the spacer extension length will produce a rise in leakage current and also in the ON-current. The same has been simulated and shown in proper visualizations to show that our device's Spacer Extension (8 nm) is producing a desirable result in terms of the device characteristics. Figure 9 shows the linear (left Y axis) and logarithmic (right Y axis) representations of the input (I_D/V_G) characteristics which

justifies the aforementioned expected characteristics. Fig. 9(b) shows a visual comparison of the Subthreshold Slope due to variation in Spacer Extension length which are Inversely Proportional to each other.

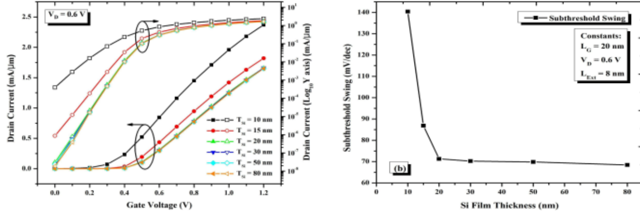

Fig. 7(a): Input (I_D/V_G) characteristics for variation in film thickness in Linear (left) and Logarithmic (right) representation. **(b)**: Comparison of Subthreshold Slope with respect to Channel Film Thickness.

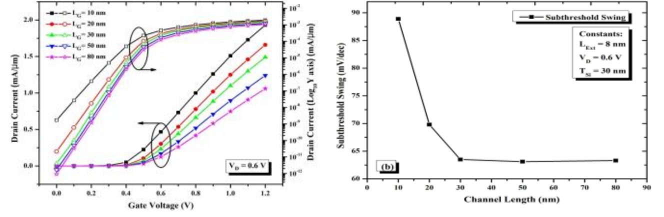

Fig. 8(a): Input (I_D/V_G) characteristics for variation in channel length in Linear (left) and Logarithmic (right) representation. **(b)**: Comparison of Subthreshold Slope with respect to channel length.

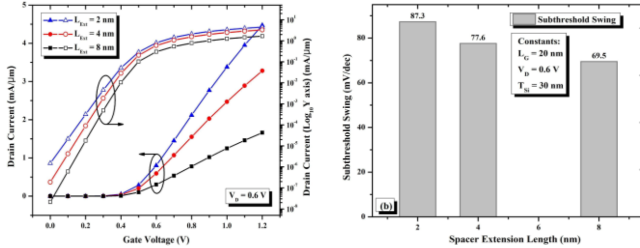

Fig. 9(a): Input (I_D/V_G) characteristics for variation in extension length in Linear (left) and Logarithmic (right) representation. **(b)**: Comparison of Subthreshold Slope with respect to spacer extension length.

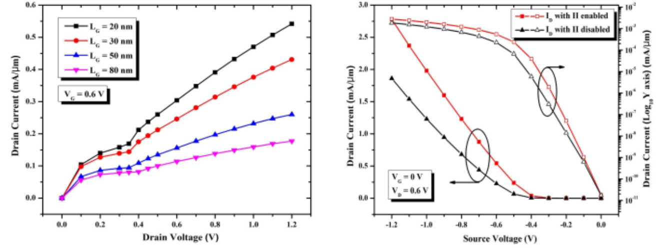

Fig. 10: Output (I_D/V_D) Characteristics for variation in channel length.

Fig. 11: I_D/V_S Variation recorded at Grounded Gate Bias in Linear (left) and Logarithmic (right) representation.

Fig. 10 shows the output (I_D/V_D) characteristics for varying channel lengths. After the kink, the peak drain current value is reducing with increasing channel length. Hence this is reducing the device efficiency. Therefore, we are using 20 nm channel length as it maintains an optimum desirable balance between the input (I_D/V_G) and output (I_D/V_D) characteristics of the device. In the similar way, Fig. 11 shows the I_D/V_S characteristics for grounded gate bias in linear and logarithmic representations respectively with and without considering the Impact Ionization parameter. Due to this, the peak drain current is again increased to a significant extent [25]. Channel length of a device has played a very important role in the scaling of transistors. Therefore Table 2 provides the key data of our device compared with variation in channel length. The I_{ON}, I_{OFF} and I_{ON} - I_{OFF}, Threshold Voltage, and Transconductance data proves the device with 10 nm channel as the most desirable but the subthreshold slope speaks differently in the table. Lower SS is more desirable but the device with 10 nm channel has produced the highest Subthreshold Swing. Comparing all the data together the primary device proves the most desirable owing to the fact that the difference in SS is negligible after 20 nm channel length, hence the lower channel length is preferred to the other.

Table 2: Comparative DC parameters of our primary device (P^+ buried NC-SOI MOSFET) with respect to variation in channel length.

Channel Length	Unit	10 nm	20 nm (Primary)	30 nm	50 nm	80 nm
I_{ON} (@ V_G = 1.2 V)	mA	1.93	1.66	1.49	1.24	1.06
I_{OFF} (@ V_G = 0 V)	mA	$1.76x10^{-6}$	$2.15x10^{-8}$	$4.06x10^{-9}$	$1.71x10^{-9}$	$9.26x10^{-10}$
I_{ON} – I_{OFF} Ratio	-	$1.56x10^{-04}$	$0.99x10^{-04}$	$0.9x10^{-04}$	$0.44x10^{-04}$	$0.41x10^{-04}$
Subthreshold Swing (SS)	mV/dec	88.9	69.5	63.5	63.1	63.3
Threshold Voltage (V_{Th})	V	0.33	0.37	0.39	0.39	0.4
Transconductance (g_m)	mS	2.69	2.44	2.22	1.9	1.65

IV. RF Analysis

To prove our device's feasibility in the RF domain, AC transient analysis of the device is necessary. The RF behavior of our proposed P^+ buried NC-SOI MOSFET including intrinsic gain, power and energy dissipation, power and energy delay factor, unity gain bandwidth, transconductance and Transconductance Generation Factor (TGF) are analyzed in detail [34-35]. The RF behavioral factors depend strongly on the C-V characteristics of the device [36]. The C-V characteristic is shown in Fig. 12. The desired data retrieved from our simulation is displayed in Table 2. Since the channel length of a device plays a very crucial role in the device performance, we have presented the RF analysis of our device along with the impact of varying channel length in the aforementioned RF parameters [37]. From the device point of view, the RF behavioral targets that are intended to achieve are also aligned with Moore's Law. This includes the minimization of power and energy requirements to operate the device, or we can specify more accurately as to reduce the power and energy requirements and also loss which impacts the efficiency of the device.

Fig. 12 clearly shows the characteristic trend that a lower channel length shows inferior Gate Capacitance [38]. This trend is desired owing to the fact that for better switching characteristics, the power and energy parameters are considered as for "Lower is Better". Fig. 13 and 14 indicate the fact that power and energy parameters are inversely proportional to channel length and directly proportional to capacitance. Therefore, we can infer that reduction in capacitance reduces the power and energy parameters as well. But keeping the previous DC characteristics in mind and the factors for choosing 20 nm over 10 nm channel length, our device shows an optimal characteristic.

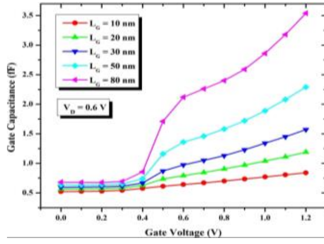

Fig. 12 (a): Variation of Gate Capacitance w.r.t. Gate Voltage recorded for different channel lengths.

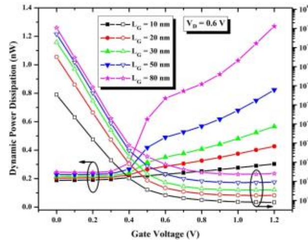

Fig. 12 (b): Variation of Dynamic Power Dissipation (left) and Power Delay Product (right) w.r.t Gate Voltage.

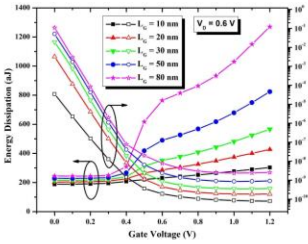

Fig. 12 (c): Variation of Energy Dissipation (left) and Energy Delay Product (right) w.r.t Gate Voltage.

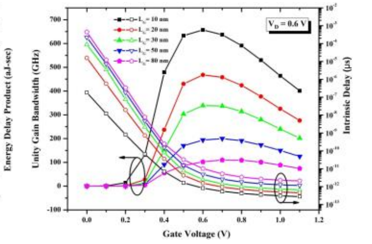

Fig. 12 (d): Variation of Unity Gain Bandwidth (left) and Intrinsic Delay (right) w.r.t. Gate Voltage.

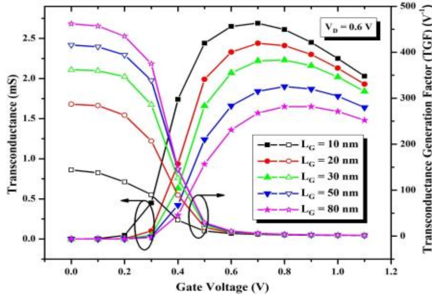

Fig. 12 (e): Variation of Transconductance (left) and Transconductance Generation Factor (right) w.r.t. Gate Voltage.

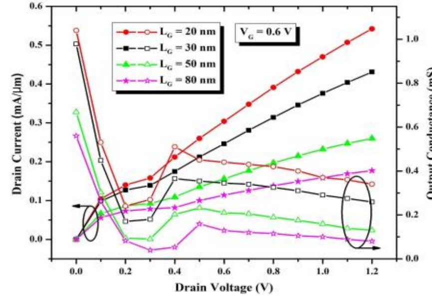

Fig. 12 (f): Variation of Drain Current (left axis) and Output Conductance (right axis) w.r.t Drain Voltage.

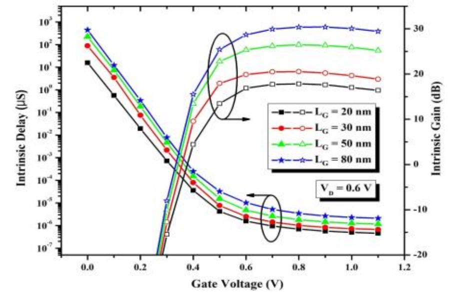

Fig 12 (g): Variation of Intrinsic Delay (left axis) and Intrinsic Gain (right axis) w.r.t Gate Voltage.

Fig. 12(e) indicates a substantial difference in Transconductance generation factor (Early Voltage) [39] between 10nm and 20nm channel devices, though transconductance is recorded higher for lower channel lengths, considering a 20 nm channel provides us substantially higher efficiency [32] over a 10 nm channel based p+ buried NC-SOI MOSFET. Fig. 12(f) shows the output characteristics (left Y axis) along with output conductance (right Y axis). The result indicates the superiority, i.e., higher on-current for lower channel length. The non-uniform variation of the Output Conductance is visually obtained as a side-effect of the kink regime. Similarly, it can also be observed from fig. 12(d) that the unity gain bandwidth is desirable to be higher, providing a better operating frequency bandwidth, and lower values of intrinsic delay, providing lesser switching capability.

Therefore, considering the output characteristics, and transconductance generation factor, unity gain bandwidth, and intrinsic delay, we can infer that 20 nm channel length will provide a much more efficient device performance.

V. Conclusion

This work presents a results backed simulated device structure of a novel P^+ buried NC-SOI FET wrapping the combined effects of keeping a thicker silicon film compared to published SOI structures, keeping a buried p^+ region under source/drain. We have introduced a FE layer in the gate stack to inculcate the negative capacitance effect into the device. This device has been investigated on the DC (input and output current characteristics) as well as AC (RF behavior) characteristics. Along with these simulation parameters, the impact of various structural parameters has been simulated, presented and also compared by varying them w.r.t our device, like channel length, film thickness, functional parameters like with and without including the NC model in the simulation deck, and the effect caused by the unavoidable parameter of such nanoscale devices, i.e., Impact Ionization. The Silicon film thickness affects the leakage current of the device directly but becomes almost constant after 20 nm. This is similar for channel length variation where 30 nm is the lower limit till which the relation between leakage current and channel is almost linear. The spacer extension is a very crucial part of such nanoscale devices and hence a variation of extension length is compared. Considering all these three aspects, our device proves desirable with Silicon film thickness (T_{SI}) = 30 nm, Channel Length (L_G) = 20 nm and Extension Length (L_{Ext}) = 8 nm and the Negative Capacitance is providing a further 4.4% increase in the output current compared to a to the same SOI device but without Negative Capacitance properties. The RF behavior of our device is also simulated and compared with varying channel lengths. Our device again proves itself power and energy efficient, i.e., input power and energy required is comparatively less. Other parameters like Transconductance, Output conductance, delay, intrinsic gain and intrinsic delay also shows that our device is comparatively better. Above all, the Negative Capacitance property is responsible for internal amplification in the DC analysis and an increase in total capacitance due to capacitance matching in AC analysis. With a Threshold Voltage of 0.37 V and a Subthreshold Swing of 70.6 mV/dec and an on-off ratio of 9.65 x 10^{-5}, our device serves as a feasible alternative nano-dimensional device for future applications.

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