ADVANCED ELECTRONIC MATERIALS
www.advelectronicmat.de

Printing of Nano- to Chip-Scale Structures for Flexible Hybrid Electronics

*Adamos Christou, Sihang Ma, Ayoub Zumeit, Abhishek Singh Dahiya, and Ravinder Dahiya**

Flexible hybrid electronics (FHE) offers potential for fast computation and communication needed in applications such as human–machine interfaces, electronic skin, etc. FHE typically comprises devices that can vary from nano- to chip scale, and their integration using a common process is often challenging. Herein, a printed electronics route is presented to integrate the ultrathin chips (chip-scale) and nanowires (NWs)-based electronic layers (nanoscale) on the same substrate. The fabrication process is categorized into three stages: i) direct transfer printing of ultrathin chips (UTCs), ii) contact printing of nanoscale structures, and iii) metal printing using the direct ink write (DIW) method to define electrodes/interconnects. The UTC printing process is carefully optimized by studying the performance of transistors present on them. Electrical data collected from 14 transistors located on 3 different chips show negligible variation in performance after they are transfer printed—thus confirming the efficacy of the printing technique. The superior grade quality of ZnO-NWs-based electronic layers printed on the same substrate is also demonstrated by constructing UV photodetectors using DIW printing. The photodetectors show high responsivity (≈2×10^7 A W^{-1}) and specific detectivity (≈5×10^{15} Jones) at a low UV intensity of 0.5 μW cm^{-2}.

1. Introduction

Flexible hybrid electronics (FHE), which combines the printed electronics and silicon (Si) technology, has gained attention recently because of the possibility to gain from the best of both technologies and obtain electronic system that allows high-speed connectivity, low data latency, enhanced functionality, conformable form factors, low-cost fabrication, and others.[1] These features are important as they underpin the transition to an increasingly connected world which will see mass digitization through wide range of applications such as digital health, environment monitoring, human–machine interfaces, internet-of-things and industry 4.0 etc.[1d,e,2] However, it is challenging to have these features with either Si technology (due to its rigid nature) or the printed electronics alone (because of the low-speed electronics the current printed devices offer).[2e,3] The cross-fertilization of conventionally manufactured and thinned Si chips, termed as "ultrathin chips (UTCs)",[1a,4] and printed electronic devices[5] on a flexible substrate could provide a practical route to satisfy these requirements. However, this also demands a common manufacturing technology platform to integrate devices with wide ranging dimensions (from nano to centimeter scale) on flexible substrates, while keeping intact the power of Si electronics.[1a,c]

The advanced printing methods such as transfer printing (TP), contact printing (CP), in-tandem contact-transfer printing etc. are some of the techniques that can enable a deterministic integration of devices with different dimensions into planar or 3D layouts.[5a,c,6] These printing techniques provide cost-effective means to realize heterogeneous integration of microchips as well as diverse functional nanomaterials. These printing methods have been separately employed to achieve high transfer yield of either nano[5c,6d,h,j,7] or micro[5a,8] or chip[9] scale structures. For instance, TP has been explored for pick-and-place of the microchips (≥100 μm) onto flexible substrates with high transfer yield.[10] Whilst pick-and-place approach using elastomeric stamps prove effective for printing large microchips, it is challenging to use the method for ultrasmall chips with ≤100 μm size and/or nanoscale materials with high transfer yield. This is because at these dimensions, i.e., <100 μm adhesion forces including electrostatic, and Van Der Waals on the chip surface may dominate over the gravitational force, as a result these adhesion forces inevitably introduces complication in micromanipulation.[10,11] Furthermore, UTCs are likely to fail during their transfer as compared to thicker

A. Christou, S. Ma, A. Zumeit, A. S. Dahiya
Bendable Electronics and Sensing Technologies (BEST) Group
University of Glasgow
Glasgow G12 8QQ, UK
R. Dahiya
Bendable Electronics and Sustainable Technologies (BEST) Group
Electrical and Computer Engineering Department
Northeastern University
Boston, MA 02115, USA
E-mail: r.dahiya@northeastern.edu

The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/aelm.202201116.

DOI: 10.1002/aelm.202201116

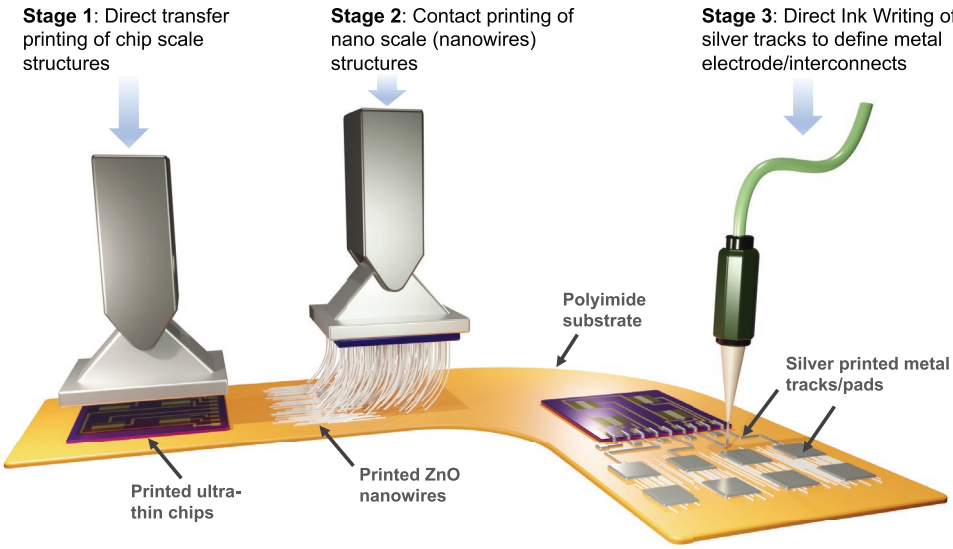

Figure 1. Schematic illustration showing different stages of the proposed printing route for integration of nano- to chip scale structures on to a flexible substrate to realize flexible hybrid electronic (FHE) system in a 2D layout. Stage 1: direct transfer printing of the ultrathin chips (UTCs); Stage 2: contact printing of nanoscale electronic layers; and Stage 3: direct ink writing of the miniaturized metal tracks defining the device electrodes and interconnects.

chips due to lower mass and fragile nature.[12] These challenges could be addressed by "direct roll transfer printing" method, which has been shown to integrate laterally aligned nanoscale and microscale structures with high transfer yield of 95%.[5a,6b,c] But the range of functional materials printed using this approach is limited to the available wafer. Such limitations however, could be overcome by alternative nanostructure assembly methods such as CP,[6d,h,j] in-tandem contact-transfer printing[5c] etc., which exploit bottom-up grown nanomaterials to realize nanoscale electronic layers on various substrates.

In this work, we sequentially use the direct transfer printing and CP to show the integration of nano- to chip-scale structures on to flexible substrate and thus present a new printing platform for FHE. The presented fabrication route is schematically depicted in **Figure 1**. The fabrication process can be categorized into three stages: i) direct transfer printing of chip-scale structures (e.g., UTCs), ii) CP of vertically aligned nanoscale structures (e.g., nanowires), and iii) printing of conductive tracks (e.g., silver) using the direct ink write (DIW) method to define electrode/interconnects. In the first stage, the direct transfer printing method is employed for the first time to place metal–oxide–semiconductor field-effect transistors (MOSFETs) based Si UTCs at selected location. The printing process is cautiously optimized by studying its impact on MOSFET's performance variation during the transfer process. Then (during the second stage), vertically aligned ZnO NWs are contact printed to form uniform nanoscale electronic layer using our custom-made semi-automated contact printing system.[6d,h] Contact printing offers several advantages such as: i) highly directional alignment of nanoscale structures, ii) single-step process for realization of high-grade electronic layers, and iii) no contamination of NW surface (as it is a dry printing method). Following printing of NWs based electronic layer, in the third stage, high-resolution DIW printing technique is employed to fabricate photodetector devices (by defining metal electrodes at two ends of NWs) and realize the interconnects to access the UTCs. The DIW offers excellent printing traits such as: i) high-resolution printing (1–10 µm) to access UTCs pads having microscale dimensions; ii) compatibility with high viscosity ink/paste (>100 000 cP) to achieve highly conductive metal tracks, iii) compatibility with the large area manufacturing, iv) maskless (digital) metal patterning, and v) environmentally benign process (no chemical wastage, less energy usage, drop-on-demand feature, etc.). The fabricated photodetector devices exhibit excellent UV responses at low bias voltage and light intensity (0.5 µW cm^{-2}), including an average responsivity of $\approx 2 \times 10^7$ A W^{-1}, specific detectivity of 5×10^{15} Jones, and current on/off ratio of 10^2, confirming superior electronic grade quality of the printed nanoscale layer.

2. Results and Discussions

2.1. Printing of Nano- to Chip-Scale Structures

Figure 2 shows a schematic representation of the experimental steps followed to integrate nano to chip scale inorganic structures on to flexible substrates. The details of the materials and process conditions are given in the methods section. In the first stage of FHE fabrication process, UTCs are fabricated, and direct transfer printed using our semi-automated custom-built set-up (Figure 2a–c). The UTCs are critical for FHE as they could perform tasks such as complex signal processing, communication etc.[13] which state-of-the-art printed circuits are not able to perform.[1f] Further, they can be bent or flexed with the flexible substrates. There are many methods available in the literature to realize UTCs[3a] but significant challenges exist in their deterministic integration to the flexible substrates. This is because of their fragile nature and stress generation during their integration, as a result of which they are

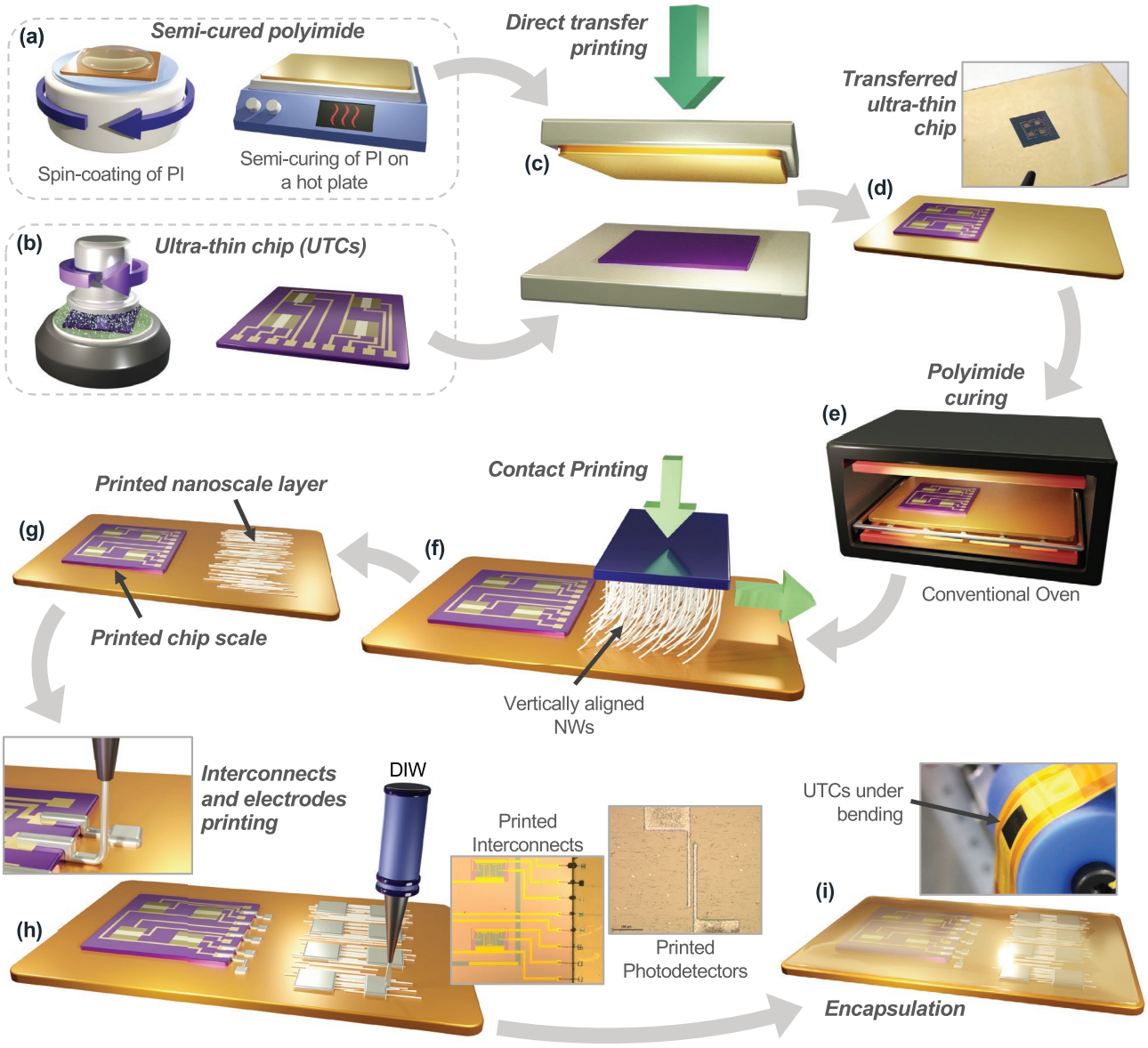

Figure 2. Schematic representation of the experimental steps followed to integrate nano- to chip-scale structures on to flexible substrates to enable FHE systems: a) preparation of receiver semi-cured PI substrate, b) realizing ultrathin chips (UTCs), c) direct transfer printing of chips, d) transferred UTCs, e) PI curing in oven, f) contact printing of ZnO NWs based nanoscale electronic layers, g) printed nano to chip scale inorganic elements, and h) DIW to print electrodes to realize photodetectors and interconnects to access UTCs; optical images of the printed photodetectors and UTCs with printed interconnects are also shown. i) Encapsulation process to embed printed nano- to chip-scale structures for enhanced robustness under bending loadings. The figure shows an optical image of UTC during bending.

likely to be damaged.[4d] To validate the efficacy of the employed direct transfer printing technique for integration of UTCs on flexible substrate, a Si chip having 4 × 4 MOSFET devices was used. The ≈520 µm-thick Si chip was first thinned down to ≈35 µm using our previously reported backside lapping process assisted with poly(methyl methacrylate) (PMMA) sacrificial layer (Figure 2b). The chip thinning steps are briefly described in the methods section and full process details are described elsewhere.[14] Next, the thinned chips were carefully integrated onto flexible substrates using the direct transfer printing approach.

In the direct transfer method, the donor substrate with micro/nano structures is brought in direct physical contact with the semi-cured polymeric film spun over the receiver substrate (Figure 2a).[5a,6b] In the present case we have used semi-cured polyimide (PI), which is also the substrate material. Here, polyimide was used because of its excellent mechanical and thermal properties. In the next step (Figure 2c), the semi-cured PI substrate is brought with close contact with the UTCs. The success of UTC transfer from an elastomeric stamp to receiver (during chip retrieval step) is mainly determined by magnitude of the adhesion strength at the interface between

chip and receiver substrate.[15] The use of semi-cured PI has the following advantages: i) it allows a strong adhesion between the UTCs and the receiver PI which helps with the transfer process, and ii) it allows conformal contact of UTCs with the flexible substrate by avoiding voids in the PI. It is critical to have a void-free bond interface after placement of the chips. Voids could appear during the PI curing due to evaporation of water and solvents.[16] Further, it is possible that air may get trapped at the bonding surface during placement of the chip. The 70–80% of the PI curing process was performed before placing the chip. We have used PI2611 for these experiments as it has coefficient of thermal expansion (CTE) very close to Si. As a result, the chip experiences negligible thermal-induced stress at the interface with substrate and this also prevents the delamination of chip as well the potential damage due to stress-related crack formation.[3d,17] In addition, we used very low thermal ramp rate (≈4 °C min^{-1}) to minimize the stress generation at the chip/PI interface during the ramping up and down of the temperature when PI is cured.

The applied contact force also plays a significant role in defining the transfer yield of direct transfer printing. In general, higher contact force results into higher transfer yield for nanoscale structures.[6b] In the present case, however, extra care was taken to limit the contact force to avoid crack generation in the UTCs. As shown in Figure 2c, UTC was placed upside down (devices facing down) and receiver substrate with a semi-cured PI layer was brought in physical contact by applying an optimized 5N force. To optimize the force applied, we carried out exhaustive experiments on dummy UTCs. Based on these experiments, three different pressure (force) regimes were identified. In the first regime, 1–3 N, the applied force was sufficient to transfer print (pick) UTCs from the stage but the interface between UTC and PI was not conformal/uniform. Because of this we observed delamination of UTCs during the thermal loading-unloading cycles. The second regime is between 4–9 N which showed high transfer yield with good conformal contact between the PI and UTCs. Because of the semi-cured nature of the PI, higher contact forces result into a higher conformal and uniform interface and thus, no delamination was observed. But after 5N no significant improvement in conformability was observed. During the third regime, i.e., ≥10 N, cracking of UTCs was observed. The chip picking from the stage at 5N contact force could be observed from the Movie S1 (supporting information). The applied force was sufficient to pick the UTCs from the stage without any crack or defect formation (observed under optical microscopy). To finalize the stage 1, the PI was fully cured at 300 °C for 2 h in a conventional oven (Figure 2d,e).

In the stage 2 of the FHE fabrication process, CP was performed to assemble uniform and functional nanoscale electronic layer based on ZnO NWs. The electronic layer was realized in a proximity of the printed chip, as shown in Figure 2f, using our custom contact printing set up. The nanoscale electronic layer is realized by the combination of a controlled vertical and shear forces. The shear force was generated due to the applied sliding at a speed of 0.1 mm s^{-1}. The ZnO NW synthesis and CP details are available in our previous articles.[5c,6d] The uniform electronic layer was realized by applying the pressure at the pre-determined level (33 kPa) throughout the printing process. The SEM images (Figure S1, Supporting Information) of printed electronic layers were analyzed using GTFiber2 software.[18] The extracted mean printed NW density is ≈0.5–1 NWs μm^{-1}. Further, >93% of the printed area has shown the average NW orientation within ±5 degrees of the direction of sliding (90°).[5c] A high density of perfectly aligned NWs is required for high-performance flexible transistors/sensors. To demonstrate the high quality of nanoscale electronic layer, in the third stage of the process, the metallization for the electronic device as well as interconnects were formed using a high-resolution extrusion printer, as shown in Figure 2h. The figure also shows optical images of the printed UV sensors and interconnects.

Finally, a thin PI layer was spin-coated for embedding printed UTCs before evaluating their interfacial delamination and mechanical robustness under bending loadings (Figure 2i). Robust flexible ICs are needed in practical applications to reliably process information under different bending/twisting conditions. It is to note that a dummy UTC was used for this purpose to observe interfacial delamination and chip cracking after bending loadings were applied. For this set of experiments, we have performed cyclic bending cycles from 0 to 100 at different bending radius (40, 30, and 20 mm). After performing cyclic bending at each radius UTCs were observed under optical microscope. No cracks/delamination of UTCs was observed, confirming the excellent interfacial behavior between chip and substrate (Movie S2, Supporting Information).

2.2. Evaluation of the Chip Performance After Direct Transfer Printing

The thinning as well as the transfer process could impact the electrical performance of devices on UTCs. For example, the stress during mechanical thinning by back grinding could lead to cracks in Si and thus result in poor bendability or early breakage of UTCs.[4d] These will significantly reduce the production efficiency.[19] Therefore, it is critical to understand the influence of both thinning and direct transfer printing on electrical performance of the devices. The effectiveness of the optimized thinning process was confirmed in our previous publication where we showed similar transistor performance before and after chip thinning. In this work, the reliability, and the influence of direct transfer printing on UTCs is evaluated by studying the n-channel MOSFETs device performance before and after printing process (**Figure 3**). First, the transfer characteristics (I_{ds}–V_{gs}) were recorded by sweeping the gate-source voltage (V_{gs}) from −2 to 2 V at different drain voltages (V_{ds}) from 0.1 to 0.5 V with a step of 0.1 V (Figure 3a). The output characteristics (I_{ds}–V_{ds}) were obtained by sweeping V_{ds} from 0 to 2 V with V_{gs} increased from 0.5 to 2 V at a step of 0.5 V, as shown in Figure 3b. Both transfer and output device characteristics show excellent gate control over the semiconducting channel. The statistical distribution of transistor performance metrics (to have better understanding of the effect of printing process), is obtained by performing electrical characterization for 14 MOSFET devices from 3 different printed UTCs. It is to note that all three UTCs were transfer printed and electrically characterized under similar conditions to have an appropriate process analysis. Percentage (%) change in key transistor

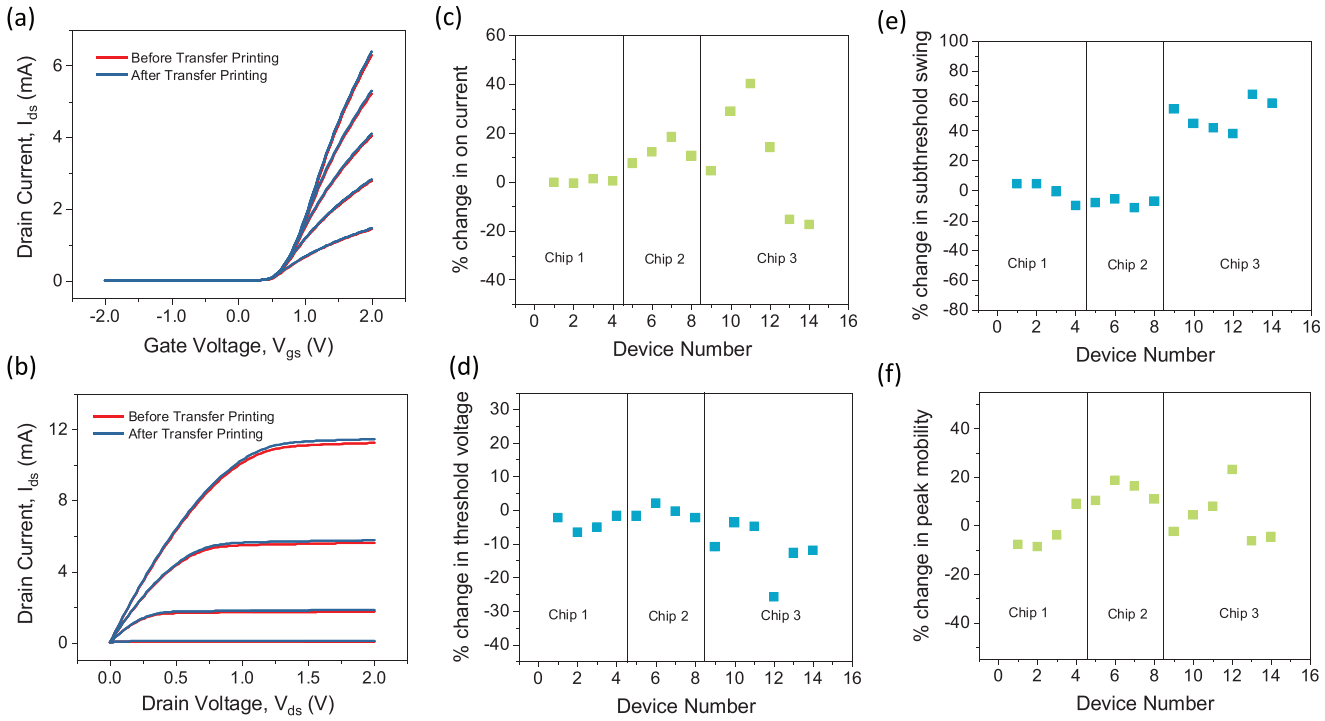

Figure 3. a,b) Device characterization before and after UTC transfer printing: a) transfer function; b) output function. c–f) Percentage change in extracted key paraments before and after transfer printing of 14 MOSFET devices from 3 chips: c) on-current; d) threshold voltage; e) subthreshold voltage; f) peak mobility.

performance parameters before and after transfer printing including device on-current (I_{on}) at V_{gs} = 2 V, threshold voltage (V_{th}), subthreshold swing (SS), and peak field-effect mobility (μ_{FE}) are studied for all devices. It can be seen using Figure 3c that I_{on} changes from ≈–0.3 to +0.5% for chip 1, ≈+7.7 to +18% for chip 2, ≈–17 to +40% for chip 3. Figure 3d presents the % change of V_{th} for each device. The V_{th} is extracted from the linear region of the transfer curve by using the linear extrapolation method to identify the intercept value at I_{ds} = 0. The % change of V_{th} reveals a range from ≈–6.5% to –1.6% for chip 1, ≈–2.1% to +2% for chip 2, and ≈–25% to –3.6% for chip 3. A slightly but negligible negative shift in V_{th} is observed in 13/14 devices. In addition, subthreshold swing (SS) was obtained using Equation (1):

$$SS = \frac{\partial(\log I_{ds})^{-1}}{\partial V_{gs}} \tag{1}$$

It is noticeable that there is an evident change in SS for all devices on 3 different chips (≈–10 to +4.7% for chip 1, ≈–11.5 to –5.4% for chip 2, and ≈+38.1 to +64.3% for chip 3). Considering the factors affecting SS according to Equation (2), the variation can be attributed to the change in the semiconductor and dielectric gate oxide capacitance caused by the origin of defects at the semiconductor/oxide interface. Such defects could be generated by the external mechanical pressure applied during the transfer printing process.

$$SS \cong \frac{kT}{q}\left(1+\frac{C_{dep}+C_{it}}{C_{ox}}\right)\ln(10) \tag{2}$$

where $\frac{kT}{q}$ represents the thermal voltage, 26 mV at room temperature (k is Boltzmann's constant, T is temperature, and q the elementary charge), C_{dep} stands for the depletion region capacitance per unit area of the gate region, C_{it} is the interface trap capacitance and C_{ox} is the oxide capacitance (thickness of Si dioxide = 50 nm). Finally, the field-effect mobility (μ_{FE}) is extracted (using Equation (4)) by deriving transconductance (g_m) using Equation (3):

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} | V_{ds} = \text{constant} \tag{3}$$

$$\mu_{FE} = \frac{g_m}{C_{ox}\left(\frac{W}{L}\right)V_{ds}} \tag{4}$$

where W and L are the channel width and length (W/L = 2000 µm/12 µm). Figure 3f shows the % change in μ_{FE}, (≈–8 to +9% for chip 1, +10 to +18% for chip 2, ≈–4 to +23% for chip 3). It is evident from these measurements that chip 3 showed large variations in performance variation after transfer printing compared to chips 1 and 2. Nevertheless, all devices on various printed chips were operational confirming the efficacy of the optimized transfer printing approach.

We have also investigated the transistor performance after realizing the printed interconnects using DIW. Towards this, devices were characterized from the extended pads printed by the high-resolution extrusion based DIW system under the same conditions as the transfer printing. **Figure 4** demonstrates the transfer and output curves as well as extracted parameters

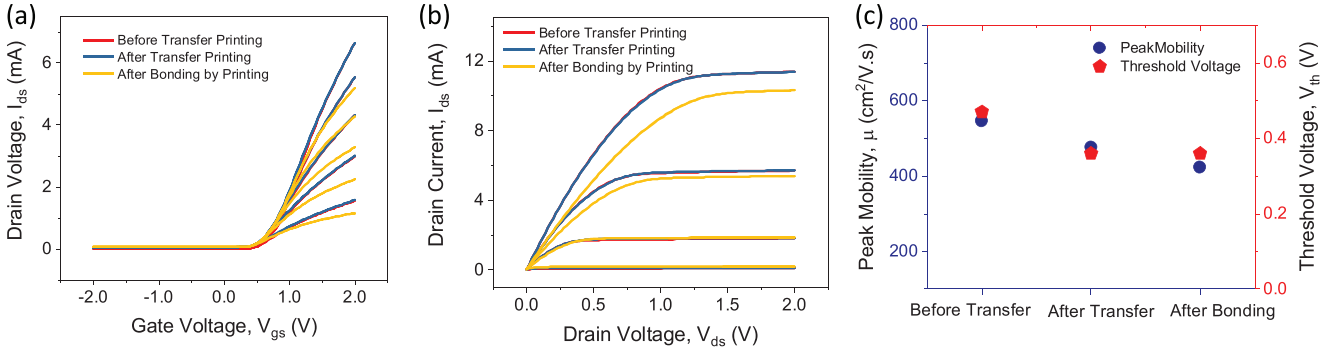

Figure 4. a–c) Transistor electrical characterizations to evaluate the performance before and after transfer printing, as well as after realizing interconnects by printing: a) transfer functions; b) output functions; and c) mobility.

including peak mobility and threshold voltage for all three scenarios, i.e., before transfer printing, after transfer printing and after bonding by printing. A slight reduction of drain current (I_{ds}) after bonding by printing is recorded, which leads to minor decrease in peak mobility (from 476 to 422 cm^2 Vs^{-1}), however, no change in the threshold voltage was noticed (≈0.36 V). The degradation in peak mobility is because of the additional resistance in series due to the resistive printed interconnects.[1a]

2.3. Evaluation of the Nanoscale Electronic Layer Performance as a Photodetector

Next, we evaluated the quality of nanoscale printed electronic layer by fabricating all-printed photodetectors (PDs). Electrical measurements for printed PDs were conducted under ambient conditions using a UV light-emitting diode (365 nm) and presented in **Figure 5**. A time-dependent UV response was recorded under different light intensities (from 0.5 to 2.5 μW cm^{-2}) at 1.5 V bias voltage (Figure 5a). A higher UV light intensity produces a higher value of photocurrent. Further, important parameters including responsivity (R), specific detectivity (D*), external quantum efficiency (EQE), and I_{Photo}/I_{Dark} ratio are extracted from the time-resolved photoresponse curves at different UV intensity. First, responsivity, as shown in Figure 5b, is extracted to determine the photocurrent generated on the effective sensing area per unit illuminated power, as expressed by Equation (5):[5c]

$$R = \frac{\left(I_{photo} - I_{dark}\right)}{\left(P_{in} \times S\right)} \tag{5}$$

where I_{photo} stands for the photocurrent, I_{dark} is the dark current, P_{in} represents the incident power per unit area, and S is the active sensing area. The sensing area S, in this case, is estimated to be the total surface area of the cylindrical ZnO NWs. Considering the channel length (10 μm) and NW diameter (≈100 nm), the sensing area is approximated to be 9.42×10^{-8} cm^2. It is observed that the device presents the highest R (≈2×10^7 A W^{-1}) at the lowest intensity (0.5 μW cm^{-2}). With the rise in light intensity, R gradually decreases. Next, specific detectivity, D^* (Figure 5b), is derived using Equation (6):[5c]

$$D^* = \frac{R}{\sqrt{2e * \frac{I_{dark}}{A}}} \tag{6}$$

where e is the elementary charge and A stands for the total cross-sectional area of the NWs in the sensing channel. D^* is extracted to be as high as ≈5×10^{15} Jones at the lowest intensity, indicating a high sensitivity to smallest detectable signals. Moreover, external quantum efficiency, EQE, is determined (Figure 5c) using Equation (7) to define the photocarrier collection efficiency:

$$\mathrm{EQE} = \frac{R \times hc}{e\lambda} \times 100 \tag{7}$$

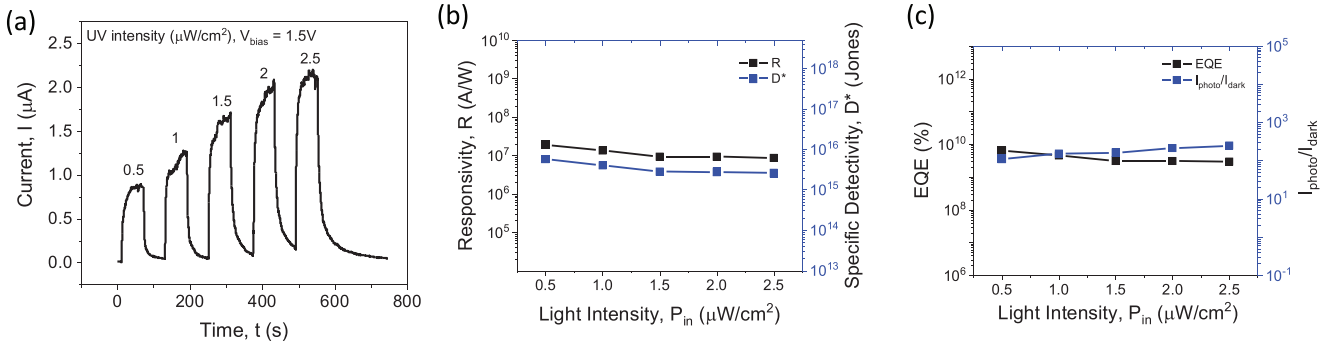

Figure 5. Device characterization of all-printed photodetectors. a) Time-dependent photoresponse at 1.5 V bias under different UV intensities from 0.5 to 2.5 μW cm^{-2}. b,c) Extracted key photodetectors performance parameters including: b) responsivity and specific detectivity; and c) external quantum efficiency and I_{photo}/I_{dark}.

where h stands for Plank's constant, c is the velocity of light and λ is the wavelength of the incident light. At low intensity, EQE reaches up to 6.5×10^{10}%, presenting a high number of electrons detected per incident photon. Last, I_{photo}/I_{dark} is extracted (Figure 5c). As the UV intensity increases, I_{photo}/I_{dark} experiences a slight increment from 1×10^2 to 2.5×10^2. The comparison of PDs device performance with the state-of-the-art printed UV detectors (Table S1, Supporting Information) displayed better sensing performance.

3. Conclusions

The development of a printing platform to incorporate conventionally manufactured and in-house thinned chips with advanced nanoscale electronic layers of nanowires was reported. The work also took advantage of direct ink write (DIW) printing to define the metal electrodes or interconnects to develop FHE system on a flexible substrate. The efficacy of each fabrication stage was tested by performing mechanical and electrical characterization tests. First, the excellent interfacial behavior between printed chip and substrate was tested by performing cyclic bending tests at 40, 30, and 20 mm radius. The experimental data showed robust interface between UTCs and substrate where no chip delamination/crack was observed after bending cycles were performed. Further, reliability and influence of direct transfer printing process on UTCs was evaluated by studying the n-channel MOSFETs performance before and after printing process. The small variation of transistor performance parameters of 14 MOSFETs from 3 different printed chips confirmed the efficacy of the optimized transfer printing approach. Finally, the superior grade quality of printed nanoscale electronic layers was demonstrated by constructing high performance UV photodetectors. We believe that the presented fabrication route will open new avenues for further progresses in the FHE field to meet the high-performance requirements of a wide range of applications.

4. Experimental Section

Chip Thinning: Ultrathin Si-based chips were obtained by using backside lapping with PMMA sacrificial technique. A detailed thinning optimization process was previously reported.[14] Briefly, a lapping machine was used to reduce Si chip's thickness. The PMMA was employed as a sacrificial layer to protect the front/device side during thinning and reduce the thermal stress during the chip separation process after thinning.

UTC Direct Transfer Printing: The custom-made contact printing set up[6d] was used to print chip-scale and nanoscale structures. First, the printing set-up was employed to perform direct transfer printing of UTCs. It is a single step printing process, unlike other traditional pick-and-place methods where an intermediate elastomeric stamp is crucial to perform the transfer process. For direct transfer printing process, first, PI substrates were obtained by spin-coating two layers of polyimide (PI), PI2611 from HD Microsystems, on rigid glass carriers. PI2611 was selected as its thermal expansion coefficient matches with that of Si (CTE_{PI} = 3 ppm per °C, CTE_{Si} = 3.2 ppm per °C) to prevent the chip damage/delamination during annealing.[3d,17] A semi-cured layer of PI was obtained to serve as an adhesive layer, prior to transfer printing by heating the PI at 90 °C for 3.5 min. This step was performed to ensure the chip is embedded successfully without defects. Next, UTC was brought into direct physical contact with the semi-cured PI receiver substrate. The applied contact force of 5 N was applied during direct transfer printing. The applied contact force was optimized to allow the UTC to be picked up and transfer printed directly on top of a semi cured PI layer on a glass substrate. After UTC transfer, PI was cured at 150 °C for 2 min before fully curing PI in an oven using slow ramp rate (4 °C min^{-1}) at 300 °C for 2 h.

ZnO Nanowires Synthesis: The ZnO NWs were grown using vapor liquid solid (VLS) mechanism. A vapor phase transport (VPT) method was performed inside a horizontal quartz tube furnace by carbothermal reduction of ZnO nanopowder on (0001) *c*-plane sapphire substrates. The details could be obtained from our previous publication.[5c] Briefly, the substrates were cleaned and coated with Au film (3 ± 1 nm) using an electron-beam evaporator. Coated substrates and the mixture of source material (ZnO and carbon powder at 1:1 weight ratio) were placed in an alumina "boat", which was inserted inside a high-temperature furnace. The samples were heated in an Ar ambient at 950 °C (growth on sapphire) for 120 min for the growth of ZnO NWs in the sub-100 nm diameter range.

Contact Printing of ZnO Nanowires: To achieve uniform assembly of nanoscale electronic layer, above-mentioned contact printing system was used. The details of the contact printing system used for NW printing are reported elsewhere.[6d] Briefly, a flat rigid donor substrate with vertically grown ZnO NWs was brought into physical contact with a receiver substrate. Then, a controlled uniform pressure (33 kPa) was exerted between the donor and receiver and subsequently the donor substrate was made to slide over the receiver substrates, at a 0.1 mm s^{-1} speed, while maintaining the applied pressure.

Electrode and Interconnects Realization Via DIW Printing: Electrical connections were formed by using a single-step extrusion based DIW printing technique (XTPL Delta Printing System) to fabricate nanowire-based photodetectors and access the MOSFET devices on the flexible PI substrate. Silver nano paste (CL85) with high viscosity (over 100 000 cP) and metal content (above 82%) was used as the printing material. In the case of chip bonding, interconnects were required to overcome the chip step height by increasing the nozzle to substrate distance along the *Z*-axis during printing. A more detailed study has been published previously.[1a] In the case of realizing fully printed PDs, the nozzle to substrate distance was kept at 1 µm to prevent the NWs from shifting and damaging during printing. The key printing parameters include the magnitude of pressure (7 bars) and printing velocity (0.02 mm s^{-1} for chip bonding, 0.05 mm s^{-1} for PD printing). Last, devices were annealed at 250 °C for 15 min to improve the ink conductivity.

Electrical Characterization: Electrical characterizations of the transfer printed UTCs and UTCs with printed interconnects as well as fully printed PDs were conducted in ambient and dark environment using Cascade Micro-tech Auto-guard probe station interfaced to a semiconductor parameter analyzer (B1500A, Agilent). A UV light-emitting diode (LED) with the wavelength of 365 nm was used to evaluate the photodetection of the fabricated devices. As the reliability of the optimized thinning technique has been confirmed by previously published studies, this work is mainly focused on the electrical characterization on the devices before and after transfer printing.[1a,4a,14] The mechanical bending stress was applied on the sample using a commercial setup (Yuasa System DMLHP-TW).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

A.C. and S.M. contributed equally to this work. This work was supported by Engineering and Physical Sciences Research Council through

Engineering Fellowship for Growth (EP/R029644/1) and Hetero-print Programme Grant (EP/R03480X/1). The work in this paper started when R.D. was with University of Glasgow, where his group was known as Bendable Electronics and Sensing Technologies (BEST) Group. The work was completed after he moved to Northeastern University, where his research group is known as Bendable Electronics and Sustainable Technologies (BEST) Group.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

contact printing, direct ink writing, direct transfer printing, hybrid electronics, nano to chip scale, nanowires, ultrathin chips

Received: October 4, 2022
Revised: November 8, 2022
Published online: December 23, 2022

[1] a) S. Ma, Y. Kumaresan, A. S. Dahiya, R. Dahiya, *Adv. Electron. Mater.* **2022**, *8*, 2101029; b) Z. Li, S. Chang, S. Khuje, S. Ren, *ACS Nano* **2021**, *15*, 6211; c) J. A. Rogers, X. Chen, X. Feng, *Adv. Mater.* **2020**, *32*, 1905590; d) Y. Ma, Y. Zhang, S. Cai, Z. Han, X. Liu, F. Wang, Y. Cao, Z. Wang, H. Li, Y. Chen, X. Feng, *Adv. Mater.* **2020**, *32*, 1902062; e) H.-R. Lim, H. S. Kim, R. Qazi, Y.-T. Kwon, J.-W. Jeong, W.-H. Yeo, *Adv. Mater.* **2020**, *32*, 1901924; f) Y. Khan, A. Thielens, S. Muin, J. Ting, C. Baumbauer, A. C. Arias, *Adv. Mater.* **2020**, *32*, 1905279; g) Y. Khan, M. Garg, Q. Gui, M. Schadt, A. Gaikwad, D. Han, N. A. D. Yamamoto, P. Hart, R. Welte, W. Wilson, S. Czarnecki, M. Poliks, Z. Jin, K. Ghose, F. Egitto, J. Turner, A. C. Arias, *Adv. Funct. Mater.* **2016**, *26*, 8764.

[2] a) D. A. van den Ende, H. J. van de Wiel, R. H. L. Kusters, A. Sridhar, J. F. M. Schram, M. Cauwe, J. van den Brand, *Microelectron. Reliab.* **2014**, *54*, 2860; b) C. Harendt, J. Kostelnik, A. Kugler, E. Lorenz, S. Saller, A. Schreivogel, Z. Yu, J. N. Burghartz, *Solid-State Electron.* **2015**, *113*, 101; c) C. García Núñez, L. Manjakkal, R. Dahiya, *npj Flexible Electron.* **2019**, *3*, 1; d) H. Nassar, R. Dahiya, *Adv. Intell. Syst.* **2021**, *3*, 2100102; e) J. Biggs, J. Myers, J. Kufel, E. Ozer, S. Craske, A. Sou, C. Ramsdale, K. Williamson, R. Price, S. White, *Nature* **2021**, *595*, 532; f) W. T. Navaraj, S. Gupta, L. Lorenzelli, R. Dahiya, *Adv. Electron. Mater.* **2018**, *4*, 1700277.

[3] a) A. S. Dahiya, D. Shakthivel, Y. Kumaresan, A. Zumeit, A. Christou, R. Dahiya, *Nano Convergence* **2020**, *7*, 33; b) S. Khan, L. Lorenzelli, R. S. Dahiya, *IEEE Sens. J.* **2015**, *15*, 3164; c) S. Gupta, W. T. Navaraj, L. Lorenzelli, R. Dahiya, *npj Flexible Electron.* **2018**, *2*, 969; d) R. S. Dahiya, S. Gennaro, *IEEE Sens. J.* **2013**, *13*, 4030.

[4] a) S. Ma, Y. Kumaresan, A. S. Dahiya, L. Lorenzelli, R. Dahiya, *IEEE Sens. J.* **2022**, https://doi.org/10.1109/JSEN.2022.3140651; b) M. S. Baghini, A. Vilouras, R. Dahiya, *IEEE Trans. Biomed. Circuits Syst.* **2022**, *15*, 1174; c) A. Vilouras, A. Christou, L. Manjakkal, R. Dahiya, *ACS Appl. Electron. Mater.* **2020**, *2*, 2601; d) S. Gupta, W. T. Navaraj, L. Lorenzelli, R. Dahiya, *npj Flexible Electron.* **2018**, *2*, 8.

[5] a) A. Zumeit, A. S. Dahiya, A. Christou, R. Mukherjee, R. Dahiya, *Adv. Mater. Technol.* **2022**, *7*, 2200772; b) J. Neto, R. Chirila, A. S. Dahiya, A. Christou, D. Shakthivel, R. Dahiya, *Adv. Sci.* **2022**, *9*, 2201525; c) A. S. Dahiya, A. Christou, J. Neto, A. Zumeit, D. Shakthivel, R. Dahiya, *Adv. Electron. Mater.* **2022**, *8*, 2200170.

[6] a) A. S. Dahiya, A. Zumeit, A. Christou, R. Dahiya, *Adv. Electron. Mater.* **2022**, *8*, 2200098; b) A. Zumeit, A. S. Dahiya, A. Christou, D. Shakthivel, R. Dahiya, *npj Flexible Electron.* **2021**, *5*, 18; c) A. Zumeit, A. S. Dahiya, A. Christou, R. Dahiya, *Jpn. J. Appl. Phys.* **2022**, *61*, SC1042; d) A. Christou, F. Liu, R. Dahiya, *Microsyst. Nanoeng.* **2021**, *7*, 98; e) A. Zumeit, W. T. Navaraj, D. Shakthivel, R. Dahiya, *Adv. Electron. Mater.* **2020**, *6*, 1901023; f) K. Sim, S. Chen, Z. Li, Z. Rao, J. Liu, Y. Lu, S. Jang, F. Ershad, J. Chen, J. Xiao, C. Yu, *Nat. Electron.* **2019**, *2*, 471; g) C. Linghu, S. Zhang, C. Wang, J. Song, *npj Flexible Electron.* **2018**, *2*, 26; h) C. García Núñez, F. Liu, W. T. Navaraj, A. Christou, D. Shakthivel, R. Dahiya, *Microsyst. Nanoeng.* **2018**, *4*, 22; i) J.-K. Chang, H.-P. Chang, Q. Guo, J. Koo, C.-I. Wu, J. A. Rogers, *Adv. Mater.* **2018**, *30*, 1704955; j) A. Javey, Nam, R. S. F. , H. Yan, C. M. Lieber, *Nano Lett.* **2007**, *7*, 773; k) K. Kim, B. Kim, C. H. Lee, *Adv. Mater.* **2020**, *32*, 1902051.

[7] a) F. Liu, S. Deswal, A. Christou, M. Shojaei Baghini, R. Chirila, D. Shakthivel, M. Chakraborty, R. Dahiya, *Sci. Rob.* **2022**, *7*, eabl7286; b) Z. Fan, J. C. Ho, Z. A. Jacobson, R. Yerushalmi, R. L. Alley, H. Razavi, A. Javey, *Nano Lett.* **2008**, *8*, 20.

[8] R. Dahiya, G. Gottardi, N. Laidani, *Microelectron. Eng.* **2015**, *136*, 57.

[9] Y. Sun, H.-S. Kim, E. Menard, S. Kim, I. Adesida, J. A. Rogers, *Small* **2006**, *2*, 1330.

[10] C. Guo, Z. Pan, C. Li, S. Zou, C. Pang, J. Wang, J. Hu, Z. Gong, *npj Flexible Electron.* **2022**, *6*, 44.

[11] Z. Lu, P. C. Y. Chen, W. Lin, *IEEE Trans. Syst., Man Cybern., C Appl. Rev.* **2006**, *36*, 713.

[12] T.-H. Cheng, C.-C. Du, C.-H. Tseng, *J. Mater. Process. Technol.* **2006**, *172*, 407.

[13] a) M. J. Christoe, J. Yuan, A. Michael, K. Kalantar-Zadeh, *IEEE Access* **2021**, *9*, 85144; b) M. J. Christoe, J. Han, K. Kalantar-Zadeh, *Adv. Mater.* **2020**, *5*, 1900733.

[14] Y. Kumaresan, S. Ma, R. Dahiya, *Microelectron. Eng.* **2021**, *247*, 111588.

[15] C. Liang, F. Wang, Z. Huo, B. Shi, Y. Tian, D. Zhang, *Soft Matter* **2021**, *17*, 4989.

[16] W. Christiaens, E. Bosman, J. Vanfleteren, *IEEE Trans. Compon. Packag. Technol.* **2010**, *33*, 754.

[17] W. Christiaens, E. Bosman, J. Vanfleteren, *IEEE Trans. Compon. Packag., Manuf. Technol.* **2010**, *33*, 754.

[18] N. E. Persson, J. Rafshoon, K. Naghshpour, T. Fast, P.-H. Chu, M. McBride, B. Risteen, M. Grover, E. Reichmanis, *ACS Appl. Mater. Interfaces* **2017**, *9*, 36090.

[19] H. Liu, Z. Liu, Z. Xu, Z. Yin, Y. Huang, J. Chen, *ASME. J. Appl. Mech.* **2015**, *82*, 101012.