Guan, Y., Georgiev, V. P., Asenov, A., Liang, F. and Chen, H. (2022) Impact of the Figures of Merit (FoMs) definitions on the variability in nanowire TFET: NEGF simulation study. IEEE Transactions on Electron Devices, 69(11), pp. 6394-6399.

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# Impact of the Figures of Merit (FoM) Definitions on the Variability in Nanowire TFET: NEGF Simulation Study

Yunhe Guan, Vihar P. Georgiev, *Senior Member*, *IEEE*, Asen Asenov, *Fellow*, *IEEE*, Feng Liang, and Haifeng Chen

***Abstract*—In this paper we investigate the effect of variability in p-type nanowire Tunnel FET (TFET) using quantum mechanical transport simulations. The simulations have been carried out using the Nano Electronics Simulation Software (NESS) from the University of Glasgow. Random discrete dopants and work-function variations have been investigated in the simulations. Our statistical simulations reveal that key Figures of Merit (FoM) such as the current variability generally decreases as the gate voltage decreases, the threshold voltage variability increases as the threshold current increases, and the dependences of these FoM variabilities on criteria become stronger with the switch characteristic ameliorated. Furthermore, it is interesting to find that the band-offset in heterostructure can more or less alleviate the current variability, especially around the off-state.**

***Index Terms*—Criteria of Figures of Merit, Nanowire Tunnel FET, Quantum simulation, Random discrete dopants (RDD), Variability, Work-function variations (WFV).**

## I. Introduction

Tunnel FETs (TFETs) are being considered as a promising candidate for low power applications in future technology nodes due to their capability to overcome the thermionic subthreshold slope limitation delivering sub-60mV/decade sunthreshold swing (SS) [1]. It has been shown that the diameter of III-V nanowires can be reduced down to a few nanometers [2], as reported by Lund university reaching 7 nm in III-V TFET by using digital etching technique [3]. For these truly nanometric size devices, dominated by the quantum mechanical effects, the performance variabilities induced by the discreteness of charge and granularity of matter have emerged as crucial concerns for their integration in billions of transistors count chips [4]-[6].

The previous studies covering the variability aspect in TFET, mainly focus on statistical variations of the Figures of Merit (FoM) which are defined by some fixed criteria [5]-[9]. Opposite to MOSFETs, the TFETs have SS that are no longer linear on a logarithmic scale [1], meaning that the FoM criteria should have influence on the variability. However, the impact of the definition of the FoM on the variability is missing from previous reports. This obscures the variability issue in TFETs when operating under different biasing conditions and the device optimization in terms of statistical variability and reliability.

In this paper, using quantum simulations, we have studied the correlation between the definition criteria and the statisical variations of the main FoM in p-type nanowire TFETs under the influences of random discrete dopants (RDD) and work-function variations (WFV). This paper is organized as follows. In Section 2, the device design and the simulation methodology are described. In Section 3, the dependence of drain current ($I_{ds}$) and threshold voltage ($V_{th}$) variations on the gate bias and threshold current criteria, are respectively analyzed under different source doping, structure, and metal-grain size. Finally, the conclusions are drawn in Section 4.

## II. Device Description and Methodology

The p-type InAs nanowire TFETs considered in this work under the influence of RDD and WFV are illustrated in Fig. 1(a) and (b) respectively. The surface roughness (SR) is not considered here due to that it presents less variability as presented in our previous work [10], [11]. Whereas, the SR shows relatively obvious impact on nanowire TFET in Ref. [12]. The different observations can be attributed to the difference of device type adopted. The device in our work is p-type, and in Ref. [12] it is n-type. It should be noted that the channel subband fluctuations are responsible for the impact of SR, since source subband appears relatively smoother due to

This work was supported in part by the National Natural Science Foundation of China under Grants 61474093 and 62104192, Natural Science Basic Research Program of Shaanxi Province under Grant 2020JM-581 and Grant 2021JQ-717. This project has also received funding from EPSRC UKRI Innovation Fellowship scheme under grant agreement No. EP/S001131/1 (QSEE) and EPSRC UKRI with grant agreement No. EP/P009972/1 (QUANTDEVMOD) (Corresponding author: Yunhe Guan.)

Y. Guan and H. Chen are with the School of Electronic Engineering, Xi’an University of Posts & Telecommunications, Xi’an 710121, Shaanxi, P. R. China (e-mail: gyhflc@xupt.edu.cn).

V. P. Georgiev and A. Asenov are with the James Watt School of Engineering, University of Glasgow, Glasgow G12 8LT, U.K.

F. Liang is with the School of Microelectronics, Xi’an Jiaotong University, Xi’an 710049, Shaanxi, P. R. China.

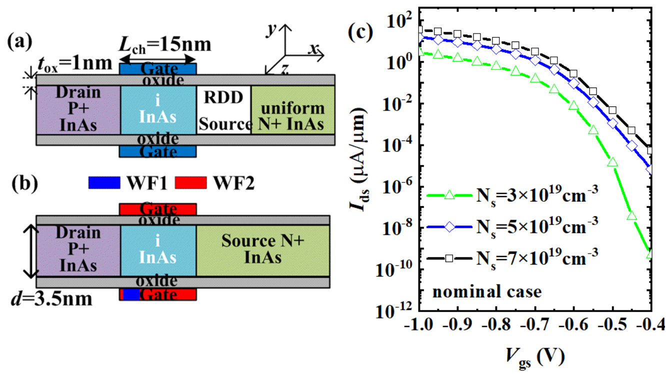


Fig. 1. Sketch of a nanowire InAs TFET with (a) RDD and (b) WFV configurations. (c) Nominal $I_{\mathrm{ds}}-V_{\mathrm{gs}}$ characteristics under various source dopings. $L_{\mathrm{ch}}$ =15nm, $d$ =3.5nm, $t_{\mathrm{ox}}$ = 1nm, and $V_{\mathrm{ds}}=-0.5$V.

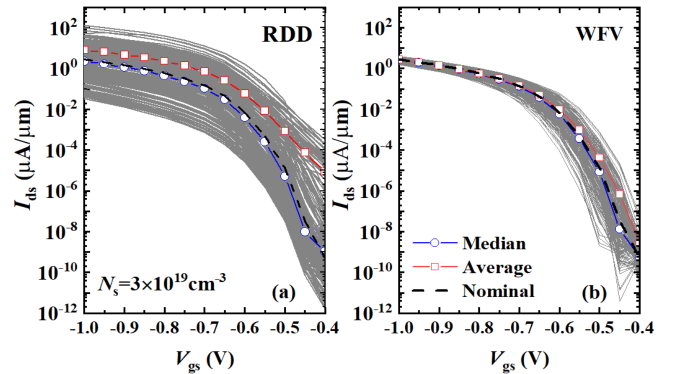


Fig. 2. The individual influence of (a) RDD and (b) WFV on the $I_{ds}-V_{gs}$ characteristics of an ensemble of 200 nanowire TFETs. The nominal, median and average data are also shown. $N_s=3\times10^{19}\mathrm{cm}^{-3}$.

the macroscopic band bending [12]. Thus, for p-type (n-type) device, it is channel valence (conduction) subband which has a relatively larger (smaller) effective mass that plays a primary role in terms of variability, thus the impact of quantum confinement by SR is small (large). The simulated nanowire diameter is $d$ =3.5nm, the channel length is $L_{\mathrm{ch}}$ =15nm, and the high-k oxide thickness is $t_{\mathrm{ox}}$ = 1nm with a relative dielectric constant $\varepsilon$ =9. The acceptor-type drain region is doped with $N_{\mathrm{d}}=5\times10^{19}\mathrm{cm}^{-3}$. The values of the effective mass in Ref. [11] are adopted for confined InAs materials. The channel is intrinsic and the doping profiles are assumed to be abrupt between the reservoirs and the channel. The drain-to-source voltage $V_{\mathrm{ds}}$ is set to -0.5V, unless otherwise specified. Fig. 1(c) shows the nominal $I_{\mathrm{ds}}-V_{\mathrm{gs}}$ characteristics under various donor-type source doping $N_{\mathrm{s}}$.

Details on the generation of nanowires with random RDD and WFV configurations can be found in Refs. [11] and [7], respectively. The RDD region is 10 nm long, as shown in Fig. 1(a), preceded by a uniform doped region required for numerical stability. The WFV-induced variability is introduced by the random grain orientations found in the TiN gate-all-around contact, as shown in Fig. 1(b) [13]. As like in Refs. [14] and [5] with nanowire structure, the TiN metal with two distinct grain orientations, which are set with 60% and 40% occurring probability and meaningful work-function difference of 0.2 eV [15], has been adopted. However, the selected work function values are not always consistent [5], [14]. They are respectively set as 5.3 eV and 5.1 eV for convergence purpose here. Although the choice of work function value or probability distribution will change the variability, the variation trends of variability will not be influenced. For example, the envelopes of variability are same when comparing the cases with two different groups of work function values [16]. The objective of this paper is to provide the dependence of variability on the bias or current criteria, and this is a trend analysis as like in Refs. [14] and [5]. Thus, we believe the work-function values or probability distributions have no influence on our conclusion. The default value of the average metal grain size is set to 3 nm. Simulations are carried out by employing the quantum transport module in NESS [11], [17], [18]. In order to accurately compute the band-to-band tunneling current in the ultra-scaled nanowire, the two-band Flietner model of the imaginary dispersion is used in combination with the couple mode-space NEGF approach [17]. The electron–phonon interactions are neglected since the tunneling in the studied devices is mainly direct, as reported in Ref. [11]. The accuracy of results from NESS has been previously verified by comparing with that from the atomistic tool OMEN [17]. In these extreme narrow nanowires, the majority of the electrons/holes are located in the lowest/highest conduction/valence subbands. Then, changing the number of conduction/valence subbands from 4, 8 up to 12 did not bring any additional novelties on our findings. For sake of saving on computational time, the simulations presented in this paper were carried out with 4 subbands for each carrier valley.

## III. Results and Discussions

In order to carry out a reliable statistical analysis of variability introduced by RDD and WFV, ensembles of 200 nanowire TFETs have been simulated for various $N_{\mathrm{s}}$ first. As an example, Figs. 2(a) and 2(b) show the $I_{\mathrm{ds}}-V_{\mathrm{gs}}$ characteristics of each of the 200 TFETs subject to the RDD and WFV variability for $N_s=3\times10^{19}\mathrm{cm}^{-3}$, respectively. The nominal, average and median characteristics are also shown. It can be found that RDD has stronger impact on the variability of the $I_{\mathrm{ds}}-V_{\mathrm{gs}}$ characteristics in comparison to WFV. In order to analyze the effect of OFF/ON-bias criteria, the dependences of the $I_{\mathrm{ds}}$ variation induced by RDD on the gate voltage under various $N_{\mathrm{s}}$ is presented in Fig. 3. It should be noted that the coefficient of variation (CV), defined as normalized deviation σ/μ, is used to quantify the performance difference under different parameters, as adopted in Ref. [19]. σ and μ are the standard deviation and mean value of the corresponding FoM. From Fig. 3, it can be found that CV($I_{\mathrm{ds}}$) generally decreases with the decrease of $V_{\mathrm{gs}}$ for each $N_s$. For example, CV($I_{\mathrm{ds}}$) is 2.23, 1.46, and 1.18 at $V_{\mathrm{gs}}=-0.45$V, $-0.6$V, and $-0.9$V under $N_{\mathrm{s}}=5\times10^{19}\mathrm{cm}^{-3}$, which means that the current around the OFF-state are more susceptible to the variability than those around the On-state. This indeed is consistent with the current distribution in Fig. 2. When TFET is biased around its ON/OFF-state, the electrical field near the tunneling junction is high/small, and the power law/exponential dependence of transmission on the electrical filed dominates the current [20]. As a result, the influence of the electrical field fluctuation resulted from RDD and thus the variation of current around the ON/OFF-state is relatively weaker/stronger.

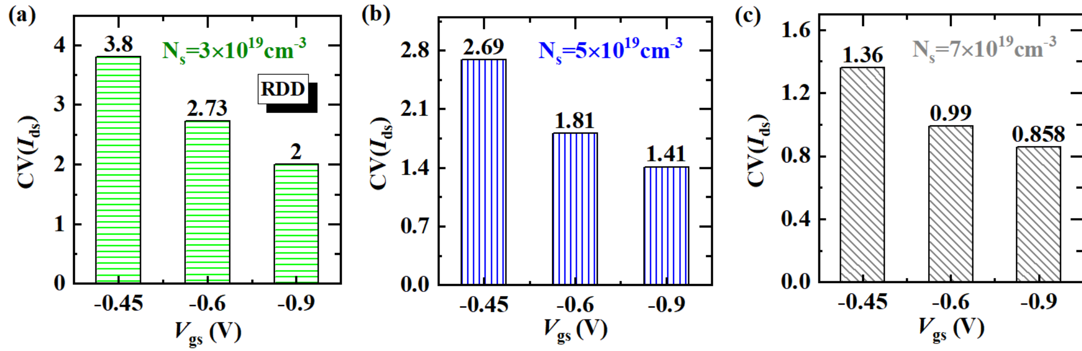


Fig. 3. Dependences of normalized current variation by RDD on $V_{gs}$ under (a) $N_s = 3 \times 10^{19}\text{cm}^{-3}$, (b) $N_s = 5 \times 10^{19}\text{cm}^{-3}$, and (c) $N_s = 7 \times 10^{19}\text{cm}^{-3}$ in InAs TFET.

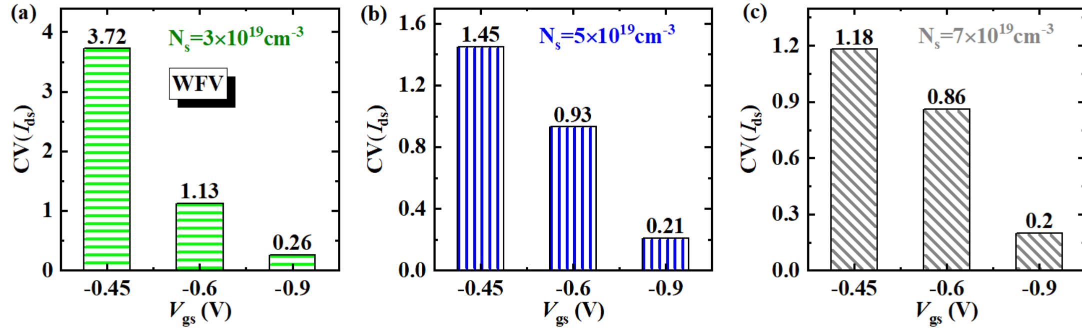


Fig. 4. Dependences of normalized current variation by WFV on $V_{gs}$ under (a) $N_s = 3 \times 10^{19}\text{cm}^{-3}$, (b) $N_s = 5 \times 10^{19}\text{cm}^{-3}$, and (c) $N_s = 7 \times 10^{19}\text{cm}^{-3}$ in InAs TFET.

Fig. 4 shows the dependences of the normalized variability of $I_{\text{ds}}$ due to WFV on the gate voltage under various $N_{\text{s}}$. The same tendency is observed as in Fig. 3, with the relative variability becoming weak as $V_{\text{gs}}$ decreases. This can also be explained by our analyses above. Comparing the quantitative data in Figs. 3 and 4, the CV($I_{\text{ds}}$) at -0.9V of $V_{\text{gs}}$ under WFV influence is around 0.2, much smaller than the variability under RDD influence. It reveals clearly that the current at lower $V_{\text{gs}}$ is less affected by WFV compared to RDD.

From both of Figs. 3 and 4, it can be found that higher source doping reduces the current variations in InAs TFET. At $V_{\text{gs}} = -0.6\text{V}$, CV($I_{\text{ds}}$) induced by RDD (WFV) decreases from 2.73 (1.13) to 1.81 (0.93) when $N_{\text{s}}$ increases from $3 \times 10^{19}\text{cm}^{-3}$ to $5 \times 10^{19}\text{cm}^{-3}$. For the RDD case, this is partially due to the larger number of the doping atom when $N_{\text{s}}$ is higher, which reduces the normalized fluctuation of dopants $N_{\text{s}}$ i.e., $\sigma(N)/N = (N_{\text{s}} \times V_{\text{rdd}})^{-1/2}$ [21] (where $V_{\text{rdd}}$ is the volume of RDD region), and thus reduce the RDD impact. Additionally, for higher $N_{\text{s}}$, the worse SS feature as shown in Fig. 1(c) also contributes to reducing the RDD influence due to the weak dependence of current on the bias and thus the band profile. The latter is also responsible for the reduction of the variation due to WFV under high $N_{\text{s}}$. Moreover, the worse SS feature under the higher $N_{\text{s}}$ also reduces the dependence of CV($I_{\text{ds}}$) on $V_{\text{gs}}$ since the point SS changes less significantly. It should be noted again that the whole SS characteristic becomes inferior when $N_{\text{s}}$ is larger as shown in Fig. 1(c), so there exists some trade-off between the switch characteristic and the variability in TFETs when choosing $N_{\text{s}}$.

The standard deviation of the threshold voltage ($V_{\text{th}}$) considering RDD and WFV under different threshold current

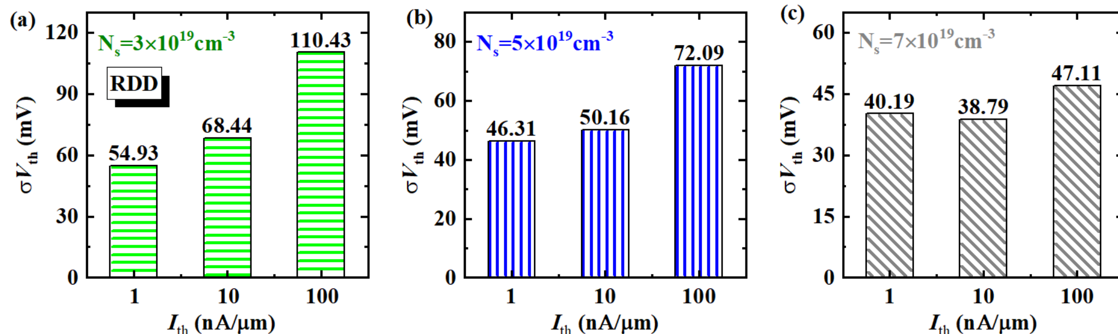


Fig. 5. Threshold voltage variation considering RDD vs. $I_{\text{th}}$ under (a) $N_s = 3 \times 10^{19}\text{cm}^{-3}$, (b) $N_s = 5 \times 10^{19}\text{cm}^{-3}$, and (c) $N_s = 7 \times 10^{19}\text{cm}^{-3}$ in InAs TFET.

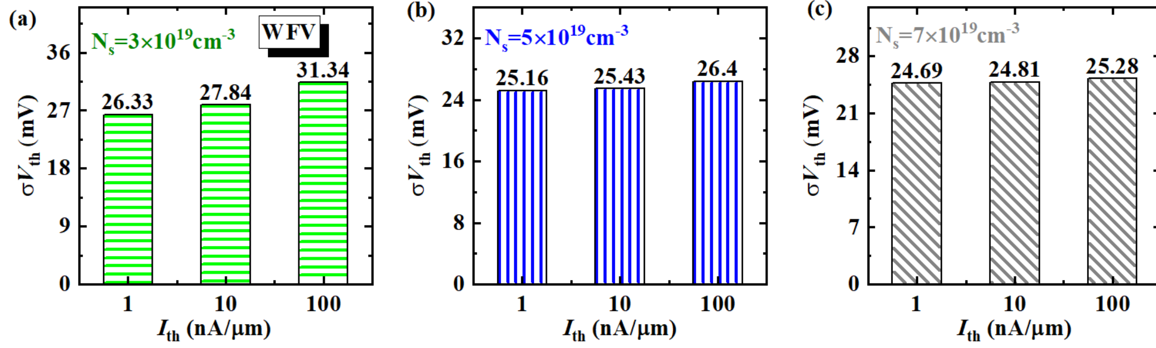


Fig. 6. Threshold voltage variation considering WFV vs. $I_{\mathrm{th}}$ under (a) $N_s = 3\times10^{19}\mathrm{cm}^{-3}$, (b) $N_s = 5\times10^{19}\mathrm{cm}^{-3}$, and (c) $N_s = 7\times10^{19}\mathrm{cm}^{-3}$ in InAs TFET.

($I_{\mathrm{th}}$) criteria is shown in Figs. 5 and 6, respectively. For simplicity, the constant current method is used to define $V_{\mathrm{th}}$, as done in Refs. [8] and [11]. With the increase of $I_{\mathrm{th}}$, $\sigma(V_{\mathrm{th}})$ increases under no matter the impact of RDD or WFV. For example, $\sigma(V_{\mathrm{th}})$ induced by RDD is 54.93mV, 68.44mV, and 110.43mV when $I_{\mathrm{th}}$ is chosen, respectively, at 1nA/μm, 10nA/μm, and 100nA/μm at $N_{\mathrm{s}} = 3\times10^{19}\mathrm{cm}^{-3}$ . The corresponding quantities are reduced to 26.33mV, 27.84mV, and 31.34mV respectively in the WFV case. Because the gate control generally becomes weaker when $I_{\mathrm{th}}$ is higher, it needs more gate voltages to reach the criteria condition when the transfer curve shifts from the nominal one due to the influence of variability. Hence, $\sigma(V_{\mathrm{th}})$ becomes larger with $I_{\mathrm{th}}$. This suggests that the statistical variation in $V_{\mathrm{th}}$ can be reduced by designing TFET with $I_{\mathrm{th}}$ appearing at the point where gate-control is stronger or point SS is relatively smaller. It can also be found that the dependence of $\sigma(V_{\mathrm{th}})$ on $I_{\mathrm{th}}$ also becomes weaker when $N_{\mathrm{s}}$ varies from $3\times10^{19}\mathrm{cm}^{-3}$ to $7\times10^{19}\mathrm{cm}^{-3}$, as the case in the current variation shown in Figs. 3 and 4, which can also be explained by the previous analyses.

Since the heterostructure can improve the on-state current of TFETs, it is worth investigating the related variabilities in heterojunction TFET (HTFET). Fig. 7(a) shows the nominal $I_{\mathrm{ds}} - V_{\mathrm{gs}}$ curve of the InAs/Si HTFET. Figs. 7(b) and 7(c) depict the dependence of variation in $I_{\mathrm{ds}}$ and $V_{\mathrm{th}}$ of HTFET on $V_{\mathrm{gs}}$ and $I_{\mathrm{th}}$ respectively, under the influence of RDD. In the HTFET, the channel and drain materials are Si, and the doping in the drain is $N_{\mathrm{d}} = 2\times10^{20}\mathrm{cm}^{-3}$. Other device parameters are the same as those in Fig. 1(a), including the configuration of RDD. As comparison, the corresponding $I_{\mathrm{ds}} - V_{\mathrm{gs}}$ curve and current variation of the InAs homojunction TFET from Fig. 1(c) and Fig. 3(b) are also replotted in Fig. 7(a) and (b), respectively. As can be seen from Fig. 7(a), the HTFET not only can deliver high on-current, such as $I_{\mathrm{ds}}$ at $V_{\mathrm{gs}} = -0.9\mathrm{V}$ is 3.5× of that in InAs TFET, but also has a steeper switch characteristic [22], [23]. From Figs. 7(b) and 7(c), $\mathrm{CV}(I_{\mathrm{ds}})$ also decreases with the decrease of $V_{\mathrm{gs}}$, and $\sigma(V_{\mathrm{th}})$ increases with the increase $I_{\mathrm{th}}$. Furthermore, from Fig.7(b), it can be said that the heterostructure is superior to the homostructure in terms of the current variability. The weaker $I_{\mathrm{ds}}$ variability in the HTFET at $V_{\mathrm{gs}}$ of -0.6V and -0.9V can be mainly attributed to its steeper switch characteristic, since then the device is within the weaker gate-control region as shown in Fig. 7(a), and thus the current is less suspectable to the variation in the band profile around tunneling junction. The $\mathrm{CV}(I_{\mathrm{ds}})$ at $V_{\mathrm{gs}}$ of -0.45V in the HTFET (2.72) is higher than that in InAs TFET (2.69) but not much although the point SS in the former is much smaller. We believe that it is the band-offset between the source and channel materials that mitigate the severe variation in $I_{\mathrm{ds}}$ at steeper point in HTFET. It should be noted that the offset band is not affected by RDD. Thus, the influence of RDD on the tunneling junction will be partially weakened when the offset-band is within the tunneling window. This means that the band-offset and the consequent stronger gate-control or steeper switch characteristic, lead to opposite effects on the current variability, counteracting each other's influence. As expected, the

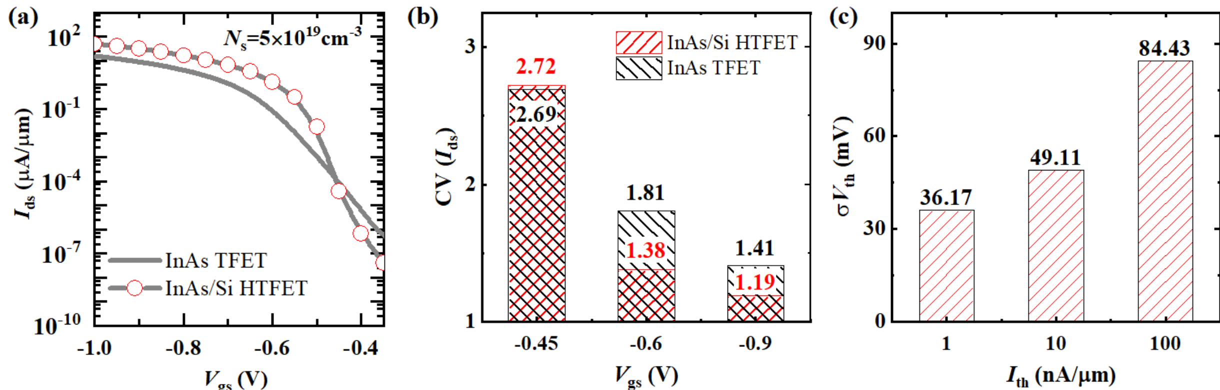


Fig. 7. (a) Comparison of the nominal $I_{\mathrm{ds}} - V_{\mathrm{gs}}$ curve of InAs/Si HTFET to that of InAs TFET under $N_s = 5\times10^{19}\mathrm{cm}^{-3}$. (b) Histograms of $\mathrm{CV}(I_{\mathrm{ds}})$ vs. $V_{\mathrm{gs}}$ and (c) $\sigma(V_{\mathrm{th}})$ vs. $I_{\mathrm{th}}$ under the influence of RDD. For simplicity, the $\mathrm{CV}(I_{\mathrm{ds}})$ vs. $V_{\mathrm{gs}}$ data from Fig. 3(b) is also replotted in Fig. 7(b).

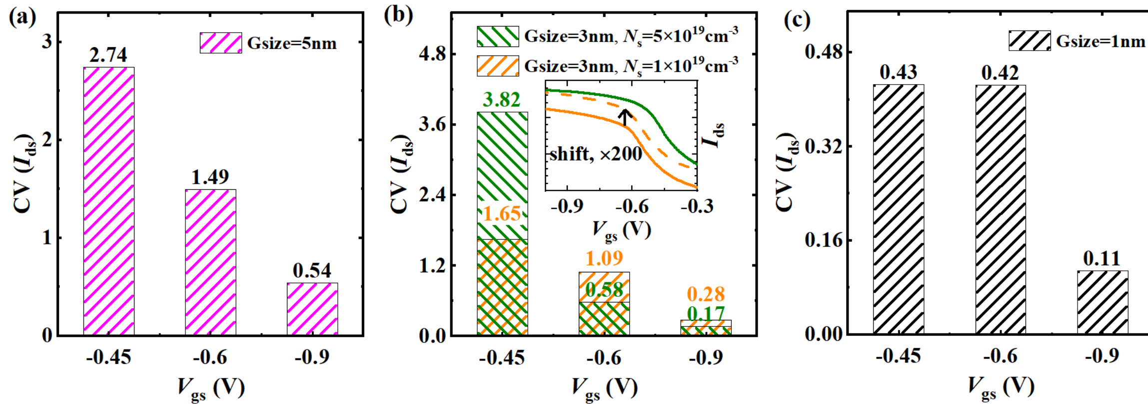


Fig. 8. Dependences of normalized current variation by WFV on gate voltage in InAs/Si HTFET under (a) Gsize = 5nm, (b) Gsize = 3nm, and (c) Gsize = 1nm. $N_s = 1\times10^{19}\text{cm}^{-3}$ and $V_{ds} = -1.0\text{V}$ . Fig. 8(b) also shows the case under $N_s = 5\times10^{19}\text{cm}^{-3}$ to emphasize the influence of band-offset in heterostructure when compared with homostructure. The inset in Fig. 8(b) plots the nominal $I_{ds} - V_{gs}$ curves of InAs/Si HTFET under $N_s = 5\times10^{19}\text{cm}^{-3}$ and $1\times10^{19}\text{cm}^{-3}$, and the dashed line is just the shifting result for comparison

dependence of $\sigma(V_{th})$ on $I_{th}$ is also stronger in the HTFET compared with that in the homojunction TFET, by comparing Figs. 5(b) and 7(c).

Considering that the lower grain size can be achieved, such as by incorporation of C or copper into TiN mental to make an amorphous film [5], [24], it is also interesting to study the dependence of FoM on criteria under the influence of WFV with different grain size, especially in the potential HTFET. Fig. 8 shows the histograms of CV($I_{ds}$) vs. $V_{gs}$ under Gsize = 5nm, 3nm, and 1nm in InAs/Si HTFET with $N_s = 1\times10^{19}\text{cm}^{-3}$. As previous reported in Refs. [5] and [7], the influence of WFV on $I_{ds}$ becomes gradually weak as the decrease of grain size due to the lower impact on energy barrier. The experimental result reported in Ref. [25] also confirms that using the amorphous metal gate is effective to suppress the influence of WFV. However, due to the limitation of cost and low deposition rate in atom-layer deposition process, which is suitable for the growth of amorphous metal in nanowire or FinFET structures [26], the conventional physical vapor deposition methods are still used in nanowire [27] despite it having the limitation of conformality and thickness control. This may cause the grown metal materials always composed of several crystal grains with distinct orientations and are not completely amorphous [5], [28], meaning that there are still some influences of WFV even in the "amorphous" case. As can be seen from Fig. 8, the CV($I_{ds}$) decreases with $V_{gs}$ in all cases. Fig. 8(b) also plots the CV($I_{ds}$) under $N_s = 5\times10^{19}\text{cm}^{-3}$ to do indicate the influence of band-offset in heterojunction on the variability. The corresponding nominal $I_{ds} - V_{gs}$ curves are shown in the inset of Fig. 8(b), and the dashed line shows the result shifting from the data of $N_s = 1\times10^{19}\text{cm}^{-3}$ just for comparison. It is obvious that the HTFET under $N_s = 5\times10^{19}\text{cm}^{-3}$ turns on faster than that under $N_s = 1\times10^{19}\text{cm}^{-3}$. Thus, the much steeper point at $V_{gs}$ of -0.45V in the former causes the very stronger fluctuation in the current (3.82 vs 1.65 for CV($I_{ds}$)). This is different from the comparison result in Fig. 7(b) with a comparable current variation at $V_{gs}$ of -0.45V although the SS features are also distinct between the two devices. It should be noted that the two devices in Fig. 8(b) are both heterostructures, meaning that the band-offset is no longer the advantage to the current variability. This demonstrates that the offset-band in the heterostructure can weaken the variation in the current, especially at the steep point, when compared with homostructure. Different from the case in InAs TFET, the stronger dependence of current variation on gate voltage occurs in the higher $N_s$ in HTFET from Fig. 8(b), which clarifies that it is the SS characteristic rather than the doping that determine the variability by WFV.

Interface traps are regarded as another important source of variability in TFET. It causes random telegraph noise [29]-[31] and trap-assisted tunneling (TAT) (the scattering influence from trap can be neglected due to TFETs are not sensitive to the mobility fluctuation [32], [33]) [34], [35]. For example, Ref. [36] modeled the influences of interface trap, and found that subthreshold region in transfer characteristics has a severer fluctuation in TFETs due to TAT. The experimental result in Ref. [37] shows that the individual nanowire Tunnel FETs has a significant variability at room temperature due to multiple factors including trap. Although the inclusion of interface trap can improve the reliability of the variability predicted, our purpose is to provide the variation tendency of variability rather than the realistic assessment of variability. Furthermore, the full-quantum simulation with inclusion of interface trap is computationally cumbersome in a large-scale statistical study like this. Thus, the inclusion of interface traps is not considered within our scope and simulation speed limitations. They can be the subject of future work.

## IV. Conclusion

The dependences of the variability in p-type nanowire TFETs under the influence of RDD and WFV on the definition of the main FoM have been investigated using quantum transport simulations. The $\boldsymbol{I_{ds}}$ variation is generally reduced with $\boldsymbol{V_{gs}}$, and the $\boldsymbol{V_{th}}$ variation is increases with $\boldsymbol{I_{th}}$ due to the gradually deteriorated SS in a TFET. This indicates that the performance variations are directly influenced by the criteria defining the FoM which could be different for different technologies. The dependence of the variability on criteria becomes stronger in the device with better SS characteristic, and the smaller the point SS, the corresponding current variation severer. In order to suppress the performance fluctuation of TFETs, adopting high $\boldsymbol{N_s}$ and amorphous metal

are effective methods in terms of RDD and WFV source of variability, respectively. Furthermore, it is interesting to find that the performance variation in heterostructure is comparable to that in homostructure although the former has a superior SS characteristic.

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