Reliable T-gate Process for THz HEMTs

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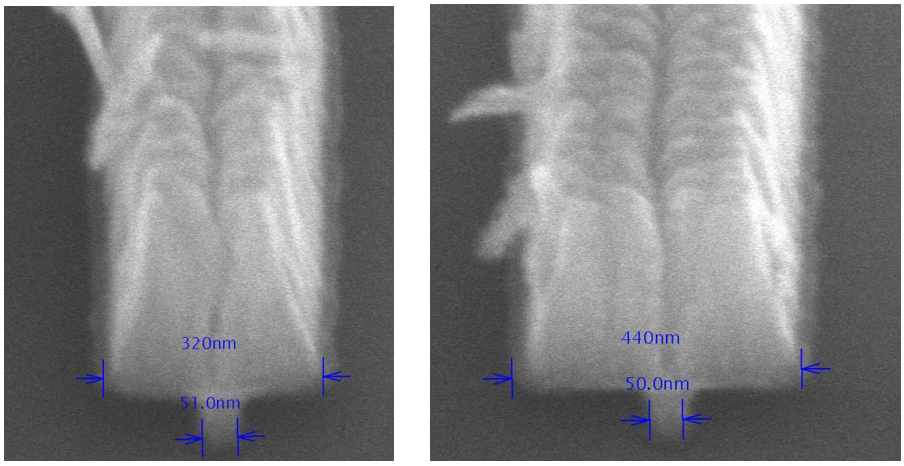
InP-based high electron mobility transistor (HEMT) with a 25 nm T-gate has recently been demonstrated amplifying at 1.1 THz [1], making the traditional electronic devices competitive over optical devices for terahertz applications. Although aggressively pushing the footprint of T-gate even shorter to achieve higher operating frequencies has now become a hot research topic, a robust and cost-effective T-gate process for sub-100 nm T-gate is still a priority for industry. In this paper, we will demonstrate our latest progress on process development of ultrashort T-gates at the University of Glasgow. The process involves a single electron beam lithography (EBL) exposure on a PMMA/LOR/CSAR tri-layer EBL resist stack. By carefully controlling resist thicknesses, E-beam dose, and appropriate developer and developing time, a reliable and robust process for T-gates with various foot and head lengths have been developed. Fig. 1 shows scanning electron microscopy (SEM) images of the typical T-gates on a GaAs semi-insulating substrate. The new process has several advantages over state-of-the-art T-gate processes[3][4] and it has a potential to further reduce the foot print to sub 20 nm for THz operation of HEMTs. We will elucidate the process in greater details at the conference.



(a) (b)

Fig.1 SEM images of T-gates (a) 50 nm foot and 330 nm head (b) 50 nm foot and 440 nm head. tilted 60 degrees.

References

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