Investigation of Al_2O_3, Si_3N_4 and SiO_2 used for surface passivation and gate dielectric on AlGaN/GaN metal-oxide-semiconductor high electron mobility transistors

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Abstract

In this work we report on the processing and device characteristics of AlGaN/GaN metal-oxide/insulator-semiconductor high electron mobility transistors (MOS-HEMTs) employing different types of dielectric layers such as SiO_2, Si_3N_4 and Al_2O_3. A device with a Schottky gate (HEMT structure) was also fabricated for comparison. The AlGaN/GaN MOS-HEMT device employing high-k Al_2O_3 material for surface passivation and gate dielectric demonstrated the highest maximum drain current density of over 1940 mA/mm and highest maximum peak transconductance of 240 mS/mm. This device also produces the lowest gate leakage current of $I_{GS} = 1x10^{-8}$ A/mm at V_{GS} = -9 V and the V_{BR} of over 200 V. These results indicate the high quality of Al_2O_3 material grown using atomic layer deposition (ALD). In contrast, devices employing PECVD (plasma-enhanced chemical vapour deposition) SiO_2 and Si_3N_4 demonstrate poor device performances compared to the Schottky gate structure. These results show the importance of applying a high quality insulator for surface passivation and gate dielectric of the AlGaN/GaN heterostructure.

Introduction

AlGaN/GaN high electron mobility transistors (HEMTs) are the group III-V materials with high breakdown electric field (> $3x10^6$ V/m), high electron mobility (2000 cm^2/Vs), high carrier concentration (> 10^{13} cm-2) and high saturated electron velocity ($2.5x10^7$ cm/s), which makes them the best candidate for high power applications, especially at high frequencies [1, 2]. However, these devices still suffer from problems such as high gate leakage current caused by surface current trapping in AlGaN barrier layer [3, 4] which limits their performance at higher voltages and frequencies. The most effective way for suppressing the gate leakage current is by employing the use of a dielectric material for surface passivation. Different types of dielectric materials such as SiO_2 [5], Si_3N_4 [6], Al_2O_3 [7], and HfO_2 [8] have been reported for the fabrication of AlGaN/GaN-based MOS-HEMTs. The choice of the gate dielectric is important to achieve lower gate leakage current, i.e. dielectric materials with high dielectric constant (high-k) such as Al_2O_3 (dielectric constant 7-9.8 [9]) or HfO_2 (dielectric constant >24 [10]). In addition, the technique to form the dielectric material and uniformity of that, also plays an important role for producing better device performance. Techniques of deposition of gate dielectric are PECVD or ALD. PECVD provides higher growth rates while ALD grown dielectric have better film quality and uniformity for surface passivation [11]. In this work, we investigate three different dielectric materials. PECVD is used to grow SiO_2, and Si_3N_4 and ALD is used to grow Al_2O_3, as surface passivation and gate dielectric on AlGaN/GaN MOS-HEMT structures. A device with standard Schottky gate (HEMT structure) was also fabricated for comparison. We discuss the processing and device characteristics for all the fabricated devices in the next sections of the paper.

Device Structure and Fabrication

The epitaxial structure used in this work was grown by University of Cambridge, United Kingdom, using metal organic chemical vapour deposition (MOCVD) on a high-resistivity (HR) silicon substrate. The wafer structure consists of (from top to bottom), a 2-nm undoped GaN cap layer, 21-nm AlGaN barrier layer, 1-nm AlN exclusion layer, 200-nm GaN channel layer, 800-nm GaN buffer layer, 1.7-µm AlGaN buffer layer graded, 250-nm AlN nucleation layer. The cross-sectional schematic diagram of the epitaxial structure used can be found in [12]. A two level wrap-around gate design (where the gate encircles the drain) was used to simplify the device processing steps, eliminating the need for mesa isolation. In this experiment, 4 samples were prepared and labelled as follows: devices #S1 (Schottky gate-HEMT structure, used as a reference sample), #S2 (MOS-HEMT structure using SiO_2), #S3 (MOS-HEMT structure using Si_3N_4) and #S4 (MOS-HEMT using structure Al_2O_3). SiO_2, Si_3N_4 and Al_2O_3 insulators were used both as surface passivation and gate dielectric to the devices respectively.

Device fabrication started with the Ohmic metal contacts along with markers formed by the evaporation of Ti/Al/Ni/Au (30/180/40/100 nm), then followed by a lift-off process, and rapid thermal annealing at 800 °C for 30 secs in N_2 environment. This is followed by a blanket deposition of 10-nm of SiO_2 and Si_3N_4 for samples #S2 and #S3, and 20-nm of Al_2O_3 for sample #S4. Both SiO_2 and Si_3N_4 were grown using plasma-enhanced chemical vapour deposition (PECVD) at 300 °C, while Al_2O_3 was grown by atomic layer deposition (ALD). The Schottky gate metal contact metallization was formed by the evaporation of Ni/Au (20/400 nm), followed by a lift-off process. Finally, the dielectric layers (SiO_2, Si_3N_4,) are removed in Ohmic regions by reactive ion etching (RIE 80+) using CHF_3 and Ar gases with flow rates of 25 and 25 sccm, 50 W, 30 mTorr at 20 °C for 60 secs for measurement purposes. Al_2O_3 is removed from the ohmic regions of #S4 using inductively coupled plasma (ICP) 180 with BCl_3, ICP = 600 W, and RF = 25 W for 90 secs. DC measurements were carried out at room temperature using Keysight's B1500A Semiconductor Device Analyzer. Device dimension used in this work are as follows: gate length, L_G = 3 µm, gate-to-source distance, L_{GS} = 3 µm, gate-to-drain distance, L_{GD} = 5 µm.

Results and discussions

The measured output characteristics of the fabricated devices are shown in Figure 1. The maximum current densities, $I_{DS(max)}$, of over 1940 mA/mm, 1300 mA/mm, 1200 mA/mm and 1200 mA/mm were obtained at V_{GS} = 2 V, for the devices employing Al_2O_3 (#S4), SiO_2 (#S2), Schottky gate (#S1), and Si_3N_4 (#S3), respectively. The highest $I_{DS(max)}$ was measured for device #S4, due to the high quality of Al_2O_3 used for surface passivation and gate dielectric. We also observed the highest peak transconductance, g_m, of over 240 mS/mm measured at V_{DS} = 5 V for this device as shown in Figure 2. Device with SiO_2 (#S2) showed higher output currents (but with lower g_m value) compared to the Schottky gate structure. Poor DC characteristics was also observed for device with Si_3N_4 (#S3) compared to the Schottky gate structure. This is probably due to the quality of the dielectric layers grown using PECVD. The measured threshold voltage, V_{TH}, values were - 4.2 V, -7.3 V, -7.6 V, and - 8.4 V (each value was extracted at I_{DS} = 1 mA/mm) for devices #S1, #S2, #S3, and #S4 respectively. The V_{TH} values were shifted to a more negative value (compared to V_{TH} value of the Schottky gate structure) due to the usage of gate dielectric layer for devices #S2, #S3, and #S4.

Lowest measured gate leakage current characteristics of $I_{GS} = 1x10^{-8}$ A/mm at V_{GS} = -9 V was observed, for devices with SiO_2 (#S2) and Al_2O_3 (#S4) as shown in Figure 3. The measured breakdown voltages, V_{BR}, for Schottky gate (#S1) and device with Al_2O_3 (#S4) exceeds the maximum compliance of measurement

set up of 200 V as shown in Figure 4. Although lower I_{GS} was observed for the device with SiO_2 (#S2), the V_{BR} value (127 V) was lower than the Schottky gate structure. This observation is not fully understood and needs further investigation. Based on the measured DC characteristics for all devices, we can conclude that both the MOS-HEMT device using SiO_2 (#S2) and Si_3N_4 (#S3) demonstrates poor device performances compared to the Schottky gate structure. As mentioned earlier, this is probably due to the quality of the dielectric layers grown using PECVD.

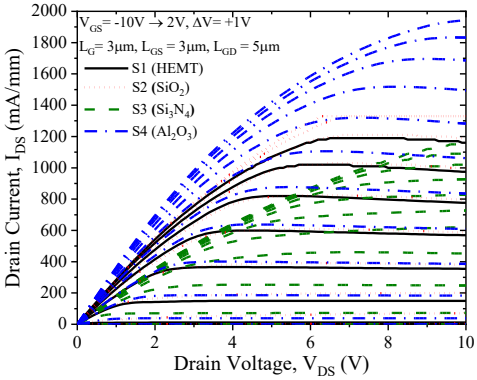

Figure 1. Measured output characteristics at voltage gate-to-source, V_{GS}, biased from -10 to 2 V with step size of 1 V for all fabricated devices.

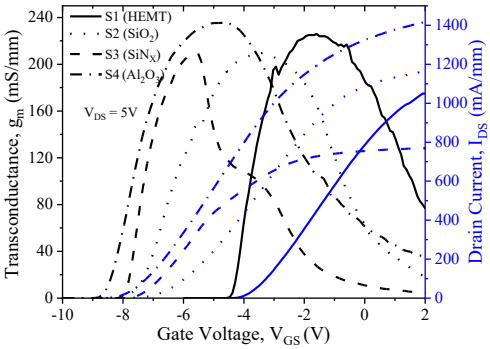

Figure 2. Measured transfer characteristics at a drain-to-source voltage, V_{DS} = 5 V, for all fabricated devices.

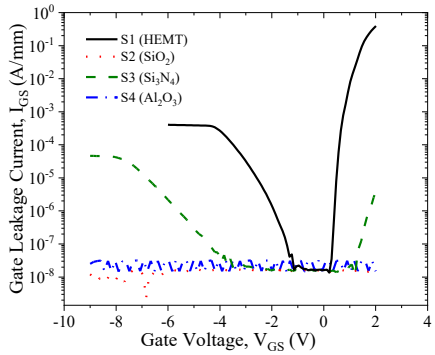

Figure 3. Measured gate leakage current characteristics at drain-to-source voltage, V_{DS} = 0 V for all fabricated devices.

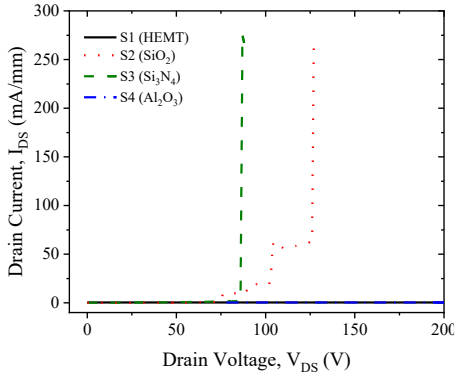

Figure 4. The off-state breakdown voltage characteristics at gate-to-source voltage, V_{GS} = 10 V for all fabricated devices.

Conclusions

We have successfully fabricated and measured devices #S1 (Schottky gate – HEMT structure), #2 (MOS-HEMT structure using SiO_2), #S3 (MIS-HEMT structure using Si_3N_4) and #S4 (MOS-HEMT structure using Al_2O_3). The AlGaN/GaN MOS-HEMT device employing high-k Al_2O_3 material for surface passivation and gate dielectric has been demonstrated the highest maximum drain current density of over 1940 mA/mm and highest maximum peak transconductance of 240 mS/mm. This device also produced the lowest gate leakage currents of $I_{GS} = 1x10^{-8}$ A/mm at V_{GS} = -9 V and the V_{BR} of over 200 V. These results indicate the high quality, high uniformity, and low defect of Al_2O_3 material grown using ALD. We also found that the devices employing PECVD SiO_2 and Si_3N_4 demonstrated poor device performances compared to the Schottky gate structure.

Acknowledgments

The authors wish to thank staff at the James Watt Nanofabrication Centre at the University of Glasgow for their support with this work. This work was supported in part by EPSRC grant no. EP/R024413/1.

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