

High-Performance n-Channel Printed Transistors on Biodegradable Substrate for Transient Electronics

Abhishek Singh Dahiya, Ayoub Zumeit, Adamos Christou, and Ravinder Dahiya*

Innovative methods to fabricate and integrate biodegradable high-grade electronics on green substrates are needed for the next generation of robust high-performance transient electronics. This is also needed to alleviate the growing problem of electronic waste (e-waste). Herein, the authors present the n-channel silicon (Si) nanoribbons-based high-performance transistors developed on biodegradable metal (magnesium) foils using the direct transfer printing method. The developed transistors present high effective mobility of $>600 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, high on/off current ratio ($I_{\text{on/off}}$) of $>10^4$, negligible hysteresis, transconductance of 0.19 mS, and an on-current of 1.6 mA at a bias of 2 V. Further, the transistors show stable device performance under temperature stress (5–50 °C), gate-bias stress, continuous long-term transfer scans for 24 h (>3000 cycles), and aging test (up to 100 days) demonstrating the excellent potential for futuristic high-performance robust transient devices and circuits. Finally, the effect of transience on the electrical functioning of devices on Mg foils (at pH 8) and degradation of Mg foils at different pH values is studied by hydrolysis. The outcome from these experiments demonstrates the potential of direct transfer printing for high-performance transient electronics and also as the new avenue toward zero e-waste.

1. Introduction

Transient electronics is on the rise as practical difficulties related to electronic waste (e-waste) requires greater attention.^[1] The unique characteristic of this emerging class of technology is that it completely disintegrates and/or dissolves into environment friendly by-products within a programmed period.^[2] With these features, transient electronics has huge potential to transform and expand the functional capabilities of vertical sectors including consumer electronics, medical, etc. with minimal adverse impact on environment through the generation of e-waste. Toward this, environmentally benign organic/bio-organic-based electronic materials have been explored to fabricate transient device/circuits including

A. S. Dahiya, A. Zumeit, A. Christou, R. Dahiya
Bendable Electronics and Sensing Technologies (BEST) Group
University of Glasgow
Glasgow G12 8QQ, UK
E-mail: ravinder.dahiya@glasgow.ac.uk

 The ORCID identification number(s) for the author(s) of this article can be found under <https://doi.org/10.1002/aelm.202200098>.

© 2022 The Authors. Advanced Electronic Materials published by Wiley-VCH GmbH. This is an open access article under the terms of the Creative Commons Attribution License, which permits use, distribution and reproduction in any medium, provided the original work is properly cited.

DOI: 10.1002/aelm.202200098

flexible complementary metal-oxide semiconductor (CMOS) circuits.^[1b] However, due to the poor charge carrier mobility, these electronic circuits do not match the performance of conventional integrated circuits (ICs) and as a result, their application is restricted to the low-end. High performance is much needed to drive advances in nearly all conventional and emerging application areas of electronics including connected systems, Industry 4.0, digital healthcare, digital agriculture, interactive systems, etc., where high-speed electronics is required to reduce the data latency.^[3] In this regard, nanostructures such as nanowires,^[4] nanoribbons (NRs),^[5] etc. and thin films of high-mobility inorganic materials offer a viable alternative. Their performance is on par with conventional silicon-based devices, and they can also be dissolved or disintegrated in controlled environments (Table 1).^[1e,1f,6]

Toward this, sputtered thin films of semiconducting inorganic oxides (zinc oxide and indium gallium zinc oxide)

on green (biodegradable) substrates have shown potential for physically transient forms of electronics for applications such as active-matrix light-emitting diode backplanes.^[1e,7] The obtained n-channel device mobility of $\approx 7 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ is sufficient for such applications but still not enough for high-speed applications. Further, the lack of viable p-type metal oxide materials resulted into implementation of a more complicated layout based on n-channel transistors and resistors for the logic functions.^[8] The drawback is the higher power consumption as compared with the complementary CMOS architecture. A significant impulse to transient electronics came from the use of silicon nanostructures including NRs and nanomembranes as an active transistor channel material enabling electron mobility of $>500 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and hole mobility of $\approx 100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.^[1d,1f,9] Accordingly, innovative attempts have been made to integrate high mobility silicon nanostructures over a variety of biodegradable substrates such as organic polymers, metal foils, etc. using transfer and contact printing methods.^[6,10] In these cases, transfer printing has received intense research interest due to facile pick-and-place approach. It allows the integration and assembly of nano to chip-scale structures from the donor to the target substrate.^[6] In a conventional transfer printing process, soft polymeric stamps are used for pick-and-place of micro/nanostructures. The use of viscoelastic stamps is cost-effective as it avoids the use of complex equipment but due to its viscoelastic nature, it is also challenging to attain a high transfer yield, particularly during the transfer of nanoscale structures.^[5c,11] To address

Table 1. State-of-the-art high mobility biodegradable materials for high-speed transient electronics. NMs – nanomembranes; NRs – nanoribbons; PLA – poly lactic acid; PLGA – poly lacticco- glycolic acid; PGA – poly glycolic acid; Mg – Magnesium.

Channel material	Channel dimensions [μm]	Performance [Mobility, $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$]	Electronic layer deposition method	Dielectric material	Substrate material	Ref.
Si NMs	p-type ($L = 5$; $W = 300$) n-type ($L = 15$; $W = 100$)	70 400	Transfer printing	SiO_2	PLGA, PLA, PGA	[1d]
Si NMs	n-type ($L = 20$; $W = 900$)	660	Transfer printing	MgO	Silk	[1f]
ZnO film	n-type ($L = 20$; $W = 500$)	0.95	Sputtering	MgO	Silk	[1e]
Si	n-type ($L = 1.8$; $W = 6$)	630	Transfer printing	SiN/SiO_2	PLGA substrate	[9]
Si NRs	n-type ($L = 5$; $W = 45$)	640	Direct transfer printing	SiN_x	Mg	This work

these challenges, single step “direct transfer printing” method has been explored for large-area electronics.^[5a] This promising printing technique avoids the use of viscoelastic stamps (this is why called “direct” transfer) and thus, reduces the number of fabrication steps with respect to the conventional transfer printing approach. In this method, structures over the donor substrate are brought into direct physical contact with the spun semi-cured thin polyimide (PI) film over the receiver substrate. Because of the semi-cured nature of the polyimide, a strong adhesion is developed between the structures on the donor substrate and the receiver which eventually leads to a high transfer yield. Furthermore, the approach leads to high registration with reduced printing time, and lower fabrication cost. These printing features can lead to resource-efficient electronics manufacturing.

In this work, we have used the direct roll printing to transfer silicon NRs arrays over biodegradable magnesium (Mg) metal foils as device substrates. Mg was chosen as the device substrate due to its inherent advantages including high thermal stability, chemical stability, hermeticity, biodegradability, and biocompatibility.^[12] In the past, metal foils such as Mo, Fe, W, etc. have been explored for fabrication of high-performance transient transistors using a conventional transfer printing technique.^[12b] We show here for the first-time the capability of the direct roll transfer printing approach to integrate arrays of Si NRs on Mg foils for high-performance transient transistors. Due to the poor elasticity of Mg foils, a flat stage printing set-up was used to hold the target Mg foil having semi-cured PI layer on top. PI is used as an adhesive layer due to its capacity to accommodate in vivo conditions and is certified as biocompatible.^[13] Next, the donor silicon-on-insulator (SOI) wafer was brought in contact with the semi-cured PI to transfer the Si NRs. Following the transfer printing of NRs, a room temperature (RT) fabrication process including dielectric (SiN_x) deposition was performed to realize high-performance n-channel transistors. The developed transient transistors exhibit excellent electrical properties including high effective mobility of $>600 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$, high on/off current ratio ($I_{\text{on}}/I_{\text{off}}$) of $>10^4$, and low gate leakage (0.2 nA). Along with the biodegradability, transient devices are expected to have a stable device operation over a predefined time frame. This could be difficult to achieve due to the intrinsic water-soluble nature of the biodegradable materials used during the fabrication. In this regard, we have performed in-depth study of the device stability which includes ageing effect, temperature-dependent stability, and electrical gate-bias stress study. Our stability study confirms robust device performance under applied temperature

and gate-bias stress and for more than three months of the collected data. This confirms the high quality of the developed fabrication process. Further, the effects of transience on the electrical functioning of devices on Mg foils in aqueous solution of pH-8 at 37 °C are systematically studied by hydrolysis. Finally, we have performed the biodegradable studies of the transistor devices in aqueous solution at different pH scales and constant temperature of 37 °C to extract the etching rate of the Mg foil.

2. Results and Discussions

Figure 1 schematically shows the process steps for fabrication of high-performance n-channel transient transistors on Mg foils. To begin with, arrays of Si NRs are fabricated on rigid SOI wafer using conventional microfabrication process (Figure 1a). Details for this step which includes selective doping of NRs to define source/drain (S/D), under etching of the buried oxide (Box), etc. could be obtained from our previous work.^[5a,5c] The fabricated arrays of laterally aligned and suspended NRs over SOI source wafers are subsequently transferred onto receiver Mg foils coated with the semi-cured PI using the direct transfer method (Figure 1b). Before the transfer method, $\approx 1 \mu\text{m}$ thick SiO_2 was also deposited to passivate the rough Mg surface (rms $\approx 800 \text{ nm}$) using the plasma-enhanced chemical vapor deposition (PECVD) method. The transfer printing process details are described elsewhere.^[5a] A high transfer yield of 95% with registration factor of $<100 \text{ nm}$ was achieved on Mg foils, similar to our previously reported results.^[5a,5b] Such a high transfer yield was achieved by applying a high contact force of 12 N during the transfer process. A high contact force ensures conformal contact between the semi-cured PI layer and suspended Si NRs on SOI wafer. The conformal contact helps to transfer the applied force uniformly and to break the anchor points of NR arrays which leads to a high-transfer yield. Following the transfer of NRs, low-temperature conventional microfabrication steps (e.g., dielectric, metal deposition, and lift-off) were carried out to finalize n-channel transient transistors on Mg foils (Figure 1c). Figure 1d shows an exploded view of schematic illustration of the various biodegradable and nonbiodegradable layers of the final n-channel transient transistors.

The fabricated n-channel transient transistors with length $\approx 5 \mu\text{m}$ and width $\approx 45 \mu\text{m}$ on Mg foils were characterized in ambient dark conditions. The electrical characterization results and schematic/optical image of fabricated n-channel devices

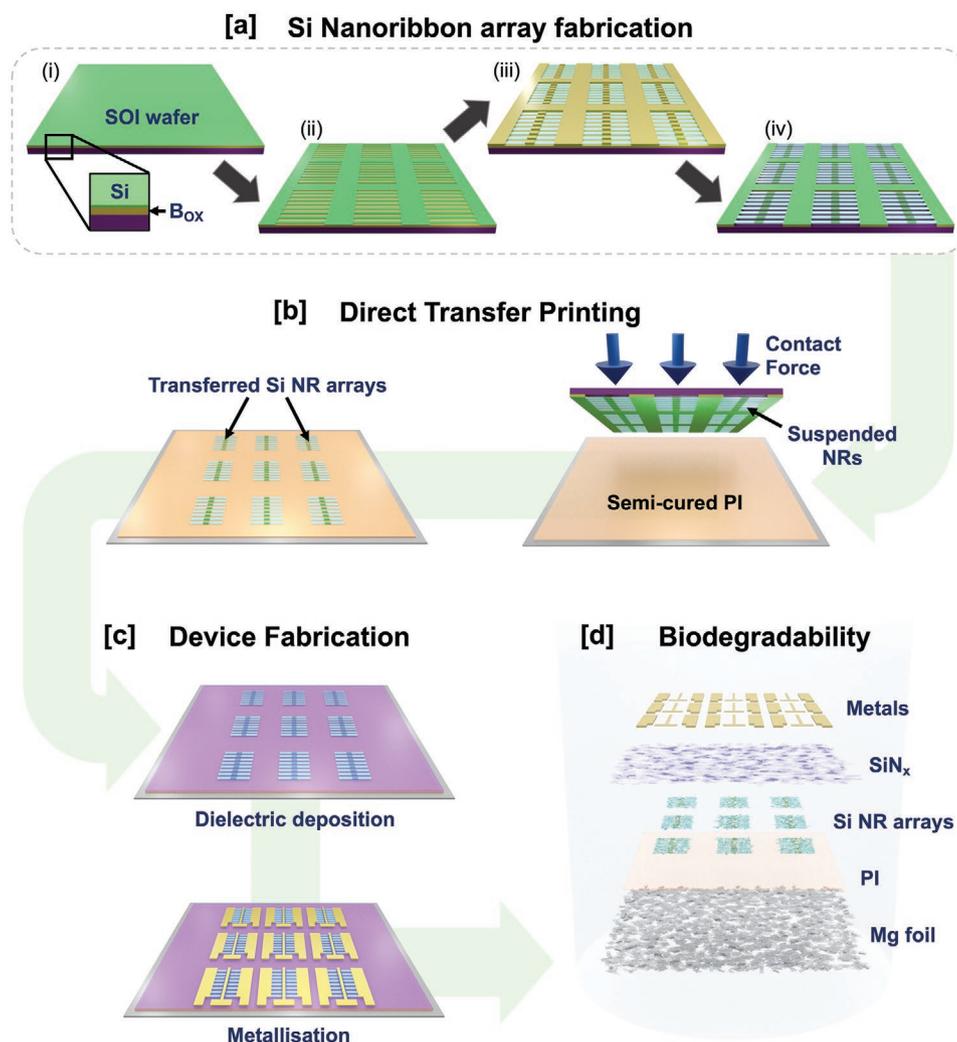


Figure 1. Schematic illustration of the fabrication steps involved in direct transfer printed n-channel Si NRs based transient transistors. a) Fabrication steps to achieve suspended Si NRs with the selective n-type doped region: (i) SOI wafer with a 70 nm thick moderately doped silicon layer on a buried oxide (2 μm), (ii) photolithography and etching steps to define the dimensions of Si NRs (width of 5 μm and length 55 μm), (iii) the Si NRs are selectively doped using spin-on dopant (SOD) through the diffusion of phosphorus (SiO_2 is used as a diffusion barrier mask layer), and (iv) releasable suspended Si NRs arrays with delicate anchor points at both ends after etching of the buried oxide layer by wet etching. b) Direct transfer printing of n-channel Si NRs arrays on biodegradable Mg metal foils. c) Conventional microfabrication steps including room temperature gate dielectric (SiN_x) deposition by ICP-CVD, metallization step to define the source (S), drain (D) and gate (G) metal contacts and lift-off, and d) exploded view illustration of the various biodegradable and non-biodegradable layers, i.e., Mg for substrate, silicon nitride (SiN_x) as gate dielectric, Si NRs for semiconducting elements, and Ti/Au for S/D/G electrode.

are shown in **Figure 2**. The transfer characteristics ($I_{\text{DS}}-V_{\text{GS}}$), with drain bias (V_{DS}) of 10 mV, were obtained by varying gate-source voltage (V_{GS}) from -5 to 10 V and shown in both linear and logarithmic scales. The high-grade electronic properties of the printed NRs such as mobility allowed the device to operate at ultra-low V_{DS} of 10 mV. The critical field-effect transistor (FET) performance parameters to consider were extracted using the transfer scan: on-state (I_{on}), off-state current (I_{off}), current on/off ratio ($I_{\text{on}}/I_{\text{off}}$), effective mobility (μ_{eff}), and subthreshold slope (S-S).^[14] The measured devices showed a typical $I_{\text{on}} (\approx 10 \mu\text{A})/I_{\text{off}} (< 1 \text{ nA})$ current ratio of $>10^4$ suggesting an excellent gate-channel control. The extracted S-S from the logarithm transfer plot is 0.9 ± 0.2 V per decade. Next, threshold voltage (V_{T}) was extracted using the linear extrapolation method. For

this, the linear extrapolation of $I_{\text{DS}}-V_{\text{GS}}$ graph, intercepting the $I_{\text{d}} = 0$ at the x-axis (V_{GS}) gives the V_{T} value (1.4 V). This was followed by the calculation of transconductance (g_{m}), according to Equation (1) shown below:

$$g_{\text{m}} = \left. \frac{\partial I_{\text{DS}}}{\partial V_{\text{GS}}} \right|_{V_{\text{DS}} = \text{constant}} \quad (1)$$

Next, the field-effect (effective) mobility was extracted using the conventional metal-oxide-semiconductor field-effect transistor (MOSFET) model in the linear regime.^[5a,5b,15] The extracted effective mobility was found to be $\approx 640 \pm 10 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ which compares well with most of the state-of-the-art n-channel Si NR-based FETs on biodegradable substrates. Further, the performance of

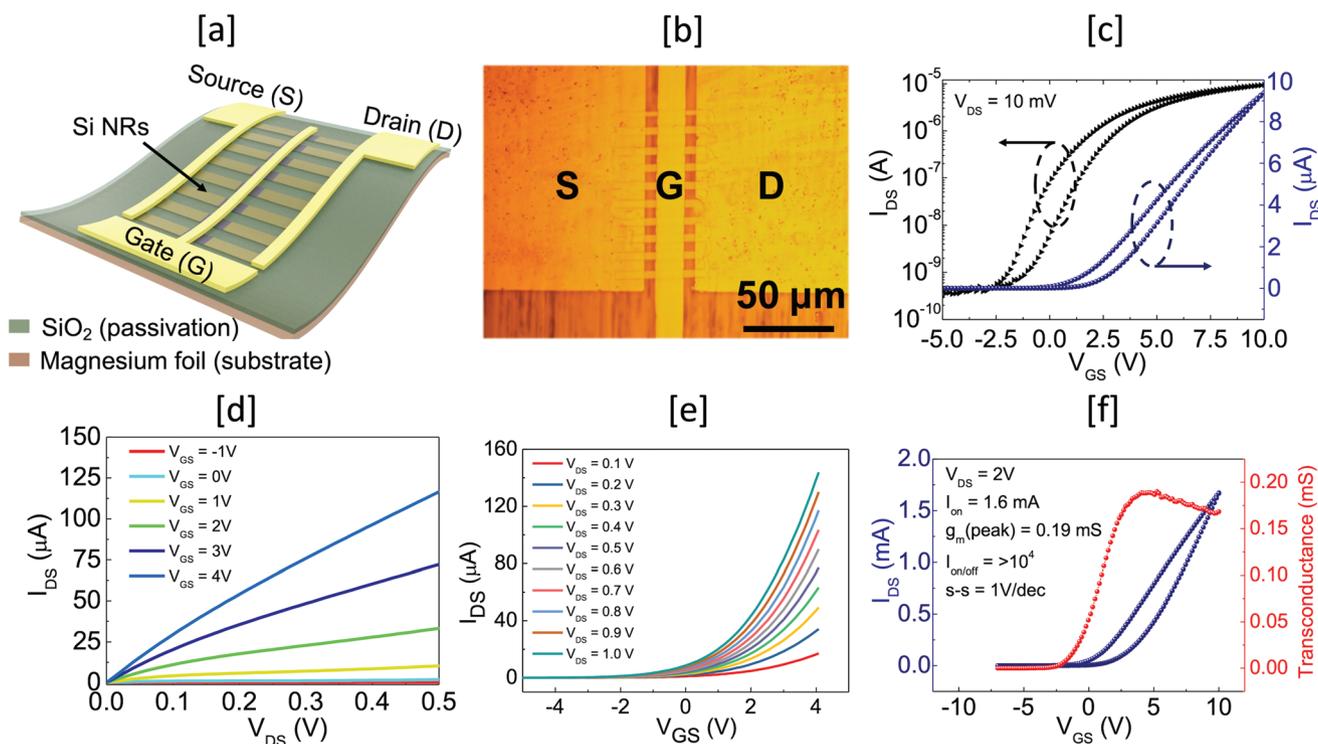


Figure 2. N-channel transient transistor and its electrical characteristics: a) schematic and b) optical image, c) transfer characteristics at $V_{DS} = 10$ mV in logarithmic and linear scales, d) output characteristics, e) transfer characteristics with varying V_{DS} from 0.1 V to 1 V, and f) transfer characteristics at $V_{DS} = 2$ V (transconductance is shown as secondary y -axis).

the direct transfer n-channel transient transistor is compared with the similar n-channel devices on flexible PI substrates (Table S1, Supporting Information). Interestingly, the performance of the transient transistor devices is like the one fabricated on PI substrates. This confirms the efficacy and substrate-independency of the developed RT printing and overall fabrication process.

To evaluate the potential of the fabricated transient transistor in the high-speed (computation and/or communication) applications such as IoT, the theoretical cut-off frequency f_T is extracted using the following equation^[16]:

$$f_T = \frac{\mu_{\text{eff}} V_{DS}}{2\pi L (L + L_{\text{ov,GS}} + L_{\text{ov,GD}})} \quad (2)$$

where $L_{\text{ov,GS}}$ is the parasitic gate-to-source overlap, and $L_{\text{ov,GD}}$ is the parasitic gate-to-drain overlap. Neglecting the parasitic capacitances, the f_T of n-channel transient transistor with a channel length of 5 μm and mobility of $640 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ is estimated to be more than 800 MHz which can be further enhanced by reducing the channel length and contact resistance in future optimized design. Nevertheless, it is already a few orders higher than the state-of-the-art transistor devices based on organics and metal oxides.^[8a,16,17] Such a high device performance can provide excellent opportunities for biodegradable implantable electronics that do not require removal. The transient ICs fabricated using the demonstrated transistors, could also perform complex logic functions enabling self-monitoring implantable systems.^[18] For the continuous recording of the

sensed signals, implantable wireless communication devices need to operate inside the body. Recently, the feasibility of Bluetooth Low Energy (BLE) technology for ingestible and implantable medical device applications has been demonstrated by studying radio frequency (RF) signal attenuation in different tissue types.^[19] It was experimentally shown that the device orientation as it moves through the body has a negligible impact on the RF signal attenuation. In the future, such high-performance transient ICs can be integrated with BLE devices applications for biomedical implants.

Next, the output characteristics (V_{DS} - I_{DS}) were obtained by varying V_{GS} from -1 to 4 V with the step of 1V. Notably, the low V_{DS} region shows a linear dependence of I_{DS} with increasing V_{DS} without any inflection point. This device characteristic (low-resistive metal-semiconductor (M-S) contacts) is needed for achieving high device performance. Figure 2e shows the transfer characteristics of n-channel transient transistors at various values of V_{DS} . It is worth noting from Figure 2e that the V_T remains constant with varying V_{DS} , indicating high stability charge transport behavior under different drain voltages. Finally, the device transfer characteristics were measured at a high V_{DS} of 2V (Figure 2f). At this bias voltage, the developed biodegradable n-channel transistors presented a high on/off current ratio ($I_{\text{on}}/I_{\text{off}}$) of $>10^4$, transconductance of 0.19 mS, and an on-current of 1.6 mA.

Stable and reliable transistor operation is critical for any practical application to allow the correct execution of programmed duties of ICs over its lifetime. This becomes even more crucial for transient devices which could easily collapse from different

available ambient sources including hydrolysis triggered by light,^[20] heat,^[21] moisture,^[7] electrochemical,^[22] or physicochemical.^[2] For this, we have assessed the stability of our transistor devices under different stress conditions including electric (gate bias and continuous cycles), temperature, and evaluated the degradation of devices performance related to aging for more than 3 months. **Figure 3** shows the results of the continuous electric bias stress where the transfer scans were performed continuously for up to >3000 cycles (≈ 24 h). The I_{DS} was monitored by sweeping the V_{GS} from -6 to $+6$ V (forward voltage sweep) and from $+6$ to -6 V (reverse voltage sweep) at a constant $V_{DS} = 10$ mV. A full transfer scan (from forward to reverse voltage sweep) is treated as one stress cycle. The transfer scans were used to extract the key transistor performance parameters namely, I_{on} , I_{off} , $I_{on/off}$ ratio, S-S, and hysteresis (from the V_T value of forward and reverse scan). Both I_{on} (Figure 3b) and I_{off} (Figure 3c) decrease with the increase in stress time. The extracted data reveals that there is a small decrease in the device I_{on} ($\approx 22\%$) and I_{off} ($\approx 26\%$) after more than 3000 operational cycles, confirming robust device operation. Because of the almost similar change in the I_{on} and I_{off} , no change is observed in the I_{on}/I_{off} ratio ($>10^4$) for all stress cycles (Figure 3d). Next, hysteresis (Figure 3g) is calculated based on the difference in V_T value for forward (Figure 3e) and reverse (Figure 3f) transfer scans. For both forward and reverse scans, a small positive V_T shift (≈ 1 V) with the stress time is observed. This value compares less with the reported transistors-based metal oxides.^[14,23] Also, the maximum hysteresis noticed for all stress cycles is ≈ 0.25 V for the transient transistors. Using the hysteresis data, the transient transistors showed a maximum interface trap charge density of $\approx 1 \times 10^{11} \text{ cm}^{-2}$ ($\Delta V_T = 0.25$ V, and $C_{ox} = 7 \times 10^{-4} \text{ F m}^{-2}$). The extracted value of interface trap charge density is an order of magnitude less than the SiO_2 -semiconductor interface for nanomaterial-based transistors.^[24] Finally, S-S values were extracted and plotted in Figure 3h. The data shows $\approx 12\%$ change in S-S value after 24 h of continuous operation.

Next, the gate bias stress studies were performed to understand the interface quality of the transistor. This is critical because poor interface quality could lead to V_T shift and thus, changes in an on-current of the device.^[14] The test results are shown in **Figure 4**. To evaluate the effect of both positive gate bias stress (PGBS) and negative gate bias stress (NGBS), transfer scans were performed immediately after PGBS and NGBS (Figure 4a). First, transfer scan was performed under no stress conditions by sweeping the V_{GS} from -5 to $+5$ V at a fixed 10 mV drain-source bias. Then, a PGBS was applied for 30 min (1800 s) (Figure 4b) and sequentially the transfer characteristic was measured. A shift in the threshold voltage toward negative gate voltages and an increase in on-current is clearly visible from the measured transfer scan after PGBS. This could be explained as follows: During the continuous applied gate field in transistors, trapping or de-trapping of the free electrons (or in general charge carrier) could occur from the interface and/or bulk defects (depending on the direction of the gate field).^[14] More electrons could be added in the channel through the de-trapping of free electrons, and thus an increase in the I_{DS} may be detected. The enhancement of the device on-current with PGBS could be explained due to de-trapping of the trapped electrons. The free electrons could be trapped either at shallow

energy level or deep energy level trap states at the channel/dielectric interface or bulk of dielectric.^[25] The charge-trapping has been explained by two models:^[14,23] i) the first one is specific to amorphous silicon (a-Si) and arises because of the motion of bonded hydrogen in the a-Si channel during prolonged gate bias stress and creates extra defect sites in the channel, and ii) the other is common to all materials and is the transfer of mobile charges to immobile trapping states at the semiconductor-insulator interface or at the semiconductor-ambient interface.^[14,26] Monitoring the S-S values could help to identify the dominant mechanism. Generally, S-S remains constant when the electrons are trapped at the shallow energy level trap centers and the device V_T comes back to its initial value after applying gate bias stress in the opposite direction.^[25] The S-S of the device remains constant, which hints that the electrons were trapped at shallow energy levels. To confirm this, NGBS was applied for 1800 s (Figure S1, Supporting Information) and the transfer characteristic under similar conditions was measured. Interestingly, the V_T of the device comes back to its initial value which confirms the charge trapping at the shallow traps.

The temperature-dependent performance variations of transient transistors are analyzed and shown in **Figure 5**. The transfer scans in the forward direction (-5 to $+5$ V_{GS}) were performed at different temperatures (5 – 50 $^\circ\text{C}$ with a step of 5 $^\circ\text{C}$), as shown in Figure 5a. The transconductance (Figure 5b) and I_{on} (Figure 5c) of the device were extracted from the transfer scans shown in Figure 5a. The extracted data shows a decrease in both I_{on} and transconductance values above 30 $^\circ\text{C}$ and below 15 $^\circ\text{C}$. The decrease at higher temperatures (>30 $^\circ\text{C}$) is understandable because of the increased scattering events (acoustic phonon assisted and Coulombic) in the channel and/or at the semiconductor/dielectric interface. Thus, at higher temperatures, the device performance is limited by scattering events.^[27] The hypothesis is further confirmed by analyzing the extracted S-S and V_T values at different temperatures. The variations in S-S and V_T with temperature are shown in Figure 5d. This figure reveals that the absolute S-S value increases above 35 $^\circ\text{C}$ (≈ 0.9 V dec^{-1}) and reached to ≈ 1.4 V dec^{-1} at 50 $^\circ\text{C}$. The S-S of transistors is largely affected by the interface (channel/dielectric) trap charge density. Also, these interface charges lead to shift in threshold voltage of transistors. To correlate the change in S-S trend to interface traps, we have calculated the magnitude shift of V_T with temperature. The V_T data shows a similar trend like S-S change with temperature. Accordingly, both S-S and V_T change can be correlated to the transfer of mobile charge carriers to immobile trapping states at the semiconductor/insulator interface. The decrease in device performance (I_{on} and g_m) at lower temperature (<15 $^\circ\text{C}$) could be because the measurements were performed in the ambient conditions. At lower temperature, condensed water molecules can contribute to charge transport degradation.^[28] Before performing biodegradation studies, the last test related to transistor reliability was performed. The transistor performance degradation related to aging for more than three months was studied (Figure S2, Supporting Information). The data shows a negligible change in the I_{on} of the transient transistor after 100 days.

Previous studies have explored the transience behavior of the biodegradable devices. It is shown that the hydrolysis kinetics of the constituent device materials depends on many factors

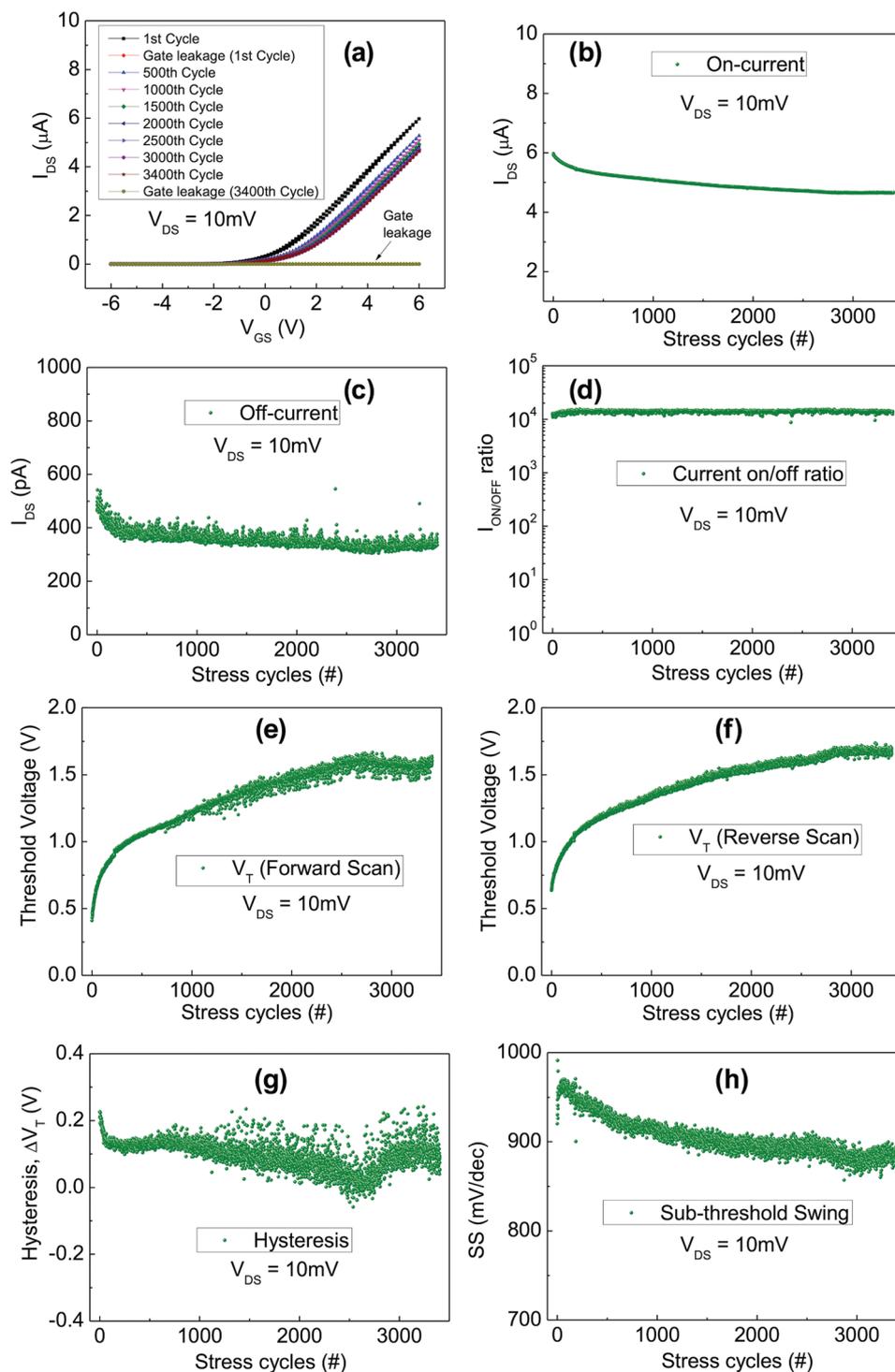


Figure 3. Electrical bias stress performance evaluation of n-channel NR-based transient transistors on Mg substrate. a) continuous transfer scan measurements (≈ 3400 cycles) with $V_{DS} = 10\text{ mV}$ up to 24 h of operation. (b-g) extracted key transistor parameters from the continuous transfer scan to observe the device performance stability: b) on-current, c) off-current, d) current on/off ratio, e) threshold voltage (forward scan), f) threshold voltage (reverse scan), g) hysteresis, and h) sub-threshold swing.

including pH, temperatures, and the thickness, grain structure, and surface morphology.^[12b,29] Here, we have studied the biodegradation behavior of the developed transient transistors in different aqueous solutions with varying pH values but kept at

constant temperature ($37\text{ }^\circ\text{C}$) (Figure 6). It is to note that $37\text{ }^\circ\text{C}$ is chosen as it represents the body fluid temperature. First, the effect of transience on the electrical performance of transistors is studied by hydrolysis at pH 8 (close to body fluids). For these

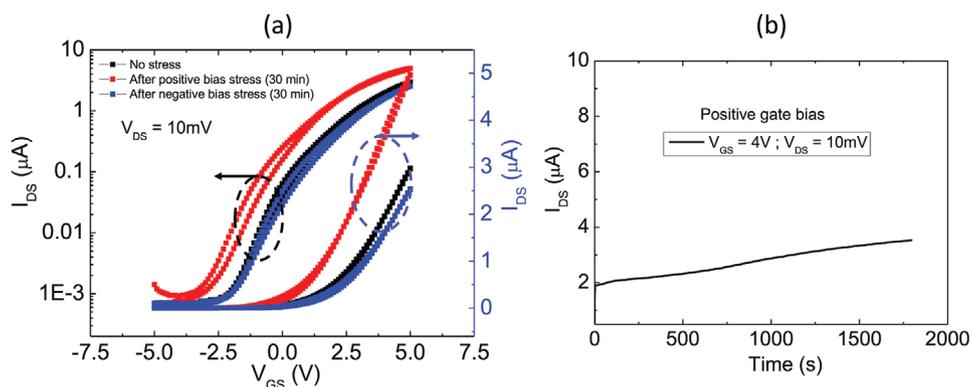


Figure 4. Gate bias stress study at $V_{DS} = 10$ mV: a) transfer scans performed under different conditions (no-stress, after positive gate bias stress, and after negative gate bias conditions). b) I_{DS} -time curve during the applied positive gate bias condition.

experiments, the transistor sample was placed inside the aqueous solution and the electrical measurements were performed at regular intervals after removing it from the solution. Figure 6a illustrates the transfer scans of transient transistor at $V_{DS} = 10$ mV performed after different times. Further, the drain current is extracted at $V_{GS} = 6$ V using the transfer scans and plotted in graph shown in Figure 6b. The data indicate stable operation for ≈ 6 h, followed by slow loss of function. To better understand the decrease in transistor on-current, we have collected optical micrographs of the device before performing the electrical measurements (Figure S3, Supporting Information). The figure shows that the disintegration process starts ≈ 10 h after the sample was placed

inside the solution. The partial disintegration of one of the metal electrodes could be the reason for the observed slow transience (due to an increase in the contact resistance). After 55 h (3300 min) in the solution, the transistor stopped functioning as the gate metal electrode was completely disintegrated from the channel.

The disintegration process and rate of Mg etching is further studied for different pH values 2, 4, 6, 8, and 11. Figure 6c presents series of images taken during the transience process by hydrolysis of transistor devices on a Mg foil (≈ 20 μm). It was observed that first, the transistor layers start to disintegrate (Ti/Au electrodes were observed to float in the solution). This is schematically shown in Figure 6d. The disintegration

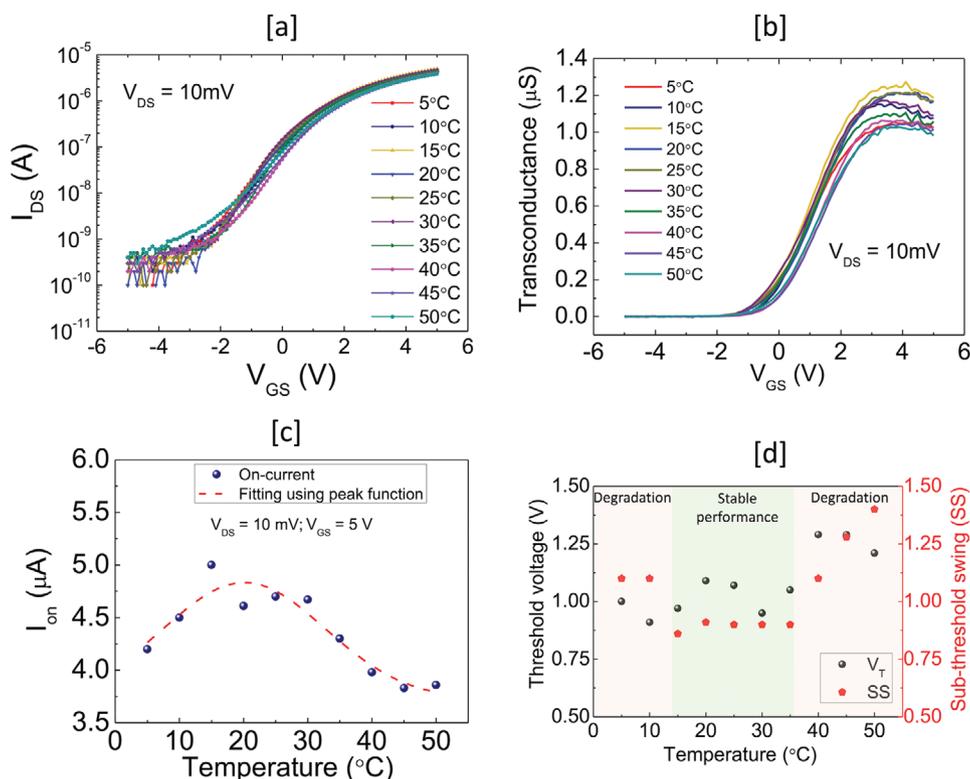


Figure 5. Temperature-dependent (5–50 °C) electrical characterizations to investigate the stability of n-channel transient transistors. a) Transfer scans. Important transistors parameters data were extracted using temperature-dependent transfer scans: b) transconductance, c) on-current, and d) S-S and V_T .

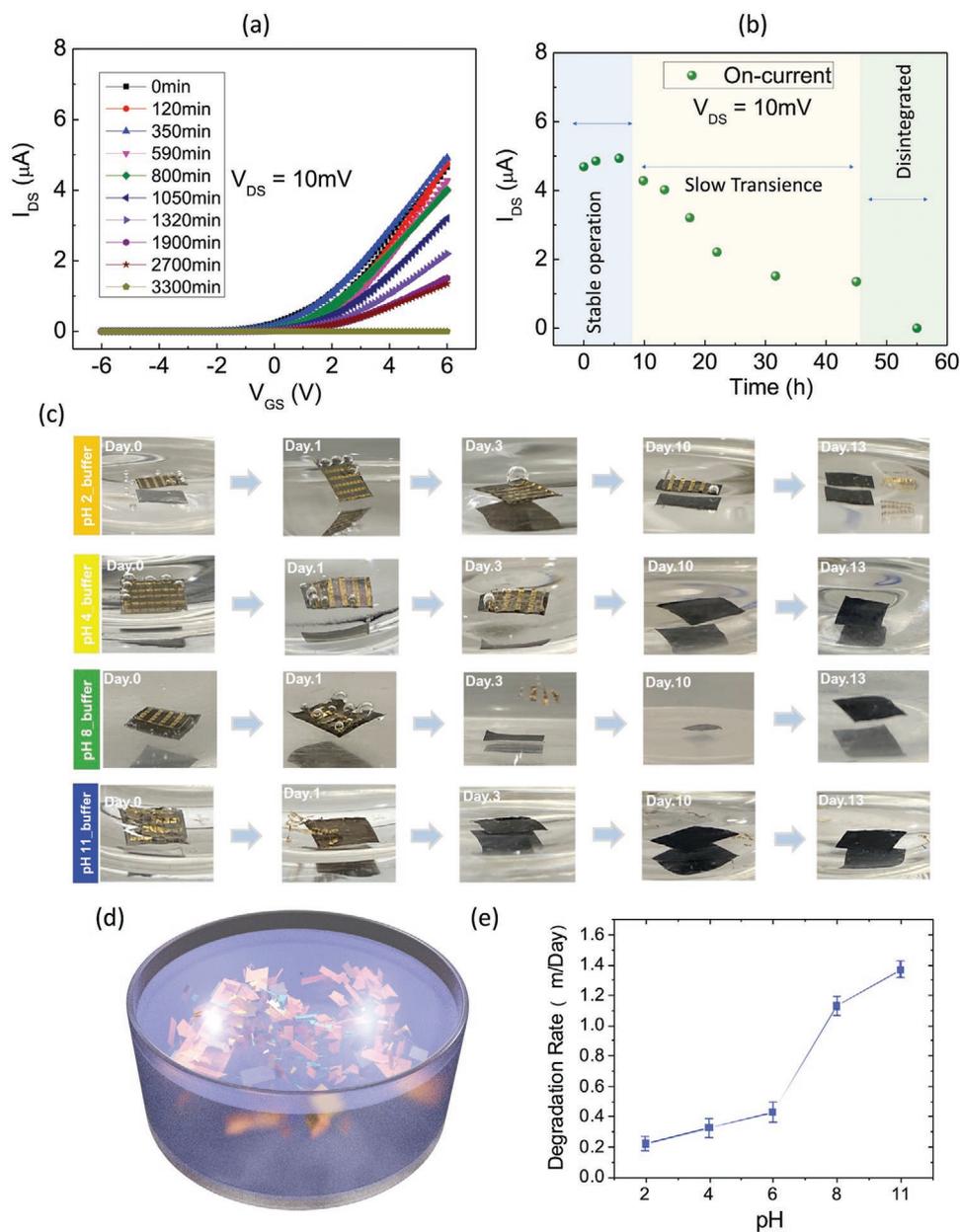


Figure 6. Biodegradation studies of the n-channel transistors on biodegradable Mg foils: a) Measured transfer scans at $V_{DS} = 10\text{ mV}$ after placing the sample for different times in the aqueous solution of pH 8 and kept at $37\text{ }^\circ\text{C}$. Different colored curves indicate responses at different times. b) The drain current extracted at $V_{GS} = 6\text{ V}$ as a function of time shows various stages of the transient transistor operation namely, stable, slow transience, and loss of functioning. c) Sequential images were collected at various stages of dissolution for devices immersed in different pH (pH-2, pH-4, pH-8, and pH-11) at $37\text{ }^\circ\text{C}$. d) Schematic representation of the biodegradation, and e) is the rate of biodegradation of Mg foil.

starts because of the etching of biodegradable interface layers between the different layers (SiO_2/Mg and $\text{SiO}_2/\text{metal}$). It was further noticed that the rate of etching was directly proportional to the pH values. This means that the disintegration step occurred earlier for transistors kept in more basic solution than the ones kept in more acidic. Day 0 images represent first day of transistor devices placed inside the solution. A distinct disintegration process was noted from the device kept in $\text{pH} \approx 11$ on day 0. Once disintegrated, further etching of the individual layers continued to occur. The rate of degradation for silicon oxides and nitrides is well known for films deposited using

different techniques^[1a,18a,29] and is therefore, not monitored. After 13 days, the Mg foil (rest other layers disintegrated) was lifted out of the solution and thickness was monitored using an optical profilometer and SEM to extract the rate of dissolution. The cross-sectional SEM images of the Mg foils kept at different pH values is shown in Figure S4, Supporting Information. The average changes in Mg foil thickness rate in solution (at $37\text{ }^\circ\text{C}$) are 0.23, 0.27, 0.36, 1.08, and 1.31 $\mu\text{m day}^{-1}$ for devices in pH 2, 4, 6, 8, and 11, respectively (Figure 6e). This clearly shows the etching rate of the Mg foil is more in solution of higher basicity. With this rate, the complete dissolution of the

Mg foil would occur after ≈ 87 , ≈ 74 , ≈ 55.5 , ≈ 18.5 , and ≈ 15 days for transistor in pH 2, 4, 6, 8, and 11, respectively.

It is important to note that the presented transient transistors also comprise of some non-biodegradable layers, i.e., metal contacts (Ti/Au), and a semi-cured PI. Although the metals are non-biodegradable, but hydrometallurgical treatments could be used to extract most of the disintegrated metals including gold.^[30] For instance, it has been shown that by using environmentally friendly lixiviants such as thiosulfate during the hydrometallurgical treatment, almost 95% of the Au could be recovered.^[30a] The recovered Au can be recycled to enhance the circularity in electronics. Thus, the circular electronics connects the recycling and degradable approaches.^[31] Accordingly, in the near to midterm, the transient electronics could be explored to complement the current recycle and reuse approach.^[1g] Nevertheless, by exploring biodegradable metals such as Mg, Fe etc., and biodegradable adhesive layer such as MICA MC-634 and spin-on glass, direct transfer printing has the potential for the fabrication of high-performance transient ICs and thus, eventually replace the present recycle and reuse approach.

3. Conclusions

In summary, we have developed high-performance n-channel transient transistors on biodegradable metal magnesium foils. To transfer the high-quality and biodegradable electronic layers (Si nanoribbons) on Mg foils, direct transfer/stamp printing was employed. The transistor devices showed high performance including high effective mobility ($>600 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$), high on/off current ratio ($I_{\text{on}}/I_{\text{off}}$) of $>10^4$, negligible hysteresis, and an on-current of 1.6 mA at a bias of 2 V. The transient device performance was compared with similar devices on flexible PI substrates. The comparable transistor performance on different substrate confirmed the robustness and substrate independency of the developed fabrication process. The transient transistors were able to operate at very low V_{DS} of 10 mV, thanks to the high electron mobility of Si NRs and high ohmicity of the metal–semiconductor contact. A stable and reliable transistor operation was confirmed in ambient conditions using a series of systematic tests: continuous transfer scans, gate bias, and temperature stress, and ageing studies for >3 months. The developed transistors constituents/layers are mostly, but not all, biodegradable. This is demonstrated by transience studies performed in aqueous solutions at different pH values at 37 °C. The loss of transistor function was observed after 55 h for devices placed inside the solution of pH 8. The study also showed that the device at higher pH (higher basicity) disintegrated and degraded at a faster rate. A technology of this type could open new avenues for commercial electronics with reduced e-wastage, sustainable environment/soil monitoring, and implantable biomedical devices.

4. Experimental Section

Fabrication and Doping of High-Grade Si Nanoribbons: As an active channel of the transient transistor devices, Si NRs were fabricated using our previously reported process steps.^[5c] Briefly, arrays of Si NRs (9 NRs) with a length of 55 μm and individual NR width of $\approx 5 \mu\text{m}$ were patterned using standard photolithography and reactive ion etching

(RIE) (CHF_3/O_2 , 50 sccm, 55 mTorr, 5 min). The active channel length of the transistor/NRs was defined by selective doping of the NRs (thermal diffusion). The doping process also assisted in obtaining low-resistive ohmic contacts. This is critical for high device performance and low-power operation. A 250 nm thick SiO_2 diffusion barrier layer was deposited using the PECVD and patterned using conventional photolithography steps. The etching was performed using RIE through optimized recipe: CH_3/Ar plasma (40 sccm CH_3/Ar flow with a chamber base pressure of 30 mTorr, 200 W RF power). Next, spin-on dopant with patterned SOI wafer was placed inside the horizontal tube furnace and annealed at 1050 °C in Ar ambient for 30 min.

Direct Transfer/Stamp Printing of Si NR on to Mg Foils: The custom-made contact printing setup^[4a] was used for a repeatable and high yield transfer of suspended and selectively doped n-channel Si NR arrays SOI wafer. The printing process is like our previously demonstrated direct roll transfer printing process^[5a] but using a flat stage. It is a single-step printing process. To carry out the transfer printing process, first, an adhesion promoter of $\approx 1.0 \mu\text{m}$ (PI-2545 precursor from HDmicrosystems) was spin coated on to the SiO_2 passivated commercial magnesium metal foils. Next, Si NRs are brought into direct physical contact with the semi-cured PI receiver substrate. The applied force during roll transfer stamping is 12 N. After NR transfer, the target device substrate (Mg foils) is subsequently cured at 250 °C for 2 h.

Si NRFET Fabrication and Characterization: After transfer printing of Si NR arrays, n-channel transistors were fabricated using RT processes. This included deposition of high-quality gate dielectric (SiN_x , 100nm) using the Inductively Coupled Plasma Chemical Vapour Deposition (ICP-CVD) followed by metal deposition (Ti (10 nm)/Au (120 nm)) for gate, source, and drain using e-beam evaporation and lift-off. Electrical characterizations were performed using Cascade Microtech Auto-guard probe station interfaced to a semiconductor parameter analyzer. Linkam PE120 Peltier system was used for heating and cooling the NRFETs to perform temperature dependence electrical measurements.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

A.S.D. and A.Z. contributed equally to this work. This work was supported by Engineering and Physical Sciences Research Council through Engineering Fellowship for Growth (EP/R029644/1) and Hetero-print Programme Grant (EP/R03480X/1).

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

biodegradable electronics, high-performance transistors, printed electronics, silicon nanoribbons, transfer printing, transient electronics

Received: January 25, 2022

Revised: March 25, 2022

Published online: April 29, 2022

- [1] a) A. A. La Mattina, S. Mariani, G. Barillaro, *Adv. Sci.* **2020**, *7*, 1902872; b) T. Lei, M. Guan, J. Liu, H.-C. Lin, R. Pfattner, L. Shaw, A. F. McGuire, T.-C. Huang, L. Shao, K.-T. Cheng, J. B.-H. Tok, Z. Bao, *Proc. Natl. Acad. Sci. USA* **2017**, *114*, 5107; c) S. Needhidasan, M. Samuel, R. Chidambaram, *J. Environ. Health Sci. Eng.* **2014**, *12*, 36; d) S.-W. Hwang, J.-K. Song, X. Huang, H. Cheng, S.-K. Kang, B. H. Kim, J.-H. Kim, S. Yu, Y. Huang, J. A. Rogers, *Adv. Mater.* **2014**, *26*, 3905; e) C. Dagdeviren, S.-W. Hwang, Y. Su, S. Kim, H. Cheng, O. Gur, R. Haney, F. G. Omenetto, Y. Huang, J. A. Rogers, *Small* **2013**, *9*, 3398; f) S.-W. Hwang, H. Tao, D.-H. Kim, H. Cheng, J.-K. Song, E. Rill, M. A. Brenckle, B. Panilaitis, S. M. Won, Y.-S. Kim, Y. M. Song, K. J. Yu, A. Armeen, R. Li, Y. Su, M. Yang, D. L. Kaplan, M. R. Zakin, M. J. Slepian, Y. Huang, F. G. Omenetto, J. A. Rogers, *Science* **2012**, *337*, 1640; g) M. Chakraborty, J. Kettle, R. Dahiya, *IEEE J. Flexible Electron.* **2022**, *1*, 4. h) N. Yogeswaran, E. S. Hosseini, R. Dahiya, *ACS Appl. Mater. Interfaces* **2020**, *12*, 54035.
- [2] J.-W. Shin, J. C. Choe, J. H. Lee, W. B. Han, T.-M. Jang, G.-J. Ko, S. M. Yang, Y.-G. Kim, J. Joo, B. H. Lim, E. Park, S.-W. Hwang, *ACS Nano* **2021**, *15*, 19310.
- [3] a) S. Gupta, W. T. Navaraj, L. Lorenzelli, R. Dahiya, *npj Flex. Electron.* **2018**, *2*, 8; b) J. Dragas, D. Jäckel, A. Hierlemann, F. Franke, *IEEE Trans. Neural Syst. Rehabil. Eng.* **2015**, *23*, 149; c) X. Yu, Z. Xie, Y. Yu, J. Lee, A. Vazquez-Guardado, H. Luan, J. Ruban, X. Ning, A. Akhtar, D. Li, B. Ji, Y. Liu, R. Sun, J. Cao, Q. Huo, Y. Zhong, C. Lee, S. Kim, P. Gutruf, C. Zhang, Y. Xue, Q. Guo, A. Chempakasseril, P. Tian, W. Lu, J. Jeong, Y. Yu, J. Cornman, C. Tan, B. Kim, *Nature* **2019**, *575*, 473; d) R. Dahiya, N. Yogeswaran, F. Liu, L. Manjakkal, E. Burdet, V. Hayward, H. Jörntell, *Proc. IEEE* **2019**, *107*, 2016; e) R. Dahiya, *Proc. IEEE* **2019**, *107*, 247.
- [4] a) A. Christou, F. Liu, R. Dahiya, *Microsyst. Nanoeng.* **2021**, *7*, 82; b) C. García Núñez, F. Liu, W. T. Navaraj, A. Christou, D. Shakhthivel, R. Dahiya, *Microsyst. Nanoeng.* **2018**, *4*, 22.
- [5] a) A. Zumeit, A. S. Dahiya, A. Christou, D. Shakhthivel, R. Dahiya, *npj Flex. Electron.* **2021**, *5*, 18; b) A. Zumeit, A. S. Dahiya, A. Christou, R. Dahiya, *Jpn. J. Appl. Phys.* **2022**, *61*, SC1042; c) A. Zumeit, W. T. Navaraj, D. Shakhthivel, R. Dahiya, *Adv. Electron. Mater.* **2020**, *6*, 1901023.
- [6] A. S. Dahiya, D. Shakhthivel, Y. Kumaresan, A. Zumeit, A. Christou, R. Dahiya, *Nano Convergence* **2020**, *7*, 33.
- [7] Y. Gao, Y. Zhang, X. Wang, K. Sim, J. Liu, J. Chen, X. Feng, H. Xu, C. Yu, *Sci. Adv.* **2017**, *3*, e1701222.
- [8] a) E. Ozer, J. Kufel, J. Myers, J. Biggs, G. Brown, A. Rana, A. Sou, C. Ramsdale, S. White, *Nat. Electron.* **2020**, *3*, 419; b) F. Liu, A. S. Dahiya, R. Dahiya, *Nat. Electron.* **2020**, *3*, 358.
- [9] J.-K. Chang, H. Fang, C. A. Bower, E. Song, X. Yu, J. A. Rogers, *Proc. Natl. Acad. Sci. USA* **2017**, *114*, E5522.
- [10] C. García Núñez, F. Liu, S. Xu, R. Dahiya, DOI: <https://doi.org/10.1017/9781108691574>, Cambridge University Press, Cambridge **2018**.
- [11] H.-J. Kim-Lee, A. Carlson, D. S. Grierson, J. A. Rogers, K. T. Turner, *J. Appl. Phys.* **2014**, *115*, 143513.
- [12] a) J. J. H. Togonon, E. A. Esparcia, Jr., J. A. D. Del Rosario, J. D. Ocon, *ChemistryOpen* **2021**, *10*, 471; b) S.-K. Kang, S.-W. Hwang, S. Yu, J.-H. Seo, E. A. Corbin, J. Shin, D. S. Wie, R. Bashir, Z. Ma, J. A. Rogers, *Adv. Funct. Mater.* **2015**, *25*, 1789.
- [13] C. P. Constantin, M. Aflori, R. F. Damian, R. D. Rusu, *Materials* **2019**, *12*, 3166.
- [14] A. S. Dahiya, R. A. Sporea, G. Poulin-Vittrant, D. Alquier, *Sci. Rep.* **2019**, *9*, 2979.
- [15] A. S. Dahiya, C. Opoku, G. Poulin-Vittrant, N. Camara, C. Daumont, E. G. Barbagioanni, G. Franzò, S. Mirabella, D. Alquier, *ACS Appl. Mater. Interfaces* **2017**, *9*, 573.
- [16] U. Zschieschang, J. W. Borchert, M. Giorgio, M. Caironi, F. Letzkus, J. N. Burghartz, U. Waizmann, J. Weis, S. Ludwigs, H. Klauk, *Adv. Funct. Mater.* **2020**, *30*, 1903812.
- [17] J. Biggs, J. Myers, J. Kufel, E. Ozer, S. Craske, A. Sou, C. Ramsdale, K. Williamson, R. Price, S. White, *Nature* **2021**, *595*, 532.
- [18] a) E. S. Hosseini, S. Dervin, P. Ganguly, R. Dahiya, *ACS Appl. Bio Mater.* **2021**, *4*, 163; b) S.-K. Kang, R. K. J. Murphy, S.-W. Hwang, S. M. Lee, D. V. Harburg, N. A. Krueger, J. Shin, P. Gamble, H. Cheng, S. Yu, Z. Liu, J. G. McCall, M. Stephen, H. Ying, J. Kim, G. Park, R. C. Webb, C. H. Lee, S. Chung, D. S. Wie, A. D. Gujar, B. Vemulapalli, A. H. Kim, K.-M. Lee, J. Cheng, Y. Huang, S. H. Lee, P. V. Braun, W. Z. Ray, J. A. Rogers, *Nature* **2016**, *530*, 71.
- [19] M. J. Christoe, J. Yuan, A. Michael, K. Kalantar-Zadeh, *IEEE Access* **2021**, *9*, 85144.
- [20] R. Raman, T. Hua, D. Gwynne, J. Collins, S. Tamang, J. Zhou, T. Esfandiary, V. Soares, S. Pajovic, A. Hayward, R. Langer, G. Traverso, *Sci. Adv.* **2020**, *6*, eaay0065.
- [21] C. W. Park, S.-K. Kang, H. L. Hernandez, J. A. Kaitz, D. S. Wie, J. Shin, O. P. Lee, N. R. Sottos, J. S. Moore, J. A. Rogers, S. R. White, *Adv. Mater.* **2015**, *27*, 3783.
- [22] K. Sim, X. Wang, Y. Li, C. Linghu, Y. Gao, J. Song, C. Yu, *J. Micro-mech. Microeng.* **2017**, *27*, 065010.
- [23] J. K. Jeong, H. W. Yang, J. H. Jeong, Y.-G. Mo, H. D. Kim, *Appl. Phys. Lett.* **2008**, *93*, 123508.
- [24] a) K. Choi, S. R. A. Raza, H. S. Lee, P. J. Jeon, A. Pezeshki, S.-W. Min, J. S. Kim, W. Yoon, S.-Y. Ju, K. Lee, S. Im, *Nanoscale* **2015**, *7*, 5617; b) Y. Paska, H. Haick, *ACS Appl. Mater. Interfaces* **2012**, *4*, 2604.
- [25] a) D.-H. Kim, H.-S. Jeong, D.-H. Lee, K.-H. Bae, S. Lee, M.-H. Kim, J.-H. Lim, H.-I. Kwon, *Coatings* **2021**, *11*, 1192; b) D. H. Kim, S. Choi, J. Jang, H. Kang, D. M. Kim, S.-J. Choi, Y.-S. Kim, S. Oh, J. H. Baeck, J. U. Bae, K.-S. Park, S. Y. Yoon, I. B. Kang, *J. Soc. Inf. Disp.* **2017**, *25*, 98.
- [26] a) A. Kuo, T. K. Won, J. Kanicki, *IEEE Trans. Electron Devices* **2008**, *55*, 1621; b) J. M. Shannon, *Appl. Phys. Lett.* **2004**, *85*, 326.
- [27] A. S. Dahiya, C. Opoku, C. Oshman, G. Poulin-Vittrant, F. Cayrel, L.-P. T. H. Hue, D. Alquier, N. Camara, *Appl. Phys. Lett.* **2015**, *107*, 033105.
- [28] a) Y.-H. Lee, Y.-J. Cho, W.-S. Kim, J. K. Park, G. T. Kim, O. Kim, *Jpn. J. Appl. Phys.* **2017**, *56*, 108001; b) P.-T. Liu, Y.-T. Chou, L.-F. Teng, *Appl. Phys. Lett.* **2009**, *95*, 233504; c) W. Kim, A. Javey, O. Vermesh, Q. Wang, Y. Li, H. Dai, *Nano Lett.* **2003**, *3*, 193.
- [29] S.-K. Kang, S.-W. Hwang, H. Cheng, S. Yu, B. H. Kim, J.-H. Kim, Y. Huang, J. A. Rogers, *Adv. Funct. Mater.* **2014**, *24*, 4427.
- [30] a) Y.-F. Huang, S.-L. Chou, S.-L. Lo, *Sustainable Environ. Res.* **2022**, *32*, 6; b) M. Sethurajan, E. D. van Hullebusch, D. Fontana, A. Akcil, H. Deveci, B. Batinic, J. P. Leal, T. A. Gasche, M. A. Kucuker, K. Kuchta, I. F. F. Neto, H. M. V. M. Soares, A. Chmielarz, *Crit. Rev. Environ. Sci. Technol.* **2019**, *49*, 212.
- [31] M. Chakraborty, J. Kettle, R. Dahiya, *IEEE J. Flex. Electron.* **2021**, *1*, 4.