High performance of n++GaN/AlN/GaN high electron mobility transistor

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Abstract

In this work, we report the processing and DC performance of n++GaN/AlN/GaN high electron mobility transistors with a recessed gate structure. The n++GaN cap layer is selectively removed under the gate region using SF_6/O_2. The fabricated device shows a maximum drain current density of over 1000 mA/mm at V_{GS}=+3 V and a maximum peak transconductance of 240 mS/mm at V_{DS}=5 V. The breakdown voltage of the device is over 95 V. The measured contact resistance between 0.4 to 0.6 Ω.mm is obtained using circular TLM. These results indicate the potential of n++GaN/AlN/GaN HEMT structure to be used for future high frequency power application.

Introduction

AlGaN/GaN high electron mobility transistors (HEMTs) have been successfully demonstrated in MMIC technology for various frequencies including mm-wave range [1]. While the gate length, L_G, scaling technologies enable AlGaN/GaN HEMTs to be promising candidates for higher frequency power applications, the gate to channel distance, d, must be scaled to mitigate the short channel effects (SCEs) [2]. To have a high aspect ratio of L_G/d, the ultra-thin AlN/GaN HEMTs have been widely investigated due to its large spontaneous and piezoelectric polarization effect which leads to a very high charge carrier density up to 3 x 10^{13} cm^{-2} [3]. Excellent DC and RF performances have been reported for this structure [4]. However, the main challenge to fabricate AlN/GaN HEMTs is to form low Ohmic contact resistance on this thin AlN barrier layer. In this work, the epitaxial structure is protected with a 5-nm heavily doped n++GaN cap layer (~1 x 10^{19} cm^3 Si doped). It is believed that the heavily doped n++GaN cap layer can help in reducing the contact resistance of the device. We discuss the processing and DC characterization of n++GaN/AlN/GaN HEMT structures in the next sections of the paper.

Experimental

The epitaxial structure used in this work was grown by SVT Associates, USA, using molecular beam epitaxy on sapphire substrate. The wafer structure consists of (from top to bottom), a 5-nm heavily doped GaN cap layer with Si-doping density of 1 x 10^{19} cm^3, 3-nm AlN, 1.4-µm GaN channel layer, 0.8-µm GaN buffer layer, and a very thin AlN nucleation layer. A two-level wrap-around gate design (where the gate encircles the drain) was used to simplify the device process flow, removing the need for isolation. First, Ohmic metal contacts were formed by evaporation of Ti/Al/Ni/Au, followed by a lift-off process then annealed at 800 °C for 30 secs. Prior to gate metallisation, the 5-nm n++ GaN cap layer in the gate region is selectively removed using SF_6/O_2. Finally, the gate metal contacts were formed by evaporation of Ni/Au, followed by a lift-off process. All fabrication steps were defined using photolithography. The cross-section schematic diagram of fabricated device is shown in Figure 1. DC measurements were made at room temperature using Agilent's B1500A Semiconductor Device Analyzer.

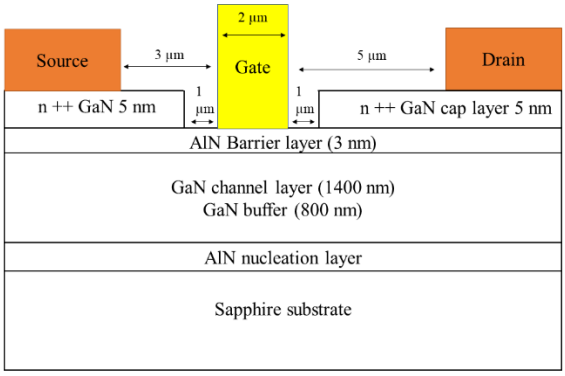

Figure 1. Cross-section schematic diagram of fabricated n++GaN/AlN/GaN HEMT structure. Device dimension used in this work is as follows: Gate length, L_G = 2 µm, gate-to-source distance, L_{GS} = 3 µm, gate-to-drain distance, L_{GD} = 5 µm, and gate width, W_G = 75 µm.

Results and discussion

The contact resistances were measured using the circular TLM and provide values between 0.4 to 0.6 Ω.mm across the sample. This low contact resistance measurements is due to the usage of a heavily doped n++GaN cap layer. Figure 2 shows an AFM scan image for both the un-etched and etched surfaces of n++GaN/AlN/GaN HEMT. From this measurement, the 5-nm of heavily doped GaN cap layer is successfully removed using the combination of gases SF_6 and O_2 with RF power of 70 W power and pressure of 50 mTorr. The maximum current density, $I_{DS(max)}$, and maximum peak transconductance, $g_{m(max)}$, of the fabricated device were over 1000 mA/mm at V_{GS} = 3 V and 240 mS/mm at V_{DS} = 5 V respectively. These values are shown in Figures 3 and 4 respectively. The threshold voltage, V_{TH}, of the fabricated device was -2.6 V (value was extracted at I_{DS} = 1 mA/mm). The measured gate leakage current characteristics shown in Figure 5 while the off-state breakdown voltage, V_{BR}, was over 95 V measured at V_{GS} =-5 V shown in Figure 6. Further device improvement can be done by employing the gate

dielectric to the device. Currently we are working on fabricating the smaller gate length ($L_g \leq 100$ nm) devices using electron beam lithography for used in W-band application.

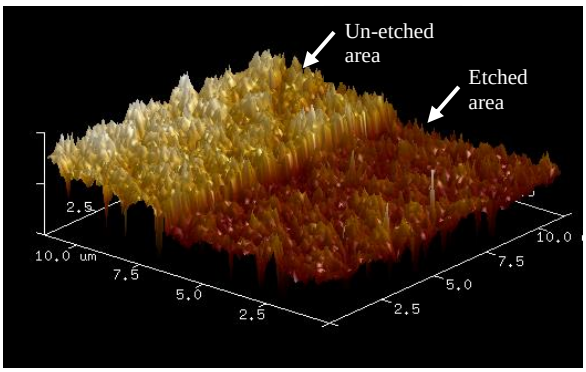

Figure 2. Atomic force microscope scan image showing both unetched and etched surfaces of n++GaN/AlN/GaN HEMT.

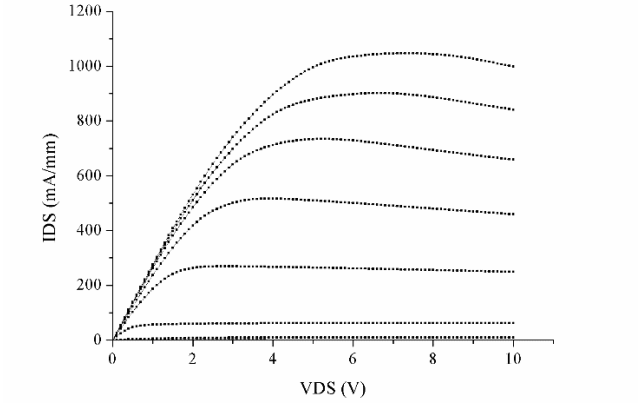

Figure 3. Measured output characteristics of fabricated device with a gate-to-source voltage, V_{GS}, biasing from -4 V to 3 V (with step size of 1 V).

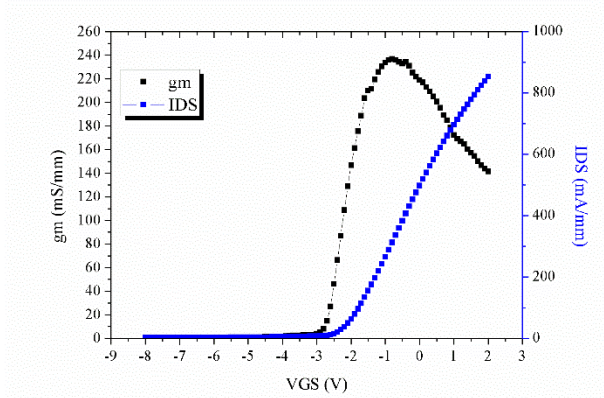

Figure 4. Measured transfer characteristics of fabricated device at a drain-to-source voltage, V_{DS} = 5 V.

Conclusions

We have successfully fabricated and measured heavily doped n++GaN/AlN/GaN HEMT structures. Very good DC characteristics have been demonstrated for this structure where the fabricated device with L_G = 2 µm show $I_{DS(max)}$ = 1047 mA/mm, $g_{m(max)}$ = 240 mS/mm, V_{TH} = -2.6 V, and $V_{BR} \approx$ 100 V. Further device performance improvements can be expected by reducing the device dimension (i.e., L_G, L_{DS}, L_{GS}) and by adopting the T-gate technology. The usage of a heavily doped n++ GaN cap layer and thin AlN barrier which gives a very high aspect ratio of L_G/d is shown to be promising for future high frequency power application.

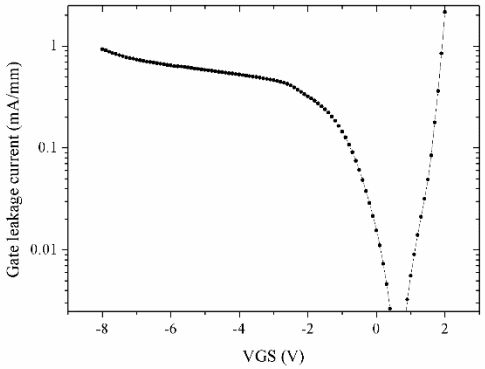

Figure 5. Measured gate leakage current characteristics at a drain-to-source voltage, V_{DS} = 1 V.

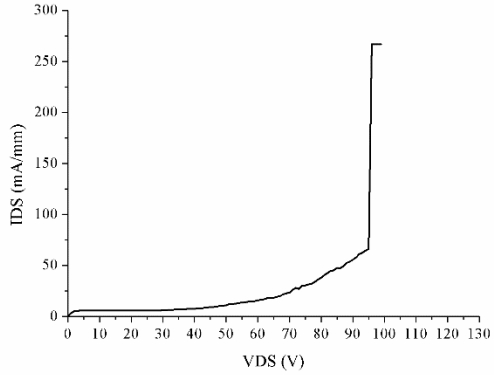

Figure 6. The off-state breakdown characteristics of fabricated device at a gate-to-source voltage, V_{GS} = -5 V.

Acknowledgments

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References

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