# Carbon Nanotube SRAM in 5-nm Technology Node Design, Optimization, and Performance Evaluation—Part II: CNT Interconnect Optimization

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***Abstract*— The size and parameter optimization for the 5-nm carbon nanotube field effect transistor (CNFET) static random access memory (SRAM) cell was presented in Part I of this article. Based on that work, we propose a carbon nanotube (CNT) SRAM array composed of the schematically optimized CNFET SRAM and CNT interconnects. We consider the interconnects inside the CNFET SRAM cell composed of metallic single-wall CNT (M-SWCNT) bundles to represent the metal layers 0 and 1 (M0 and M1). We investigate the layout structure of CNFET SRAM cell considering CNFET devices, M-SWCNT interconnects, and metal electrode Palladium with CNT (Pd-CNT) contacts. Two versions of cell layout designs are explored and compared in terms of performance, stability, and power efficiency. Furthermore, we implement a 16 Kbit SRAM array composed of the proposed CNFET SRAM cells, multiwall CNT (MWCNTs) inter-cell interconnects and Pd-CNT contacts. Such an array shows significant advantages, with the read and write overall energy-delay product (EDP), static power consumption, and core area of 0.28×, 0.52×, and 0.76× respectively to 7-nm FinFET-SRAM array with copper interconnects, whereas the read and write static noise margins are 6% and 12% respectively larger than the FinFET counterpart.**

***Index Terms*— Area, carbon nanotube (CNT) interconnect, carbon nanotube field effect transistor (CNFET) static random access memory (SRAM) array, energy-delay-product (EDP), FinFET SRAM array, layout, read latency, static noise margin, write latency.**

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## I. Introduction

IN THE ultra-deep sub-micrometer regime, interconnects rather than devices play a decisive role in the performance and power dissipation of integrated circuits [1]. Thus, we find it relevant to consider their impact on carbon nanotube field effect transistor (CNFET) static random access memory (SRAM) performance. There have been some experimental and simulation works of CNFET circuit application where copper (Cu) is applied as back-end-of-line (BEOL) metal [2], [3]. Carbon nanotube (CNT) interconnects, including single-walled CNT (SWCNT) and multiwalled CNT (MWCNT), have been shown to alleviate some of the issues currently faced with Cu interconnects such as electromigration due to their high current-carrying capacity [4]–[6]. Moreover, it has been found that compared with Cu interconnect, even though single SWCNT is not suitable as global interconnect due to its large ohmic resistance, both single MWCNT and SWCNT bundle have super conductivity and can provide improvement in delay and power efficiency for global interconnect routing in multicore chip applications [7]. Hence, in this work, we consider the intra-cell interconnects (connect device metal electrodes with BEOL interconnect layers 0 and 1) composed of SWCNT inside the CNFET SRAM cell and inter-cell interconnects [as bit and word lines (WLs)] with MWCNT. Experimental work has demonstrated that both metallic SWCNT [8] and metallic MWCNT [9] are good candidates of high-performance circuit interconnects that can operate more than 1 GHz frequency. In addition, doping techniques, such as $NO_2$, $H_2SO_4$, $SOCL_2$, $PtCl_4$, etc., [10]–[15] have been experimentally found to be effective in significantly improving the conductance of CNT interconnects. We use the CNT interconnect models based on compact models proposed in [16] and [17]. For the intra-cell interconnect design, to obtain the best CNT interconnect electrical performance, side-contacts instead of end-contacts [18] are

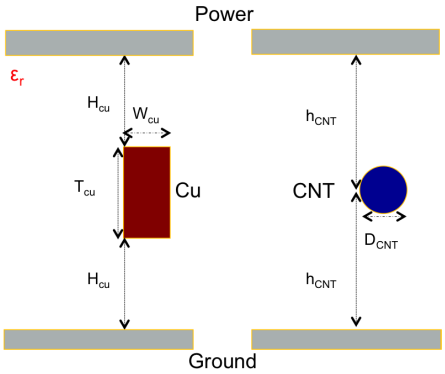



Fig. 1. Geometric structure of interconnects (layers 1 to 3) between ground/power lines. The dielectric constant $\varepsilon_r$ is set as 2, which is low and in the roadmap of future technologies. $T_{\text{cu}} = 2W_{\text{cu}}$ and $h_{\text{cnt}} = H_{\text{cu}} + T_{\text{cu}}/2$. $W_{\text{cu}}$ is from Table I and $H_{\text{cu}} = 20$ nm.

considered to enable multiple metal electrode-CNT contacts without introducing additional contact resistance. We investigate two versions of CNFET SRAM layout designs (based on the schematically optimized 5-nm CNFET SRAM cell in Part I of this article [19]) considering CNFET devices, intra-cell CNT interconnects and contacts where we evaluate layout area, performance and power consumption. Furthermore, we implement a 16 Kbit CNFET SRAM design labeled as all carbon SRAM (ACS) which combines the physically designed CNFET SRAM cell with inter-cell MWCNT interconnects for SRAM array-level evaluations. Finally, we compare the ACS array with a 7-nm FinFET SRAM array of the same capacity which is composed of the schematically optimized 7-nm FinFET SRAM cell (in Part I of this article) and Cu interconnects (for both intra- and inter-cells) in the aspects of area, performance, stability, and power efficiency.

The rest of this article is organized as follows. In Section II, Cu and CNT as BEOL interconnects for the 7-nm FinFET and 5-nm CNFET SRAM arrays are introduced, respectively. In Section III, we present the two versions of CNFET SRAM cell layout designs and compare them in terms of layout area, performance, stability, and power consumption. In Section IV, we implement an ACS for array-level evaluations. In Section V, optimal configurations for inter-cell CNT interconnects are derived, and the ACS design is compared with the FinFET counterpart to illustrate the advantage of ACS design. Section VI concludes this article.

## II. Cu and CNT Interconnect Description

For FinFET SRAM cell design, we consider copper interconnect geometries based on 7-nm technology node [20], [21] with details provided in Fig. 1 and Table I. The selected 7-nm FinFET technology node is a representation of one of the most advanced technology node of silicon. A more advanced node like 5 nm or below will enable silicon technology to have more advantage in power, performance, and area compared to the CNFET SRAM. For CNFET SRAM cell design, we consider single-walled CNT (SWCNT) bundles or multiple SWCNTs connected in parallel to reduce the interconnect parasitic resistance. SWCNT bundle can be arranged in such a way that the distance between SWCNTs is equal or larger than (assumed

TABLE I
Layout Design Rules for 7-nm FinFET and 5-nm CNFET SRAMs [21], [22]

| Technology parameters | FinFET | CNFET |
|---|---|---|
| Minimum $CGP$ (nm) | 54 | 42 |
| Minimum active width $Wa$ (discrete) (nm) | 27 | 21 |
| Minimum active to active distance $Da$ (nm) | 27 | 21 |
| Interconnect layers 1 to 3 minimum width (nm) | 18 | 12 |
| Minimum via or contact width (nm) | 18 | - |

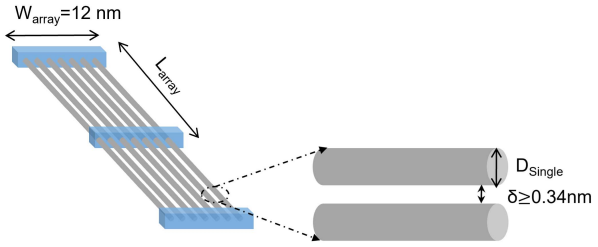



Fig. 2. Illustration of SWCNT bundle and related parameters. The distance between CNT $\delta$ is not small than the van der Waals gap, 0.34 nm.

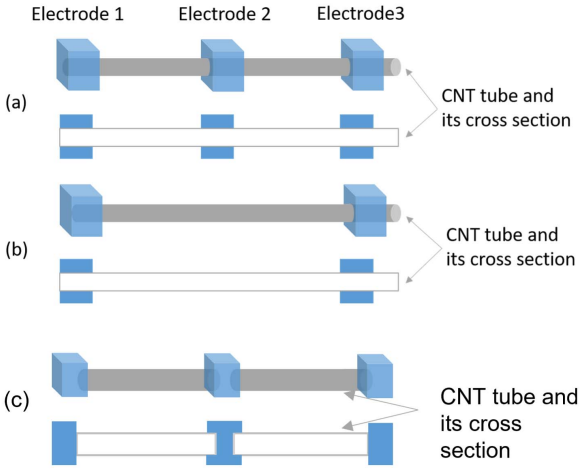



Fig. 3. Side-contact to connect multiple metal electrodes: (a) and (b) contain three and two electrodes, respectively. Here the metal electrode is Palladium (Pd), forming Pd-CNT side-contact. Also shown is the three electrodes case for end-contact in (c).

in this work, as shown in Fig. 2) the van der Waals distance of 0.34 nm. In general, there are two types of contacts between CNT interconnects and metal electrodes, i.e., side-contacts and end-contacts. The side-contact is inversely dependent on the contact length along the CNT while the end-contact is inversely dependent on the diameter or cross-sectional area of the CNT [16]. The other difference is that the end-contact is formed between the CNT end and the metal whereas, the side-contact is formed between the CNT side surface and metal. Hence, end-contacts are covalent metal-carbon bonds, and side-contacts are van der Waals bonds. Due to the structure difference, side-contacts allow multiple electrodes along a single CNT tube without the need to create multiple end-contacts between shorter CNT tubes, which would lead to overall more contact resistance. For example, as shown in Fig. 3(a) and (b), the total side-contact resistance between

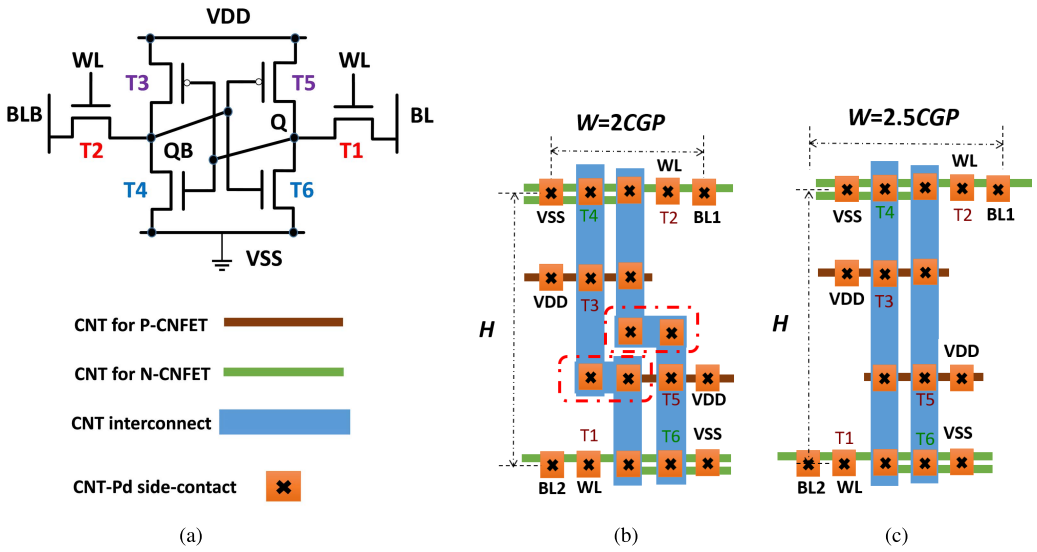



Fig. 4. CNFET SRAM cell. (a) SRAM schematic and layout layers illustration, where Pd-CNT side-contact is used for CNFET source/drain/gate electrodes connection with CNT (refer to Fig. 3). (b) and (c) Two SRAM layout structure designs (not drawn to scale) for the baseline and proposed structures, respectively. Please note that FinFET SRAM can have a similar layout design where CNFET, CNT interconnect, and Pd-CNT contact are replaced with FinFET, Cu interconnect, and pure metal contact respectively using the design rules shown in Table I.

electrodes 1 and 3 are the same. However, if end-contact was used, it would require two noncontinuous CNT tubes (two shorter CNT tubes) connected at electrode 2, thus, leading to additional contact resistance, as shown in Fig. 3(c). In this work, the intra-cell interconnect electrodes at the source, drain and gate are of Palladium (Pd) [23], forming Pd-SWCNT side-contacts. Whereas for inter-cell interconnect such as bit and WLs, MWCNT with Pd-CNT end-contact are used instead.

## III. Layout Structure of CNFET SRAM

We investigate two versions of layout structures for CNFET SRAM, as shown in Fig. 4(b) and (c) where the schematic and layer details are in Fig. 4(a). The numbers of CNTs underneath the gates of the pull-up, access, and pull-down transistors are 1, 1, and 2 respectively, as optimized and determined in Part I of this article. The layout structure in Fig. 4(b) is based on [24], also labeled as baseline layout structure. Our proposed layout structure is shown in Fig. 4(c), which is an updated version of the baseline layout but the layout is extended in the horizontal direction by half of the contact gate pitch (CGP). The main reason for such an extension is to allow CNT interconnects to run long and uninterrupted by contacts, which causes an increase in resistance. Our goal is to propose a CNT-aware layout structure to exploit the advantage of CNT physical properties. For example, as CNTs provide long mean free paths, having short CNT interconnects does not allow to exploit this property, furthermore introduces more CNT-metal contacts which overall increase interconnect resistance. Thus, the proposed layout extension leads to fewer contacts, long and continuous CNT interconnects than the baseline layout [highlighted by dot dash boxes in Fig. 4(b)] at the cost of only 25% area increase.

We design the layout structure of the schematically optimized 5-nm CNFET SRAM cell in Part I of this article and the design rules are listed in Table I. SWCNT bundles are used as intra-cell interconnects inside the CNFET SRAM, as shown in Fig. 2. According to the 7-nm FinFET technology, the copper interconnects in the layers 1–3 have the same design rules, thus, we also assume that the CNT interconnects for these layers have same geometric structures as shown in detail in Table I. For CNFET, the minimum CGP and metal 1 width are 42 and 12 nm, respectively [22]. However, as in the Part I of this article, the 31.1 nm CGP is still applied to the CNFET compact modeling here to obtain a conservative estimation of the CNFET-SRAM performance. The reason is that a more relaxed CGP in CNFET should allow for an increase in contact length between CNT and metal electrode which reduces the contact resistance and hence improves the CNFET-SRAM performance. Since the design rule of the active area of 5-nm CNFET is not available, we assume it to be proportional to the CGP of 7-nm FinFET. Details of these parameters are presented in Table I.

Similarly, the FinFET SRAM layout can be designed with schematically optimized FinFET SRAM cell as derived in Part I of this article and the design rules are also listed in Table I and made available by [21]. FinFET SRAM intra-cell interconnects are made of copper with an aspect ratio of 2. The geometric structure of interconnects between ground/power is shown in Fig. 1. The coupling capacitance between interconnects on the same metal layer (relatively small) is ignored while coupling to power/ground (or neighboring interconnect layers) is considered. The distance between the top/bottom surface of the evaluated interconnect to the power/ground is set as 20 nm [$H_{cu}$ (in Fig. 1)], which is smaller than the nominal value of 36 nm [25]. Hence, it increases the coupling capacitance to power/ground. This to some extent compensates for the exclusion of mutual coupling from neighboring interconnects on the same interconnect layer. The estimation of coupling capacitance to ground/power considering the fringing effect is based on [26] and [27] for Cu (rectangular cross section) and CNT (round cross section), respectively. The inductance in CNT and Cu interconnects are not considered

in this work due to its relative small impact than the RC in the scale of interconnect dimensions in this article. There are pretty many works on CNT inductance modeling and its impact on interconnect performance and reliability [28]–[30].

### A. Interconnect Parasitics

As mentioned, we consider Pd-CNT side-contacts, which are inversely proportional to the contact length along the CNT interconnect. As shown in [31], the Pd-CNT total side-contact resistance can be reduced from ∼20 to 3.25 kΩ by increasing the contact length from ∼20 to 300 nm. The 3.25 kΩ is the quantum limit. Besides the quantum resistance, the additional parasitic contact resistance is due to Schottky barriers between metal to CNT interface. In this article, we assume the Pd-CNT additional (imperfect) contact resistance varies from 20 to 0 kΩ, indicating the total Pd-CNT contact resistance varying from 23.25 to 3.25 kΩ. We also take into account the other parasitics such as CNT intrinsic resistance and capacitance as derived in [32]. Whereas, for 7-nm FinFET technology, copper interconnects have a resistivity of ∼96 Ω · nm, and the contact resistance between copper and device electrodes is ∼25 Ω for the 18 nm via or contact size [33]. We incorporate these parasitic parameters to both layout structures to compute more realistically the performance, power consumption, and stability of FinFET and CNFET SRAMs. It should be noted that in the cell level, read/write delay/dynamic power and static power, read/write noise margin are characterized/simulated as in the part I of this article including the same supply voltage of 0.7 V for both the technologies. And similar to the cell-level characterization, the author mainly used SPICE simulation (including Cadence specter and Synopsys hspice tools) to evaluate the different types of circuits and technologies with parasitic parameters extracted and considered. The extracted parasitic parameters of CNT/Cu interconnects are mainly based on analytic calculation and estimation, which however has been demonstrated to be close to the numerical simulation results. In the array level, the inter-cell parasitics are further included to simulate the whole SRAM array read/write dynamic power and performance. The detailed descriptions of the read/write operations are presented in Section V-A of this article.

### B. Read and Write Performance

The performance of CNFET SRAM with CNT interconnects is compared with an ideal case (i.e., CNFET SRAM with ideal interconnects, no contact, interconnect resistance, or capacitance) to evaluate the impact of intra-cell interconnect parasitics. Fig. 5(a) and (b) show the change of read energy-delay product (EDP) due to parasitics of CNT-metal contacts while varying SWCNT diameter, $D_{\text{cnt}}$ and number of SWCNT bundles, $N_{\text{cnt}}$, respectively. Both Fig. 5(a) and (b) show that an increase in contact resistance leads to an increase in the read EDP. This indicates the resistance (mainly induced by contact resistance) from intra-cell interconnect leads to degraded EDP. Furthermore, when the additional contact resistance is low such as 0 kΩ, the EDP is smaller than the ideal case, indicating that parasitic capacitance from intra-cell interconnect improves

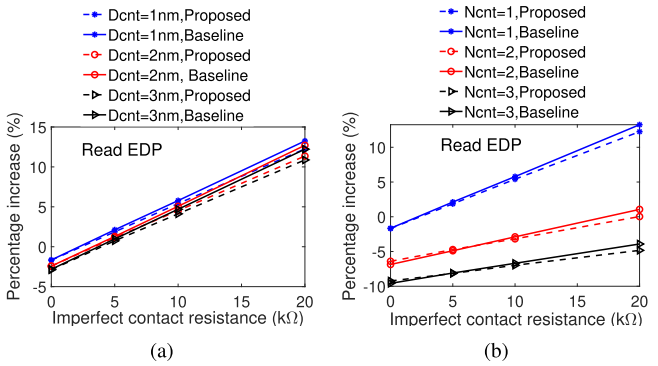



Fig. 5. CNFET SRAM Read EDP dependence on the SWCNT diameter $D_{\text{cnt}}$ and the number of SWCNT bundles, $N_{\text{cnt}}$. (a) $N_{\text{cnt}} = 1$ with varying CNT diameter, $D_{\text{cnt}}$. (b) $D_{\text{cnt}} = 1$ nm with varying number of CNTs, $N_{\text{cnt}}$.

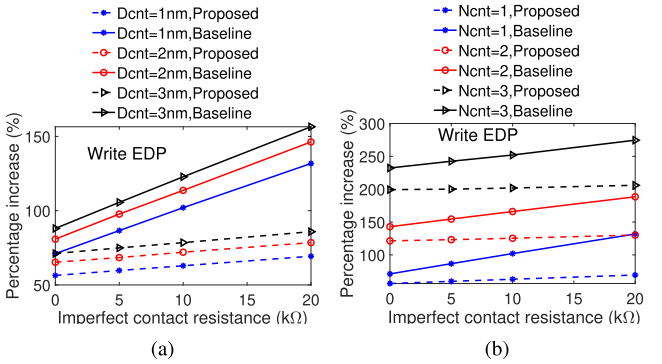
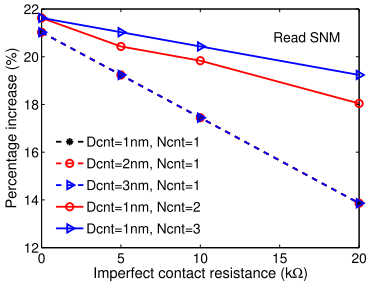


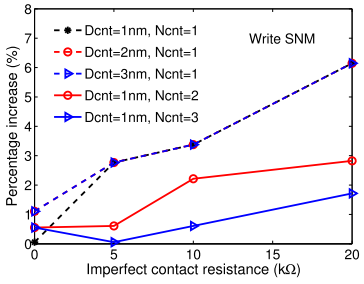

Fig. 6. CNFET SRAM Write EDP dependence on the SWCNT diameter, $D_{\text{cnt}}$ and number of SWCNT bundles, $N_{\text{cnt}}$. (a) $N_{\text{cnt}} = 1$ with varying CNT diameter, $D_{\text{cnt}}$. (b) $D_{\text{cnt}} = 1$ nm with varying number of CNTs, $N_{\text{cnt}}$.

the SRAM EDP. Hence, the parasitic capacitance and contact resistance from intra-cell interconnect have opposite roles in the read EDP. This also explains that the read EDP decreases with the SWCNT diameter $D_{\text{cnt}}$ and the number of CNTs $N_{\text{cnt}}$, as shown in Fig. 5, because the CNT parasitic capacitance increases with $D_{\text{cnt}}$ and $N_{\text{cnt}}$. Also, we observe almost no improvement in the read EDP of the proposed layout structure compared with the baseline one. This is because the proposed layout design can reduce both intra-cell interconnect parasitic capacitance and contact resistance, which however has an opposing effect (i.e., they offset each other) on the read EDP.

For write case, we observe a different trend from the read case. As shown in Fig. 6(a) and (b), even though write EDP increases with contact resistance as in the read case, the parasitic capacitance from intra-cell interconnect also leads to degraded write EDP which is opposite to the read case. For example, when the additional contact resistance is 0, the write EDP is still much larger than the ideal write case (no parasitics from intra-cell interconnect), indicating the degraded impact from parasitic capacitance. Furthermore, as shown in Fig. 6(a), write EDP increases with CNT diameter, which increases capacitance, further implying that CNT parasitic capacitance increases the write EDP; as illustrated in Fig. 6(b), when the $N_{\text{cnt}}$ increases from 1 to 3 (3× parasitic capacitance increase) a drastic increase in write EDP is observed. Hence, as the proposed layout reduces both parasitic capacitance and resistance from intra-cell interconnect, the write EDP is significantly better than the baseline case, as shown in Fig. 6.




(a)




(b)

Fig. 7. CNFET SRAM read and write SNM dependence on the SWCNT diameter, $D_{\text{cnt}}$ and the number of SWCNTs, $N_{\text{cnt}}$. (a) Read SNM. (b) Write SNM.

Overall, we deduce that both CNT interconnects and contacts (in terms of $D_{\text{cnt}}$ and $N_{\text{cnt}}$ on the layout structure) impact CNFET SRAM read and write performance. We find that sets of $D_{\text{cnt}} = 3$ nm, $N_{\text{cnt}} = 3$ and $D_{\text{cnt}} = 1$ nm, $N_{\text{cnt}} = 1$ can be optimal choices for read performance and write performance, respectively. However, considering the more degrading impact from intra-cell interconnects on write EDP than read EDP, parameters $D_{\text{cnt}} = 1$ nm and $N_{\text{cnt}} = 1$ are more suitable to better trade-off between the write and read EDP optimization.

### C. Read and Write SNM and Static Power Consumption

Here, we investigate both read and write SNMs of CNFET SRAM when considering the layout structure such as CNT interconnect diameter, bundle and contacts. Fig. 7(a) and (b) show that both read and write SNMs are improved. It is relevant to note that the read SNM means how much interior noise margin an SRAM cell has during the read operation while the write SNM represents the tolerance against noise for a successful write operation.

We find that CNT interconnect parasitic resistance and capacitance render CNFET SRAM more resistant to bitline (BL/BLB) disturbance during the read and the write operations, resulting in increased read SNM up to 22% and write SNM up to 1% with no contact resistance as shown in Fig. 7(a) and (b). However, once contacts are considered, the read and write SNMs change in opposite directions. This is because the increase in contact resistance reduces the effective supply voltage of the SRAM cell due to increased voltage drop in the contact resistance between the power/ground line and SRAM cell local VDD/VSS as shown in Fig. 4. Such voltage drop causes the SRAM cell to be more easily influenced by the BL/BLB disturbance, i.e., lower read SNM, which has also been demonstrated by simulations in [34].

On the contrary, the write SNM is improved when the contact resistance increases, which is because an increase in contact resistance leads to smaller effectively supply voltage for SRAM cell and hence more easily flipping the SRAM cell state during write operation [34]. As both the proposed and baseline layout structures have the same power supply and the corresponding contact resistance structure, we also obtain identical read and write SNMs. Finally, though not shown here, it is found that parasitics of CNT interconnects and contacts have a negligible impact on the static power consumption of CNFET SRAM cell. By comparison, we deduce that CNT interconnect and contact parasitics improve more read SNM than write SNM. Hence, to simultaneously optimize the read and write SNM of CNFET SRAM cell, we select parameters of $D_{\text{cnt}} = 1$ nm and $N_{\text{cnt}} = 1$ which is consistent with the read and write performance optimization results as well.

TABLE II

COMPARISON OF FINFET SRAM AND CNFET SRAM (CONTACT RESISTANCE IS 10 kΩ) WITH DIFFERENT LAYOUT DESIGNS. THE ∗ INDICATES THE RECOMMENDED LAYOUT STRUCTURE FOR THE FINFET AND CNFET SRAM CELLS

| | FinFET SRAM | | CNFET SRAM | |
|---|---|---|---|---|
| Performance | Proposed | Baseline (∗) | Proposed (∗) | Baseline |
| Read EDP (aJ·ps) | 16.45 | 16.43 | 3.684 | 3.697 |
| Read SNM (V) | 0.1857 | 0.1857 | 0.1966 | 0.1966 |
| Write EDP (fJ·ps) | 2.597 | 2.741 | 0.9089 | 1.127 |
| Write SNM (V) | 0.1662 | 0.1662 | 0.1867 | 0.1867 |
| Static power (pW) | 51.13 | 51.13 | 26.53 | 26.53 |
| Area ($\mu$m$^2$) | 0.0328 | 0.0262 | 0.0198 | 0.0159 |

### D. Comparison With 7-nm FinFET SRAM Cell

The simulation results of the 7-nm FinFET SRAM including the impact of Cu interconnects (layout structure is similar to Fig. 4) are listed in Table II. Although the proposed layout structure for FinFET SRAM cell has some benefit in write EDP, the overall benefits are not significant. Thus, the proposed layout structure is not suggested for FinFET SRAM considering also its 25% area overhead compared with the baseline counterpart.

On the proposed layout structure for CNFET SRAM cell, we utilize CNT interconnects with $D_{\text{cnt}} = 1$ nm and $N_{\text{cnt}} = 1$, and contact resistance of 10 kΩ. From simulations, we obtain an important improvement in write EDP (∼40% as in Fig. 6) of the proposed layout compared with the baseline one. Thus, the proposed layout structure is recommended for CNFET SRAM cell despite its 25% area cost. The detailed comparisons between FinFET and CNFET SRAM cells are shown in Table II. The area of FinFET/CNFET SRAM cell is calculated by $H \cdot W$, as illustrated in Fig. 4. The $H$ is found to be $3Da+6Wa$ for both layouts while $W$ is 2.5 and 2 CGP (refer to Table I for detailed sizes) for the proposed and baseline layouts, respectively. The calculated baseline FinFET SRAM cell area is 0.0262 $\mu$m$^2$, which is identical with the results presented in [35] and [36] and similar to the result (0.029 $\mu$m$^2$)

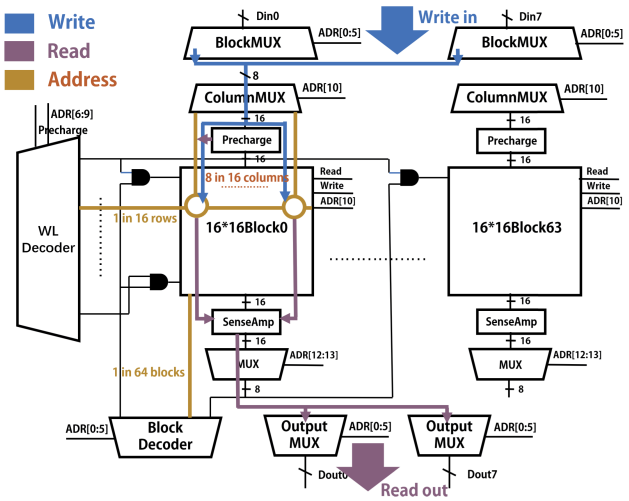



Fig. 8. 16 Kbit ACS array that can process 8-bit data in parallel. The red line illustrates the read path and the blue line represents the write path.

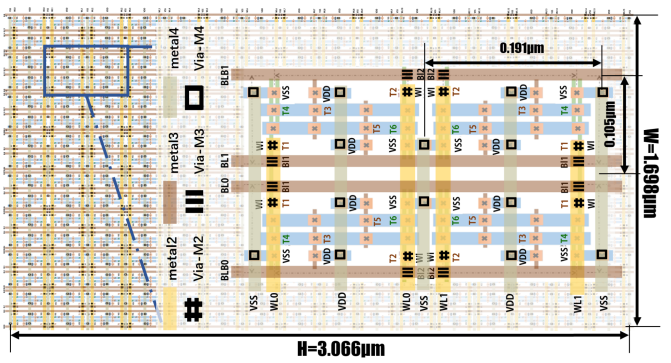



Fig. 9. Layout of 16 × 16 5-nm CNFET SRAM array. The interconnect segment lengths for the word and bitline can be calculated by the proposed 5-nm CNFET SRAM cell layout.

presented in [37] for the same number of fins for the pull-up, access, and pull-down transistors (1, 1, and 2, respectively) in the 7-nm SRAM cell. This confirms the accuracy of the SRAM cell area calculation method used in our work. Moreover, our computed FinFET read SNM is comparable to that simulated in [36] (0.183 V) with the same 7-nm process design kit (PDK) and size ratios. Comparing the proposed CNFET SRAM to the baseline FinFET SRAM cell, we find it has better results: read, write EDPs, static power, and area are 22.4%, 32.7%, 51.9%, and 76.7% of those of the FinFET SRAM cell respectively and meanwhile the read SNM and write SNM are about 6% and 12% larger, respectively.

## IV. All Carbon SRAM (ACS) Design

In this section, we will explore the benefits of carbon nanotube-based SRAM array called ACS. ACS is composed of the proposed CNFET SRAM cell described in Section III with MWCNTs as inter-cell interconnects, and also CNFET-based peripheral and control logic circuits. The ACS is compared with the 7-nm FinFET SRAM with Cu interconnects in terms of power consumption and performance.

### A. Description of Structure of SRAM Array

For system-level simulations, we constructed a 16 Kbit SRAM array as illustrated in Fig. 8. It consists of 64 memory blocks and associated peripheral and control logic circuits including address decoders, sense amplifiers, and I/O interface circuits. Each SRAM cell in the memory block can be represented as either FinFET SRAM or CNFET SRAM cell.

The read path of SRAM array consists of a sense amplifier, a column mux, an output selection mux, and a precharge circuit. During the read operation, the WL and BL/BLB decoders select one byte in the memory block, and the precharge circuit precharges BL/BLBs before read. When data are read to the BL/BLBs, the sense amplifier amplifies the data, and the output multiplexer selects 8 out of 16-bit data in one block to output. Write operation path consists of a block mux, a column mux, and a write driver. The block mux sends 8-bit data to a specific memory block, and the column mux is used to select which columns within the block the data are sent to by a write driver. Combined with the address decoder, data can be written successfully.

### B. ACS Array

The inter-cell interconnects in ACS array are represented by MWCNTs and we use compact models developed in [38] that include the impact of variability, contacts, and doping. It should be noted that MWCNT variabilities due to CNT diameter, chirality, and defects will greatly impact the performance of MWCNT interconnects and consequently the ACS array performance. Doping technique has been proposed and experimentally demonstrated to be an effective method to reduce these variabilities as [16], [17]. However, CNT variability analysis is beyond the scope of this article and they will be studied in our future work. For a fair comparison, the inter-cell CNT interconnect length is calculated in the same way as for Cu interconnects. We can obtain the length of the wordline or the BL/BLB based on the proposed CNFET SRAM cell layout structure, as illustrated in Fig. 9. Since the SRAM array has at most three interconnect layers, the CNT interconnect sizes shown in Table I and Fig. 1 can be applied for inter-cell interconnect design in the ACS array.

### C. FinFET SRAM Array

Similar to the ACS array in Fig. 9, we construct a reference case with 7-nm FinFET SRAM cells with Cu inter-cell interconnects. Copper interconnects are represented by the RC model as in [39] where inductance is ignored. Inter-cell interconnects between neighboring cells (including BL/BLBs and WLs) are modeled as a $\pi$-model. We obtain the inter-cell Cu interconnect lengths according to the 7-nm FinFET SRAM layout and the geometric size of Cu interconnect shown in Table I and Fig. 1. Then, the parasitic resistance and capacitance of Cu interconnects can be estimated as in [33] and [26], respectively.

## V. ACS Simulation Results

A 16 Kbit (8-bit per word) ACS memory array is constructed for the array-level evaluation. However, to accelerate

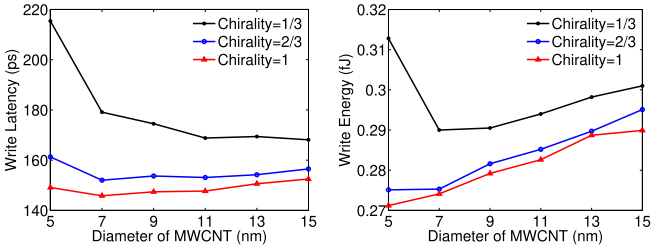



Fig. 10. Impact of CNT outer diameter (with no doping) on ACS write latency and energy. (a) Write latency. (b) Write energy.

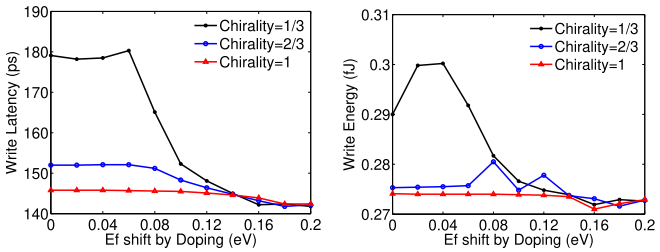



Fig. 11. Impact of CNT doping ($D_{\max} = 7$ nm) on the ACS write latency and energy. (a) Write latency. (b) Write energy.

the simulation without losing generality, we take one memory block (16 × 16) as a representative for both the FinFET and ACS studies. Furthermore, to obtain the worst case or largest latency of the read and write operations, we simulate the SRAM cells located on the array corner (corresponding to the largest latency). However, it should be noted that the read/write latency and energy simulations consider the impact and contribution of the peripheral circuits including the WL decoder, pre-charge circuit, sense amplifier, write driver, and the multiplexer (identical circuit structures designed with CNFET and FinFET respectively for the CNFET and FinFET SRAM arrays). We first investigate the impact of interconnect parameters on the performance and energy efficiency of the ACS SRAM. Then, we derive the optimal configurations for inter-cell CNT interconnects. Lastly, we compare the ACS design with the FinFET reference design to illustrate the benefits and costs of ACS design. It should be noted that the leakage power consumption comparisons between ACS and FinFET counterpart in the array-level study are expected to be similar to those in cell-level as we assume that both SRAM arrays are of the same capacity, i.e., the same number of cells which is much larger than the peripheral and control logic circuit. Hence, the leakage power consumption in the array level is not further compared or discussed.

### *A. Impacts of Inter-Cell MWCNT Diameter, Chirality and Doping*

Read and write operations activate different paths of the SRAM cell circuit, so they may have different dependencies on inter-cell interconnect parameters. Hence, we investigate and optimize ACS array for the read and write operations sequentially. We investigate CNT interconnect diameter, chirality, and doping level to evaluate their impacts on the ACS array read and write power efficiency and performance. CNT interconnect outer diameter is varied from 5 to 15 nm. It is important to note that MWCNTs with Pd-CNT end-contact [16] are considered for inter-cell interconnects in the ACS array.

For the write operation, we observe that both latency and energy decrease and then increase with MWCNT diameter, as shown in Fig. 10. The increase in MWCNT diameter leads to an increase in interconnect capacitance and a reduction in resistance (both CNT intrinsic and contact resistance), which is inversely dependent on the CNT diameter. We deduce that $D_{\max} = 7$ nm is a good choice for MWCNT outer diameter to trade-off performance and energy consumption.

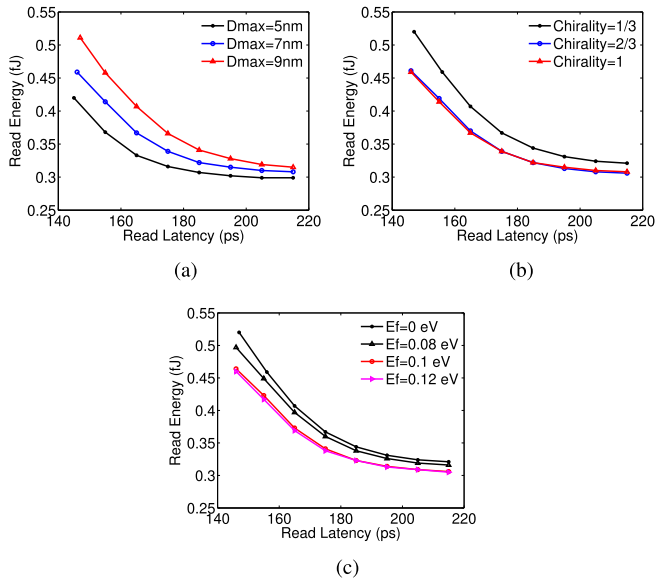



Fig. 12. Impact of (a) CNT outer diameter, $D_{\max}$ (with chirality = 1 and no doping), (b) chirality (with $D_{\max} = 7$ nm and no doping), and (c) doping (with $D_{\max} = 7$ nm and chirality = 1/3) on the ACS read latency and energy.

Chirality is another important parameter that determines the metallic or semiconducting behavior of CNTs, hence its parasitics resistance and capacitance. Studies have shown that once CNTs are grown, they have an average chirality of 1/3 metallic [40]. To control chirality and convert semiconducting CNTs to have metallic-like electrical properties for interconnect applications, charge-based doping has been effectively demonstrated by [41]. Here, we investigate doping of CNT interconnects by varying the Fermi shift level, $E_f$ to represent the change on CNT interconnects from semiconducting to metallic-like electrical properties. It was shown by [16] that doping level of $E_f = 0.1$ eV changes chirality to 2/3 metallic and $E_f \geq 0.12$ eV achieves chirality 1. We investigate these different CNT chiralities and their impact on performance and energy as in Fig. 11.

Different from the write latency which can be defined as the difference between write enable signal and the successful data flip inside the SRAM cell, the latency of the read operation is dependent on the trigger of the sense amplifier. Hence, instead of showing the latency results as a function of different CNT interconnect parameters, we show the read energy versus read latency as they are closely related. Results are shown in Fig. 12.

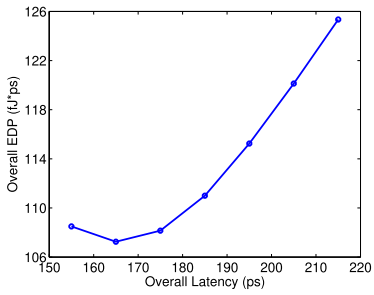



Fig. 13. Write and read overall EDP calculations for the ACS array at various overall latency.

TABLE III

COMPARISONS BETWEEN FINFET SRAM ARRAY WITH Cu INTERCONNECTS, ACS ARRAY AND CNFET + Cu INTERCONNECTS (ALL 16 × 16 CAPACITY). THE BRACKET RESULTS ARE RESPECTIVE METRICS NORMALIZED TO THE FINFET + Cu COUNTERPARTS

| | FinFET+Cu | ACS(NM) | CNFET+Cu(NM) |
|---|---|---|---|
| Read Latency (ps) | 119.8 | 165.0(1.38) | 179.5(1.49) |
| Read Energy (aJ) | 1210.0 | 373.0(0.31) | 903.4(0.75) |
| Write Latency (ps) | 119.8 | 152.3(1.27) | 179.6(1.50) |
| Write Energy (aJ) | 1970.0 | 276.6(0.14) | 1295(0.66) |
| Overall Latency (ps) | 119.8 | 165.0(1.38) | 179.6(1.5) |
| Summed Energy (aJ) | 3180 | 649.6(0.20) | 2198.4(0.69) |
| Overall EDP (fJ·ps) | 381.0 | 107.2(0.28) | 394.8(1.04) |
| Array core area ($\mu m^2$) | 6.72 | 5.08(0.76) | 5.08(0.76) |
| MWCNT inter-cell interconnect physical parameters | | | |
| $D_{max}$=7 nm, chirality=0.333, $E_f$=0.1 eV | | | |

In the read operation, there is a trade-off between read latency and energy. We observe that there is less energy consumed with small CNT diameters for the same read latency as in Fig. 12(a). Thus, the CNT diameter of 7 nm is a good choice for both read and write operations. As for chirality, we observe that CNT interconnects with 1/3 chirality have significant larger energy consumption than interconnects with chirality 2/3 or 1 as in Fig. 12(b). However, similar to the write operation, doping can significantly improve read energy after doping of $E_f = 0.1$ eV, as shown in Fig. 12(c).

To assess overall ACS array performance and power efficiency, we evaluate the EDP metric. Because the overall latency or delay of ACS array depends on the largest values of read and write latency, the overall EDP can be calculated by the larger latency from either write or read operation and multiplied by the sum of write and read energy. Because write latency is fixed, the optimization of overall EDP is thus dependent on the selection of the read latency, as shown in Fig. 13. The minimum overall EDP is found to be of 107.2 (fJ · ps) at the latency of 165 ps. Based on the above analysis, we derive the optimal CNT inter-cell interconnect parameters for the ACS array as listed in Table III. Next, we will compare the proposed ACS array design with FinFET SRAM array with Cu inter-cell interconnects in terms of performance and power efficiency.

### *B. Comparisons With the FinFET SRAM Baseline*

Similar to the EDP minimization process for the ACS array, the minimum EDP of the FinFET SRAM array is obtained and shown in Table III. It is important to state that to date there is no equivalent capacity of 7-nm FinFET SRAM array available in literature to compare our results on read and write performance. The available 7-nm SRAM array (with 122 cell size ratio) [37] is 8 KB, which is 250 times larger than the 7-nm SRAM array of 256-bit capacity evaluated in this article. In [37], the reported write and read energy are 0.25 and 0.23 pJ, respectively, or about 126 and 190 times larger, respectively than the our baseline FinFET, indicating the overall accuracy of the array-level energy evaluation in this article.

By comparison, the ACS has a significant advantage on energy consumption during both read and write operations, with only 0.31× and 0.14× of the FinFET counterpart. Despite relatively larger read and write latency for ACS, about 1.38× and 1.27× compared to the FinFET counterpart respectively, the overall EDP value of ACS array is much lower, with only 0.28× compared to the FinFET structure. Nevertheless, we should also note that this is based on the design configuration of a lower static power CNFET SRAM. If we target a high-performance SRAM design, by increasing the CNT diameter or/and number for CNFET, the drive strength of CNFET will be increased to a level where the CNFET SRAM is of better performance than the FinFET counterpart. Moreover, based on the single cell area from Table I, we can compute the array core area (by ignoring the peripheral and control logic circuit) of ACS and FinFET SRAM arrays which are also listed in Table III. We deduce that ACS core area is about 24% smaller than the FinFET counterpart. The normalized column in Table III highlights the overall benefits and costs of ACS array design over FinFET SRAM array. In addition, the CNFET + Cu interconnect combination has also been evaluated in the power and speed metrics as shown in Table III. Overall, it has larger latency and power consumption than the ACS counterpart. The main reason is that the CNFET has not strong enough driving capacity to drive the Cu interconnect which has much larger capacitance than the CNT interconnect, inducing both speed and energy efficiency degradation. However, it has some power efficiency advantage over the FinFET counterpart due to smaller parasitics in the devices despite even larger degradation in the performance metrics. Hence, the ACS among the different technology scenarios has the best power efficiency with slightly worse speed than the FinFET + Cu counterpart. There are some works that show the good noise margin and low power of 2D-FET SRAM such as $WSe_2$-based SRAM design [42]. However, the performance of the 2D-FET SRAM is around one order of magnitude smaller than the CNFET counterpart. This is due to the unsolved huge contact resistance existing in the 2D-FET as discussed in the introduction of part I of this article as well.

## VI. CONCLUSION

In this article, we devised an all carbon-based SRAM (ACS) array (16 Kbit) at 5-nm technology node which has significant power efficiency advantage than the 7-nm FinFET counterpart, with its overall EDP and static power about 0.28× and 0.52× respectively compared to the later despite some speed degradation, which is however acceptable particularly for future

ultralow power application of SRAM. Meanwhile, the core area of ACS array is 0.76× of the FinFET SRAM array with the same capacity and the read SNM and write SNM are about 6% and 12% larger respectively. Hence, overall, the proposed ACS array presents a possible feasible candidate for future high-performance and low-power SRAM design.

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