A frontend for magnetoresistive sensors with a 2.2 pA/√Hz low-noise current source

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***Abstract*—In this letter, we present an integrated readout chip for magnetoresistive (MR) sensors consisting of a readout chain that comprises a DC-coupled fully differential difference amplifier (FDDA) followed by a programmable gain amplifier (PGA), as well as a low-noise current biasing scheme for the MR sensor. The current bias scheme features a 10-bit digital-to-analog converter (DAC) to compensate for process variations of the MR sensing element as well as to calibrate for variations in the DC bias field of the sensor. The bias current source achieves a very low current noise floor of $2.2\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ for bias currents up to $1\,\mathrm{mA}$ showing a 5x improvement compared to prior arts. The readout chip is manufactured in $180\,\mathrm{nm}$ SOI CMOS and consumes a total power of $38\,\mathrm{mW}$. The paper is an extended version of [8], incorporating additional modeling details and measurement results.**

I. Introduction

Many emerging biosensing applications [1], [2] as well as human machine interfaces for augmented reality applications [3] rely on giant magnetoresistive (GMR) sensors due to their good sensitivity and low 1/f noise. As an alternative, tunnel magnetoresistive (TMR) sensors can provide superior sensitivity compared to GMR sensors due to their higher magnetoresistive (MR) ratios. However, such high MR ratios impose strict requirements on the interface electronics due to the large variations in their base resistance. Such variations lead to large voltage offsets at the amplifier input, reducing the dynamic range of the amplifier, and, in the worst case, saturating the frontend if uncompensated. A possible solution to eliminate the input DC offset of the amplifier is to use a chopped capacitively-coupled instrumentation amplifier (CCIA) in combination with a DC servo loop (DSL) [4], cf. Fig. 1a. However, this approach presents a tradeoff between the input-referred voltage noise of the amplifier and the maximum offset that the DSL can compensate. More specifically, a higher input offset can be compensated by increasing C_{DSL}, which, in turn, increases the input-referred voltage noise of the CCIA [5]. As an alternative, Fig. 1b shows the possibility of using a voltage bias across the MR element in combination with a transimpedance amplifier (TIA) to process the resulting current [2]. In this scheme, frequently, an auxiliary resistive

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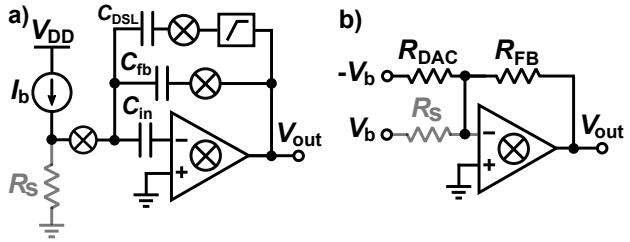

Fig. 1: Block diagram of a) a CCIA frontend with embedded DSL and b) a TIA readout with a resistive DAC.

DAC is added at the virtual ground node to source or sink the DC current generated by the base resistance and offsets. While this scheme is simple, it displays inferior linearity compared to a current bias with voltage readout since the change in resistance occurs in the denominator of the TIA output voltage [2]. Consequently, the linearity can be improved using a current bias followed by a voltage amplifier [1], [6]–[8]. In order to avoid the tradeoff between offset and noise as it occurs in the case of DSLs embedded inside CCIAs as well as the non-linearity problem associated with a voltage bias and TIA readout, in this paper, we implement the offset compensation prior to the amplification stage with an adjustable current biasing using a 10-bit binary-weighted current digital-to-analog converter (DAC) with a large dynamic range. A voltage-mode readout using a fully differential-difference amplifier (FDDA) followed by a programmable gain amplifier (PGA) amplifies the voltage signal at the sensor output, providing a spectrally purer readout compared to a current readout implementation. The presented design is optimized for TMR sensors but can also be used for different MR sensors. This letter, which is an extended version of [8], providing more modeling details and additional measurement results, is organized as follows: In section II, the architecture of the proposed chip is introduced. Section III presents the measurement results of the readout chip. The paper concludes with a summary in section IV.

II. Chip Description

Fig. 2 shows the block diagram of the presented readout ASIC, consisting of the current bias of the sensor and the subsequent voltage amplifiers, together with the chip micrograph [8]. An on-chip fixed current source and an adjustable current DAC bias the MR sensor and a reference resistor, respectively. This differential readout scheme improves the baseline-to-signal-ratio [7]. The compensation of the offset between the sensor and the reference resistor is achieved by continuously monitoring the difference between the MR and the reference resistor output voltages using a DC-coupled

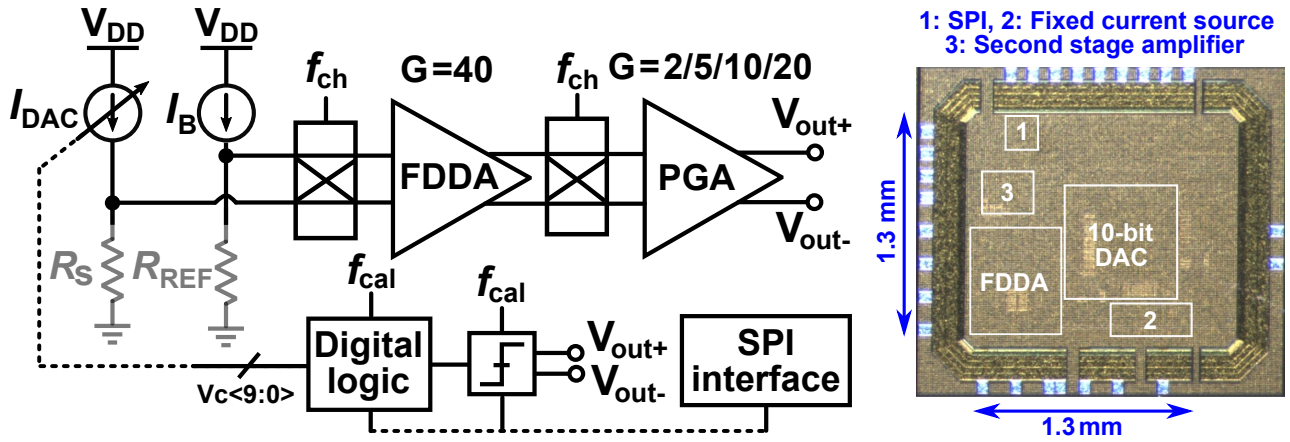

Fig. 2: a) System level block diagram of the readout chip. b) Chip micrograph.

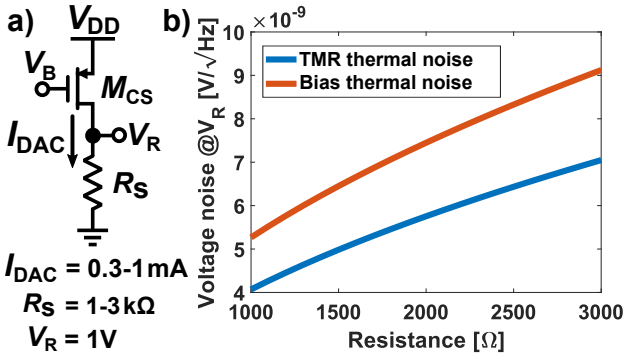

Fig. 3: a) A simple implementation of a PMOS current source biasing an MR sensor. b) Voltage noise at V_{R} due to the thermal noise of the TMR sensor and the current bias.

readout circuit formed by an FDDA and a PGA, which feeds a dynamic comparator followed by a digital logic that finds the DAC digital codeword necessary to compensate the offset. The automatic compensation routine is triggered via an on-chip SPI interface.

A. Sensor biasing

A simple implementation of a current bias of a resistor is shown in Fig 3a, where a PMOS transistor in saturation region is used to bias the MR sensor. To account for the large manufacturing tolerances of TMR resistors (1 kΩ up to 3 kΩ for the TMR used in [8]), I_{DAC} has to be adjustable. The voltage across the sensor V_{R} should be maximized for a given supply voltage, breakdown voltage of the utilized sensor and its passivation layer to optimize the SNR of the sensor [1]. Here, we target $V_{\mathrm{R}} = 1\,\mathrm{V}$ by making I_{DAC} adjustable between 0.3 mA and 1 mA. The voltage noise power spectral density (PSD) at V_{R}, ignoring flicker noise of the MR sensor, is given by:

$$\begin{aligned} S_{\Delta V^2_{\mathrm{R,OL}}} &= 4kTR_{\mathrm{s}} + S_{\Delta I^2_{\mathrm{nD,OL}}} \cdot R_{\mathrm{s}}^2, \\ S_{\Delta I^2_{\mathrm{nD,OL}}} &= 4kT\gamma g_{\mathrm{m}} + \frac{\mathrm{KF} \cdot g_{\mathrm{m}}^2}{C_{\mathrm{ox}} \cdot W \cdot L \cdot f}, \end{aligned} \tag{1}$$

where $S_{\Delta I^2_{\mathrm{nD,OL}}}$ is the current noise PSD of M_{CS}, k is the Boltzmann constant, T is absolute temperature, γ is the excess noise factor, g_{m} is the transconductance of transistor M_{CS}, KF is the flicker noise factor, C_{ox} is the oxide capacitance per unit area and W and L are the transistor width and length, respectively. The first summand of eq. (1) models the thermal noise of the MR sensor while the second and third summand model the thermal and flicker noise of the transistor M_{CS}. The voltage noise PSD can be lowered by biasing the transistor M_{CS} deeply in strong inversion, where $g_{\mathrm{m}} = 2 \cdot I_{\mathrm{DAC}}/V_{\mathrm{ds,sat}}$ and $V_{\mathrm{ds,sat}}$ is limited by the available voltage overhead of $V_{\mathrm{DD}} - V_{\mathrm{R}}$ and/or the onset of velocity saturation effects. For a supply voltage of 1.8 V and a voltage drop across the resistor of $V_{\mathrm{R}} = 1\,\mathrm{V}$, the maximum voltage headroom for the transistor is given by 0.8 V. Fig. 3b shows the thermal noise floor of both the MR sensor and the current source according to eq. (1) for $V_{\mathrm{DD}} = 1.8\,\mathrm{V}$, $V_{\mathrm{R}} = 1\,\mathrm{V}$ and the process parameters of the 180 nm CMOS process used for the chip implementation described in section III, as a function of the sensor resistance R_{s}. Clearly, the thermal noise floor of the current bias dominates the MR noise, and hence degrades the intrinsic SNR of the MR sensor. As a possible route to lowering the noise of the current source transistor M_{CS}, in this paper, we follow the idea of [1] and [6] of embedding the transistor M_{CS} into a feedback loop. However, in contrast to [1], [6], the feedback loop used in this work, cf. Fig. 4a, utilizes a TIA to reduce noise-induced fluctuations in the output current [8]. Importantly, the TIA architecture greatly reduces the influence of the opamp noise on the overall current noise compared to previously presented noise reduction loops [1], [6]. The TIA-based feedback loop works as follows. Overall, the feedback loop regulates the source-gate voltage v_{sg} of transistor M_{CS} with a high loop gain to reduce noise-induced fluctuations in the output current. The virtual short at the opamp input causes the source of transistor M_{CS} to be biased at V_{DD}. The bias current flows through the TIA feedback resistor R_{FB}, producing a proportional voltage at the TIA output, which counteracts fluctuations in the output current. To allow for adjusting the DC bias current using the on-chip generated bias voltage V_{B}, the TIA output is AC coupled to the gate of $\mathrm{M_{CS}}$, cf. Fig. 4a, effectively high pass filtering the TIA output with a very low cut-off frequency formed by capacitor $C_{\mathrm{AC}} = 20\,\mathrm{pF}$ and pseudo-resistor $R_{\mathrm{AC}} = 10\,\mathrm{G\Omega}$. Additionally, a reset switch is added to the gate of the transistor $\mathrm{M_{CS}}$ to reset this high impedance node

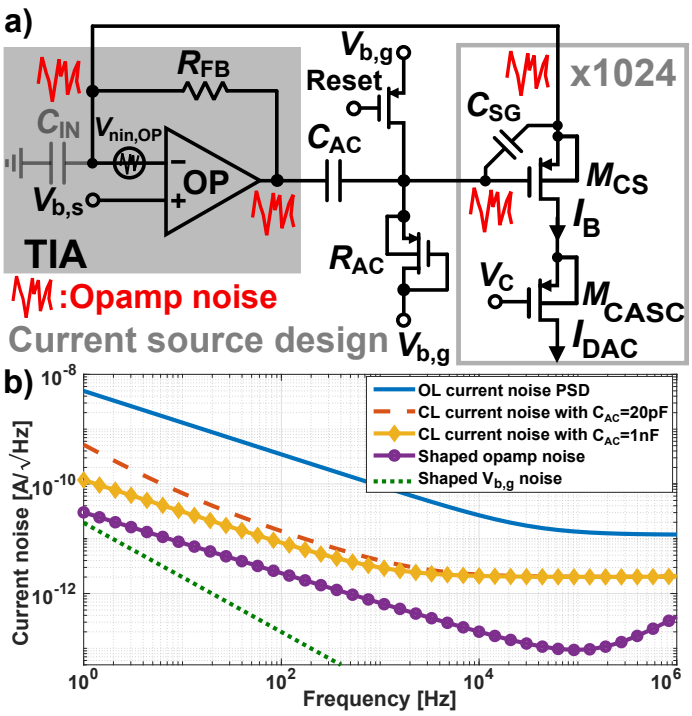

Fig. 4: a) Block diagram of the proposed current bias. b) Simulated current noise PSD of the current bias with and without the feedback loop.

if necessary. In [8], we provided a simplified noise analysis of the circuit of Fig. 4a that neglected second-order effects such as the voltage divider between C_{AC} and C_{SG} as well as the effect of the finite channel conductance g_{ds}, of transistor M_{CS}, on the overall noise performance. Here, we specifically account for these two effects, and the resulting output current noise PSD of the proposed current source is given by:

$$
\begin{aligned}
S_{\Delta I^2_{\mathrm{nD,CL}}} \approx & \frac{S_{\Delta I^2_{\mathrm{nD,OL}}}}{(1+g_{\mathrm{m}}R_{\mathrm{FB}}x_{\mathrm{div}})^2} + \frac{4kT}{R_{\mathrm{FB}}} \\
& + \left[S_{\Delta V^2_{\mathrm{nin,OP}}} + S_{\Delta V^2_{\mathrm{b,s}}}\right]\left[\frac{g_{\mathrm{ds}} - j\omega g_{\mathrm{m}} R_{\mathrm{FB}} C_{\mathrm{in}} x_{\mathrm{div}}}{1+g_{\mathrm{m}}R_{\mathrm{FB}}x_{\mathrm{div}}}\right]^2 \\
& + S_{\Delta V^2_{\mathrm{b,g}}}\left[\frac{g_{\mathrm{m}}}{1+j\omega R_{\mathrm{AC}}C_{\mathrm{AC}}\left(1+g_{\mathrm{m}}R_{\mathrm{FB}}\right)}\right]^2,
\end{aligned}
\tag{2}
$$

where $x_{\mathrm{div}} = C_{\mathrm{AC}}/\left(C_{\mathrm{AC}}+C_{\mathrm{SG}}\right)$ and C_{IN} is the opamp input capacitance. Here, it is important to point out that, in contrast to the open-loop case, increasing g_{m} improves the overall noise performance by increasing the loop gain, cf. eq. (1). Hence, the scheme of Fig. 4a favors an operation of transistor M_{CS} in weak inversion, drastically reducing the headroom requirements for the current source. Moreover, any noise originating in the opamp of the TIA is greatly suppressed by the feedback loop of Fig. 4a, cf. eq. (2). Intuitively, at low frequencies, the TIA provides a voltage gain of unity from its input-referred voltage noise to the TIA output voltage, i.e. the gate voltage of transistor M_{CS}. Moreover, the virtual short at the TIA input causes the source voltage of M_{CS} to also equal the TIA's input-referred voltage noise as depicted by the noise signals in Fig. 4a. Therefore, any noise originating in the TIA opamp does not change the source-gate voltage v_{sg} of transistor M_{CS} and, therefore, does not increase the output current noise. However, the finite output conductance, g_{ds}, of M_{CS} prevents a complete cancelation of the internal opamp and opamp bias voltage noise $V_{\mathrm{b,s}}$, even at DC. At higher frequencies, the voltage divider between R_{FB} and C_{in} further deteriorates the cancelation of the opamp internal and bias noise, producing a noise contribution that increases with 20 dB/dec. It is worth mentioning that the overall noise of the opamp is typically still negligible compared to the noise of M_{CS}, cf. Fig 4b. Importantly, according to eq. (2), for a proper noise reduction, the value of the AC coupling capacitor C_{AC} has to be chosen sufficiently larger than the gate source capacitance of M_{CS}, C_{sg}. The gate bias voltage, $V_{\mathrm{b,g}}$, is low-pass filtered with a very low corner frequency, rendering its noise contribution negligible. Fig. 4b shows the simulated current noise PSD for an output current of 1 mA and a TIA feedback resistor of $R_{\mathrm{FB}} = 4\,\mathrm{k\Omega}$. According to eq. (2), the open-loop current noise PSD of transistor M_{CS}, $S_{\Delta I^2_{\mathrm{nD,OL}}}$, is reduced by the loop gain $g_{\mathrm{m}}R_{\mathrm{FB}}x_{\mathrm{div}}$. The closed-loop noise floor is established by the current noise of the feedback resistor R_{FB}, cf. eq. (2), and given by $2\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ for the $4\,\mathrm{k\Omega}$ resistor used in the presented design. According to Fig. 4b, assuming a fairly large bias voltage noise of $S_{\Delta V_{\mathrm{b,g}}} = 100\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, for frequencies above 1 Hz, the resulting current noise is still negligible. Moreover, the shaped opamp, assuming an input-referred opamp noise of $80\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, is also negligible compared to the closed-loop noise of M_{CS} up to frequencies beyond 1 MHz.

B. Amplifier implementation

According to Fig. 2a, the low-noise bias current I_{DAC} flows through the TMR sensor and produces a voltage signal which is subsequently amplified by a fully differential-difference amplifier (FDDA) followed by a programmable gain amplifier (PGA). In the presented design, the FDDA has a fixed gain of 40 and the PGA features four different gain settings to accommodate different dynamic range requirements. In order to lower the power consumption of the FDDA while maintaining a good noise performance, the input differential pair is implemented using stacked PMOS and NMOS pairs [9]. Moreover, chopping switches are incorporated into the FDDA to suppress its flicker noise and offset.

III. Measurement Results

The chip is manufactured in $180\,\mathrm{nm}$ SOI CMOS and occupies an active area of $1.7\,\mathrm{mm}^2$. The presented readout chain consumes $10.4\,\mathrm{mW}$ from a $1.8\,\mathrm{V}$ supply while the entire chip, including the MR and reference resistor bias, consumes $38\,\mathrm{mW}$ from $3.6\,\mathrm{V}$ and $6.8\,\mathrm{V}$ supplies [8]. The measured input-referred noise of the readout electronics with and without chopping ($f_{\mathrm{ch}} = 60\,\mathrm{kHz}$) and with nominally identical ohmic resistors connected to the input is shown in Fig. 5. In both cases, the measured noise floor is $4\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. With enabled chopping, the 1/f-noise corner frequency improves from 10 kHz to 400 Hz. The residual flicker noise after chopping originates from the unchopped PGA, cf. Fig. 2a. To demonstrate the effectiveness of the presented biasing

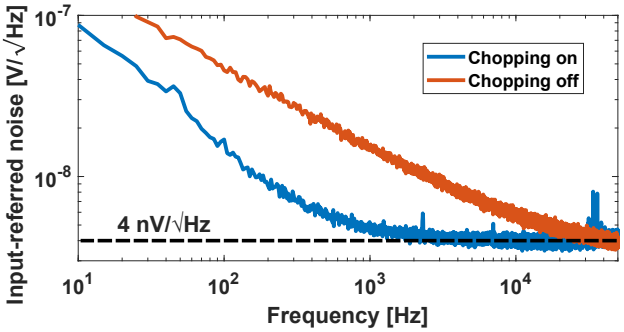

Fig. 5: Measured input-referred voltage noise PSD of the amplifier chain without and with chopping at 60 kHz.

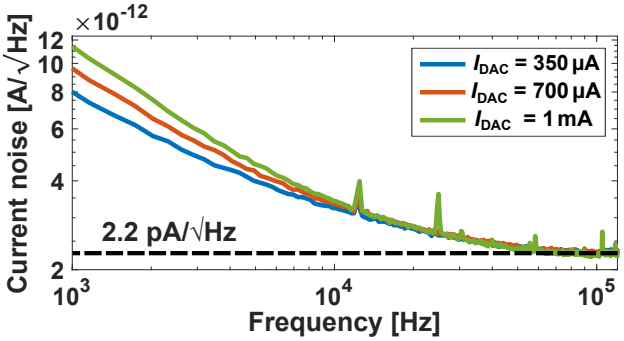

Fig. 6: Measured current noise PSD of I_{DAC} for different current settings.

scheme, Fig. 6 shows the measured closed-loop output noise of transistor M_{CS} for bias currents of $350\,\mu\mathrm{A}, 700\,\mu\mathrm{A}$ and $1\,\mathrm{mA}$. The measured noise floor is $2.2\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ with activated control loop and is defined by the feedback resistor R_{FB} for all current settings. A slight increase in the flicker noise is observed for higher currents due to the larger C_{SG} associated with a larger effective device area used for larger currents. Hence, the factor x_{div} is reduced for higher currents, and, as a result, the low-frequency noise is slightly increased, cf. eq. (2) and Fig. 4b. The measured current noise floor presents a 5x improvement compared to previous designs [1], [6]. The output characteristics of the current source for $I_{\mathrm{DAC}} = 500\,\mu\mathrm{A}$ and $I_{\mathrm{DAC}} = 1\,\mathrm{mA}$ is measured in Fig. 7. Despite the very-low noise operation of the designed current source, it can operate with a V_{SD} as low as $0.3\,\mathrm{V}$ for different I_{DAC}. Table I compares this work to the state-of-the-art in MR frontends with current biasing as well as a commercial adjustable very low-noise current source [10].

IV. Conclusion

In this letter, we have presented a combined bias and readout chip for MR sensors. The current bias achieves a state-of-the-art noise floor of $2.2\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$ for currents up to $1\,\mathrm{mA}$. Its large bias range accommodates the high process variations of TMR sensors. Moreover, the proposed current bias can provide a very low noise floor while operating at a large $g_{\mathrm{m}}/I_{\mathrm{D}}$, i.e. low $V_{\mathrm{ds,sat}}$. The included programmable readout chain including chopping displays a low noise floor of $4\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ together with a low 1/f-noise corner of 400 Hz, rendering the overall MR frontend a very versatile and high-performance platform for next-generation MR sensing systems.

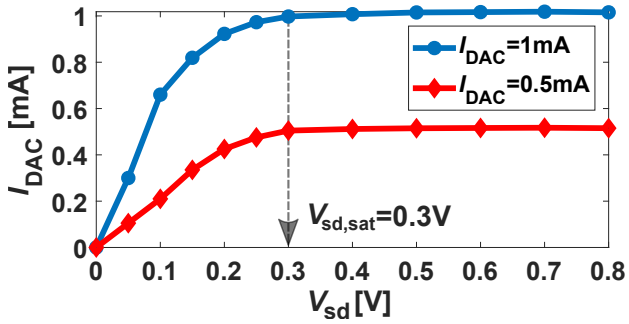

Fig. 7: Measured output characteristics of I_{DAC} for different current settings.

TABLE I: Comparison against the state-of-the-art.

	LM134 TI [10]	Costa TBCAS'17	Zhou JSSC'21	**This work**
Current bias	up to 10 mA	0.5 mA	–	**up to 1 mA**
Bias noise floor [pA/√Hz]	100$^{\alpha}$	10	≈10$^{\gamma}$	**2.2**
Power [mW]	–	4.9*	2.5*	**10.4*§/38**
Area [mm^2]	–	3.17	1.92	**1.7**
Min. V_{ds} [V]	0.85$^{\alpha}$	–	–	**0.3**
Process [µm]	–	0.35	0.18	**0.18**

*Power excludes the current bias. $^{\gamma}$Calculated from figures and text.
§Power measured while switching off the sensor bias. $^{\alpha}$For 1 mA current.

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