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Ultra-thin ISFET-based sensing systems

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Abstract

The ion-sensitive field effect transistors (ISFETs), proposed little over 50 years ago, today make the most promising devices for lab-on-a-chip, implantable, and point-of-care (POC) diagnostics. Their compatibility with CMOS (Complementary Metal Oxide Semiconductor) technology and the low cost through mass production have been the driving factors so far. Nowadays, they are also being developed in flexible form factors for new applications such as wearables and to improve the effective usage in existing applications such as implantable systems. In this regard, the CMOS ultra-thin chip (UTC) technology and the bonding by printing are the noteworthy advances. This paper comprehensively reviews such new developments in the CMOS-compatible ISFETs, along with their theory, readout circuitries, circuit-based techniques for compensation of the ISFET's instabilities, such as the offset, flicker noise, and drift. The sensing mechanisms and the properties of interface between the electrolyte under test and the metal-oxide based ion-sensitive electrodes have been discussed along with a brief overview of the metal-oxide based pH sensors. An overview of the reported mechanically flexible pH sensors, including ISFETs, is provided and the history of ISFET applications are also covered. Finally, established models that can be used to design flexible circuits are presented, and possible opportunities to use circuit techniques to compensate for mechanical deformation are discussed.

KEYWORDS
CMOS, flexible electronics, ISFET, potentiometric sensors, read-out, ultra-thin chips

1 | INTRODUCTION

Field-effect transistor (FET) based solid state sensors have attracted considerable attention since late 1960s, that is, immediately after the introduction of standard silicon planar technology for integrated circuits (IC). They offer excellent response to a wide variety of stimuli, small size, and easy on-chip integration and, as a result, underpin the development of miniaturized systems that can be interfaced with computers to enable remote monitoring of desired parameters (health, environment, etc.).[1] They encompass a wide realm of sensing technologies in everyday use including the chemical sensors (e.g., gas and biosensors),[2] physical sensors (e.g., strain, pressure, temperature),[3,4] acoustic sensors (e.g., bulk and surface acoustic wave devices),[5] optical sensors (e.g., optical waveguide, infra-red detectors),[6] thermochemistry (e.g., micro-calorie and micro-enthalpy sensors),[7] and

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magnetic sensors.[8] The field of tactile or touch sensing too benefited from this approach and early touch sensors based on semiconducting devices have been reported.[9]

Among this wide variety of solid-state sensors, the one type that clearly stands out is the Ion-Sensitive Field Effect Transistor (ISFETs), which have played a major role in enabling the fully integrated complementary metal-oxide semiconductor (CMOS)-based chemical sensing systems. They are commonly used for the detection of pH that is needed in a plethora of applications consisting of, but not limited to, tissue health monitoring,[10] cancer detection,[11,12] soil and water content analysis,[13,14] DNA detection and amplification,[15,16] food processing and preservation,[17] and bacterial and yeast growth identification.[18,19] They can also be modified or functionalized for potentiometric biochemical sensing of inorganic ions and biomolecules such as K^+, Na^+, Pb^{2+}, Mg^{2+}, Ca^{2+}, Cl^-, NO_3^-, SO_4^{2-}, nucleic acids, proteins, and carbohydrates[20–25] of which the label-free detection is inevitable for gauging electrolyte balance and individual cell health. With the advancement of CMOS technology, bulky passive pH sensors such as glass probes are being replaced by their miniaturized active ISFET counterparts that can be developed on semiconducting substrates. They enable the development of System-on-Chip architectures with integrated signal conditioning circuits, read-out topologies, digitization, and wireless modules.[26] This paves the way for the development of Point-of-Care (PoC) devices and diagnostic tools deployable in resource-deprived areas as well as for in-vivo modules capable of being affixed to tissues, blood vessels, and even cells.[24,27] They also provide the opportunity for the fabrication of large-scale chemical sensing arrays. In this regard, the utilization of high-density ion-sensitive transistors for non-optical genome sequencing presents an important step in the development of next-generation sequencing platforms.[28] The basis of the ISFET as a hydrogen ion sensor is efficiently exploited towards DNA sequencing reactions wherein protons are generated during nucleotide incorporation.[28]

With reference to electrochemical sensing, CMOS microelectrode arrays (MEA) have also gained traction due to their high-density realization for recording neuronal membrane potentials as well as providing electrical stimuli to surrounding cells on the MEA that is critical toward in vitro analysis of neural networks as well as biomimicry.[29] While ISFETs are largely non-faradaic devices consisting of dielectric sensing membranes, MEAs consist of polarizable electrodes capable of both faradaic and non-faradaic processes. With the advancement of fabrication processes, three-electrode measurements comprising of on-chip working, counter and reference electrodes have been developed with subsequent signal conditioning modules on the same substrate with potential expansion towards two-electrode systems such as ISFETs.[30–33] This facilitates efficient electrode placement of the sensing and reference electrodes toward on-chip measurement of open circuit potential indicative of the pH of the media under test as well as its electrochemical stability. Furthermore, the electro-biological response of high-density interconnected neurons has recently been obtained via modified CMOS chips with Platinum electrodes.[34]

With increasing technology miniaturization, the development of sensitive and conformal devices has gained momentum. With regards to ISFETs, this entails the presence of flexible sensing, transducing, referencing, and signal-conditioning units. Currently available review papers highlight the evolution of ISFETs and their read-out methodologies over the past decades.[35–37] In this short review, we present the evolution of ISFETs in terms of the device structure, materials, and advances such as physical flexibility. Additionally, ultra-thin chip technology has been introduced in the context of ISFETs and an overview of the available instrumentation techniques is presented. The remainder of the paper is organized as follows. Section 2 highlights the evolution of ISFETs in the context of previously published research and the growing importance associated with flexible ISFETs. The development of non-rigid ISFETs is presented in Section 3 constituting of devices wherein one or more segments of the device is flexible. This section also introduces the domain of chip thinning that has gained paramount significance toward the development of foundry-fabricated CMOS ISFETs incorporated with on-chip read-out topologies. The read-out topologies are presented in Section 4 where the challenges and opportunities are discussed and a summary of key points is presented in Section 5.

2 | EVOLUTION OF ISFETS

2.1 | Historical perspective

In its essence, ion-sensitive FETs consist of architectures that closely mimic MOSFETs wherein the metallic/poly-Si gate is replaced by an ion-sensitive membrane. The classic ISFET architecture was first proposed in the 1970s and is composed of a single-gate detector-transducer integrated into the same structure for pH detection.[38] A systemic study of trends in published research on Web of Science pertaining to ISFETs and their flexible counterparts since their inception is shown in Figure 1. Additionally, trends associated with flexible pH sensors comprising of transistor structures as well as thin films and microstructures are included. It must be noted that research on flexible

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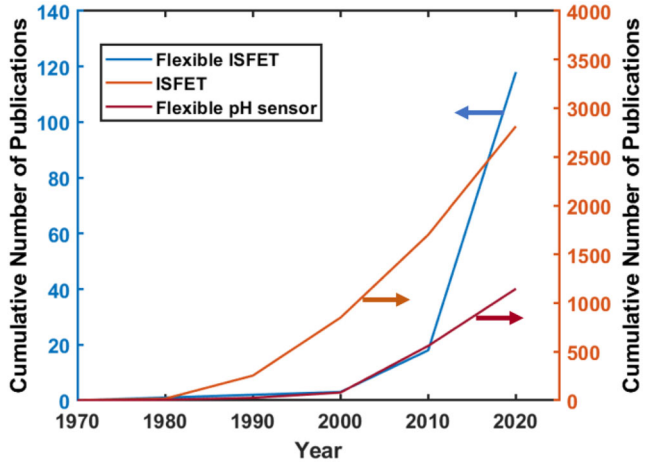

FIGURE 1 Cumulative number of publications in the domain of ISFETs and flexible pH sensing (arrows denote respective y-axis)

ISFETs often comprises hybrid devices wherein one or more aspects of the device are flexible.

The domain of flexible ISFETs is currently in its nascent stages accounting for ~10% of flexible pH sensors. Furthermore, analysis of literature from 1970 in the area of flexible ISFETs highlights that chip thinning as a technique for the integration of ISFET CMOS dies on flexible and curvilinear substrates is a very recent approach explored by a limited number of researchers wherein etching of high-cost Silicon-on-Oxide (SOI) wafers remains the primary technique for obtaining ultra-thin bodied FETs.[39,40] Reviews pertaining to the development of all-flexible ISFETs comprising bendable sensing, transducing, and read-out topologies have not been reported yet and this article accomplishes to fill this gap in the literature. Additionally, the development of non-traditional ISFETs in terms of structure and materials is presented as the next generation of ISFETs. In this minireview, we focus on the current trends attributed to the development of flexible and conformable ISFETs in terms of technology, material, response as well as their capability to be monolithically integrated with on-chip electronics. It must be noted that in this context an ISFET refers to an active device capable of sensing pH. Modified chemically sensitive transistors, often called ChemFETs or BioFETs, constitute a separate category of sensors of which the fabrication process and requirements differ from that of ISFETs.[41]

2.2 | Next-generation ISFETs

The conventional ISFET device consists of an ion-sensitive material as the dielectric layer of the FET of which the variation in the surface potential is observed as a change in the output voltage or current of the device, biased via a reference electrode. Dielectric stacks composed of materials with a high electric permittivity as well as surface binding sites are a popular choice of materials for developing ISFETs of which the response is near-Nernstian under a wide range of pH values that also mitigate capacitive division in the device. The sensitivity of transistors based on the single-gated traditional structure exhibits a maximum value of ~59.6 mV/pH due to the theoretical Nernstian limit.[42] In this regard, novel architectures as well as materials have been proposed to further exceed the sensitivity of the devices while also improving their downscaling abilities without affecting effective carrier mobility, capacitive coupling, cross-sensitivity, and material degradation. For example, dual-gate (DG), triple-gate (TG), and extended-gate (EG) ISFET architectures have been developed that increase the capacitive coupling to the gate leading to self-amplification within the device and can exhibit intrinsic sensitivities above 1 V/pH.[42–46] From a material perspective, traditional single-layer metal oxides and nitrides such as SiO_2, Al_2O_3, Si_3N_4 are being replaced by individual or stacked high-k dielectrics such as SiO_2/Ta_2O_5, HfO_2, and RuO_2/SnO_2 that aid in increasing the sensitivity of the device and a complete review on metal-oxide based pH sensors can be found in the work of Manjakkal et al.[47] Furthermore, the low-frequency noise developed in ISFETs due to charge trapping and de-trapping in the oxide layer of the transducer FET can be mitigated by adopting the MESFET (Metal-Semiconductor FET) architecture wherein the oxide layer is removed and a Schottky Junction (SJ) is formed and the detector unit comprising of the sensing oxide is fabricated as an extended gate structure.[48]

The design of glass-substrate-based ISFETs inspired by thin-film technology has also been explored and an example is based on a 6 nm thick Ta_2O_5 dielectric and a ZnO channel, exhibiting a sensitivity of ~55 mV/pH.[49] Improvements in device stability have been made by utilizing atomic layer deposition (ALD) of Al_2O_3 with a thickness of 20 nm on a silicon substrate capable of integration with CMOS processing.[50] The sensitivity of the devices post-annealing exhibited a strong correlation to the annealing temperature (58.8 mV/pH at 500°C versus 52.6 mV/pH at 900°C) that occurred due to variations in film quality with temperature.[50] The strong dependency of the transistor's response to porosity and crystallinity of the dielectric material manifests as a non-ideal behavior in the ISFET called drift that is characterized by a slow and monotonic variation in the output voltage under no external variations or disturbances. This occurs primarily due to the ultra-slow diffusion of electrolytic ions through the bulk of the dielectric due to buried sites as well as physio-chemical modification of the dielectric layer due to mass transfer limited reactions.[51] Research directed

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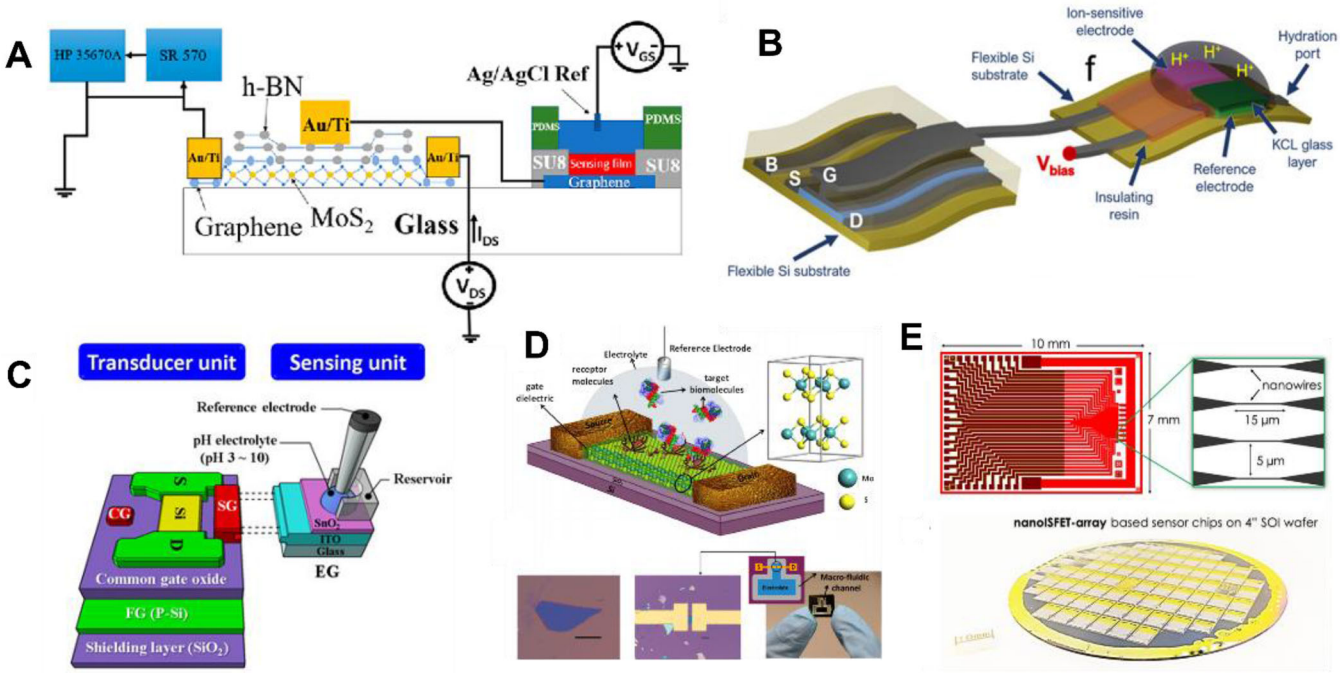

FIGURE 2 Schematics of ISFETs for accurate pH measurements. (a) Extended gate ISFET on glass with Al_2O_3-hBN sensing stack and MoS_2 channel. Adapted with permission from Ref. [42]. Copyright 2020, American Chemical Society, (b) Ultra-thin extended gate ISFET with RuO_2 sensing membrane. Adapted with permission from Ref. [54]. Copyright 2020, American Chemical Society, (c) Coplanar dual-gated ISFET structure with tin oxide sensing layer. Adapted with permission from Ref. [45]. Copyright 2020, American Chemical Society, (d) Dielectric encapsulated MoS_2 based ISFET with biosensing capabilities. Adapted with permission from Ref. [57]. Copyright 2014, American Chemical Society, (d) Wafer-level fabrication of SOI-based SiNW-ISFET capable of antigen detection. Adapted with permission from Ref. [58]. Copyright 2016, American Chemical Society

toward reduction of drift has been carried out via fabrication of novel materials and topologies as replacements to classic metal-oxide architectures, development of electrical read-out techniques as well as machine learning algorithms.[42,52,53] For example, EG-ISFETs comprising of a stacked Al_2O_3/h-BN (hexagonal boron nitride) as the sensing layer in the detector unit coupled with a MoS_2 channel FET with graphene contacts as the transducer unit have been developed and exhibit a drift of ~2.5 mV/h and a sensitivity of 54 mV/pH as shown in Figure 2a.[42] Recently, we have demonstrated the use of a RuO_2-based ISFET fabricated on an ultra-thin Si chip wherein the intrinsic piezoresistivity of bent Si is utilized to compensate for drift of which the structure is shown in Figure 2b.[54]

In order to cross the theoretical Nernstian limit, the electrostatic control of the gate (s) must be improved. For instance, multi-gated CMOS compatible thin-film ISFETs comprising of three gates exhibit sensitivities of ~467 mV/pH and ~57 mV/pH for the dual-gated and single-gated structures, respectively.[46] The device sensitivity was measured to be ~1283 mV/pH for the triple-gated structure as opposed to. Similarly, EG-ISFETs fabricated on glass with a sensitivity of 304.12 mV/pH, consisting of a floating gate and a silicon channel have been developed and shown in Figure 2c.[45] Low power devices that utilize the inherent double-layer capacitive coupling, constructed using electrolyte-gated structures, have eliminated the need for fabrication of individual high-k dielectrics as sensing layers. These devices are often developed using thin-film technology processes with zinc oxide-derived materials as channels in contact with or electrically coupled to the solution under test.[55,56]

The minimum detectable concentration of the ISFET has gained increased importance as a figure of merit particularly in the domain of label-free biosensing, wherein detection in the sub-ppm level is often necessary, usually following surface functionalization. This is further advanced by the downscaling needs associated with developing miniaturized point of care devices as well as implantable microsystems while utilizing voltages within the potential window of target electrolytes. Hence, 2D and 1D nanomaterials have gained momentum in the fabrication of ultra-sensitive devices with a high surface area-to-volume ratio, fast response time and capability to be integrated with bendable substrates. In this regard, dual pH-protein sensors based on a MoS_2 channel device only 2–5 nm thick have been fabricated via exfoliation and encapsulation with a functionalized dielectric capable of

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detecting sub-picolitre target molecules as shown in Figure 2d.[57] Silicon nanowire-based ISFETs (SiNW-ISFET) for detection of prostate-specific antigen (PSA) levels via aptamer-based functionalization of the nanowires have also been reported.[59] Arrayed SiNW-ISFETs-on-a-chip, portrayed in Figure 2e, was developed as an extension on an SOI wafer through nanoimprint lithography which was subsequently wire-bonded to a PCB for electrical read-out.[58] The development of ISFETs and their associated read-out modules with mechanical flexibility has gained momentum due to the growing need for carrying out non-invasive as well as continuous measurements of physiological parameters. Hence, conformable and wearable systems that can be integrated with soft and/or curvilinear surfaces, such as biological tissues are vital toward improving the quality of life of patients and extending the reach of technology to remote areas via on-chip data transmission capabilities.[60–62]

3 | FLEXIBLE ISFETS

Flexible ISFETs can provide additional advantages in the field of consumer or industrial applications permitting, for example, the continuous quality monitoring of packages food or the unsupervised operation of heavy machinery in unpredictable environments among humans, obstacles, or in underwater or space environments.[63] One of the major advantages of wearable/epidermal electronics fabricated in thin and conformable form factors is that they allow natural and intimate contact with the soft and curvilinear surfaces, such as the human skin, thus ensuring robust physical and electro-physiological measurements.[64] Additionally, the determination of pH in sweat is a parameter that can reflect metabolic activity or indicate the body's exercise intensity and dehydration level as well as targeted tissue ischemia. The flexibility of ISFETs is improved by replacing the sensing unit with materials fabricated on polymeric or soft substrates some of which are discussed in the next section. In order to achieve fully-flexible ISFETs, the transducing unit composed of the FET must also be made flexible and is often considered as the limiting factor and technologies that circumvent this issue and enable the fabrication of bendable CMOS ISFETs. The substrate material choice is currently dominated by silicon due to its ability to be integrated with CMOS micro-nano fabrication procedures as well as its appropriate electronic properties in terms of carrier mobility that aid in efficient detection of ions and fast response time.

Device performance and sensitivity is an intricate function of sensing membrane binding site density, trapped charges, channel material, as well as the sensing architecture utilized. However, the real-time application of ISFETs in conformal, flexible, and stretchable electronics is limited due to their rigidity often dominated by the stiff mechanical nature of the substrate. Efforts have been made to push the field of wearables a step closer to sensing microsystems that can seamlessly comply with the curvilinear geometry of human tissue by fabricating ISFETs on mechanically flexible substrates such as polyamide, polyethylene terephthalate (PET), and polyethylene naphthalate (PEN) often utilizing thin-film transistor (TFT) fabrication processes.[65]

Efficient fabrication of high-performance ion-sensitive FETs on flexible substrates is often impeded by the high-temperature processes involved in the deposition of high-quality dielectrics and sensing membranes. Furthermore, the transduction of the obtained chemical signals to electrical signals requires transistors with improved electrostatic control that are often fabricated on rigid substrates. In this regard, alternative materials with flex-rigid as well as flexible structures have been explored to fabricate electrochemical transistors based on organic, amorphous conductive oxides, carbon nanotubes, semiconducting materials, and polycrystalline silicon with extended or electrolytic gating of which some are highlighted in Table 1.

Flexible ISFETs based on a-IGZO (amorphous Indium Gallium Zinc Oxide) acting as both the electrolytic sensing gate as well as the channel on a PET substrate, exhibiting a sensitivity of 20 mV/pH with capabilities to also detect PSA levels via functionalization with amine groups, have been developed.[66] Furthermore, a dual temperature-pH sensor using a thin-film of a-IGZO fabricated on a PET substrate as the channel has been fabricated via sputtering as shown in Figure 3A.[67] The utilization of a separate sensing membrane with a high binding site density leads to a near-Nernstian sensitivity of 51.2 mV/pH, at the cost of additional fabrication steps.[67] In order to address the challenge of incorporating a separate reference electrode into the system for accurate measurements, they hand-printed Ag/AgCl ink onto the substrate.[67] The use of a-IGZO in the fabrication of flexible ISFETs was further exploited toward the development of extended gate FETs using SnO_2 sensing membrane, high-k gate dielectric stack composed of SiO_2/Ta_2O_5, an in-plane ITO (Indium Tin Oxide) gate, a floating bottom gate, and an a-IGZO channel in conjunction for in-device amplification leading to a maximum sensitivity of 2364 mV/pH as can be seen in Figure 3b.[68] Toward developing a completely flexible device wherein all the sub-structures consisting of the reference electrode as well as sensing and transducing units are flexible, an electrolytic gated transistor has been fabricated with a sensitivity of 19.4 mV/pH on a PET substrate as shown in Figure 3c.[69] Herein, two channels are composed of graphene, wherein one channel acts as the reference electrode.[69] This biasing channel is not

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TABLE 1 Summary of flexible ISFETs and their sensitivities

Ion Sensitive Material (ISM)	ISM Fabrication	Substrate Material	Substrate Thickness	Sensitivity	Detected pH range	Reference
ITO	Sputtering	PEN	125 μm	72 nA/pH	4-10	[65]
Carboxylic group functionalized SWCNT and PDDA stack	Layer by layer self-assembly	PET	250 μm	25 μA/pH	5-9 (also sensitive to glucose)	[82]
Oxygenated Graphene	Oxygen Plasma treatment of commercial graphene-PET substrate	PET		19.4 mV/pH	4-10	[69]
Amorphous IGZO	Sputtering	PET	175 μm	22 mV/pH	4-9	[66]
SnO_2	Magnetron Sputtering	Cellulose Paper	~ 100 μm	55.97 mV/pH (Single Gate) 1199.22 mV/pH (Dual Gate)	4-10 (EG-FET structure with rigid FET)	[83]
SnO_2	Magnetron Sputtering	PEN	125 μm	56 mV/pH (Single Gate) 1039 mV/pH (Dual Gate) 2364 mV/pH (In-plane Gate)	3-10	[68]
PANI	Potentiodynamic Deposition	PET	–	66.5 mV/pH	2.8-10.2	[84]
n-SiO_2/IZO	Magnetron Sputtering	PET	–	105 mV/pH	4-10	[56]

encapsulated and is continually in contact with the solution as is the protocol for the development of Reference Electrode FETs (REFETs).[69] An interesting study in the application of electrolyte multi-gating in the domain of neuromorphic pH sensing was carried out wherein the devices exhibited a sensitivity of 105 mV/pH[56]. Nanogranular silicon dioxide was deposited at room temperature via chemical vapor deposition followed by a variable transconductance IZO-channel sputtering highlighted in Figure 3d.[56] Due to the variation of channel properties with pH, the output spiking characteristics differed thus mimicking neuronal responses.[56]

In the application of sweat-sensing, fabrication of organic electrochemical transistors (OECT) on a PET substrate with a conducting dye-loaded PEDOT channel has been carried out.[70] These devices exhibit a sensitivity of ~93 mV/pH within the biological pH range.[70] Drawing inspiration from the operation of charged couple devices, dual temperature-pH ISFETs on a PET film has been carried out with a sensitivity of 240 mV/pH and enhanced responsiveness to temperature variations.[71] The pH sensing module was constructed using a-IGZO channel underneath an Al_2O_3/SiO_2 dielectric stack while the temperature sensor was fabricated using an SnO_2-carbon nanotube composite.[71] A semi-flexible ISFET comprising of an ultrasonically sprayed carbon nanotube sensing layer on a polyamide substrate and a rigid extended FET exhibited promising outcomes particularly towards the development of ISFETs deployed in areas with high curvilinearity such as finger-tips where the degradation in the structural morphology of metal-oxide based sensing membranes could lead to diminished performance.[72]

However, bendability itself is not sufficient as many of the emerging flexible ISFET-based applications require high performances to meet fast communication and computation requirements. Furthermore, due to the assimilation of mechanical energy during traditional wire-bonding utilizing ultrasonic power, flexible substrates exhibit a loss of mechanical robustness that leads to additional challenges associated with their integration on substrates such as flexible printed circuit boards (FPCBs).[73] Up to date, all the previously discussed technologies offer modest performances compared to high-performance silicon-based CMOS technology owing to the low charge-carrier mobility and the poor resolution of printing technologies typically used to fabricate the devices from organic semiconductors.[74] For these reasons, silicon has caught the attention again and new ways of using it in the area of flexible electronics have been explored, such as Si-nanowires (Si-NWs) and ultra-thin chips (UTCs) that can be also utilized under high temperatures due to their ability to withstand high temperatures.[75–77] Toward the

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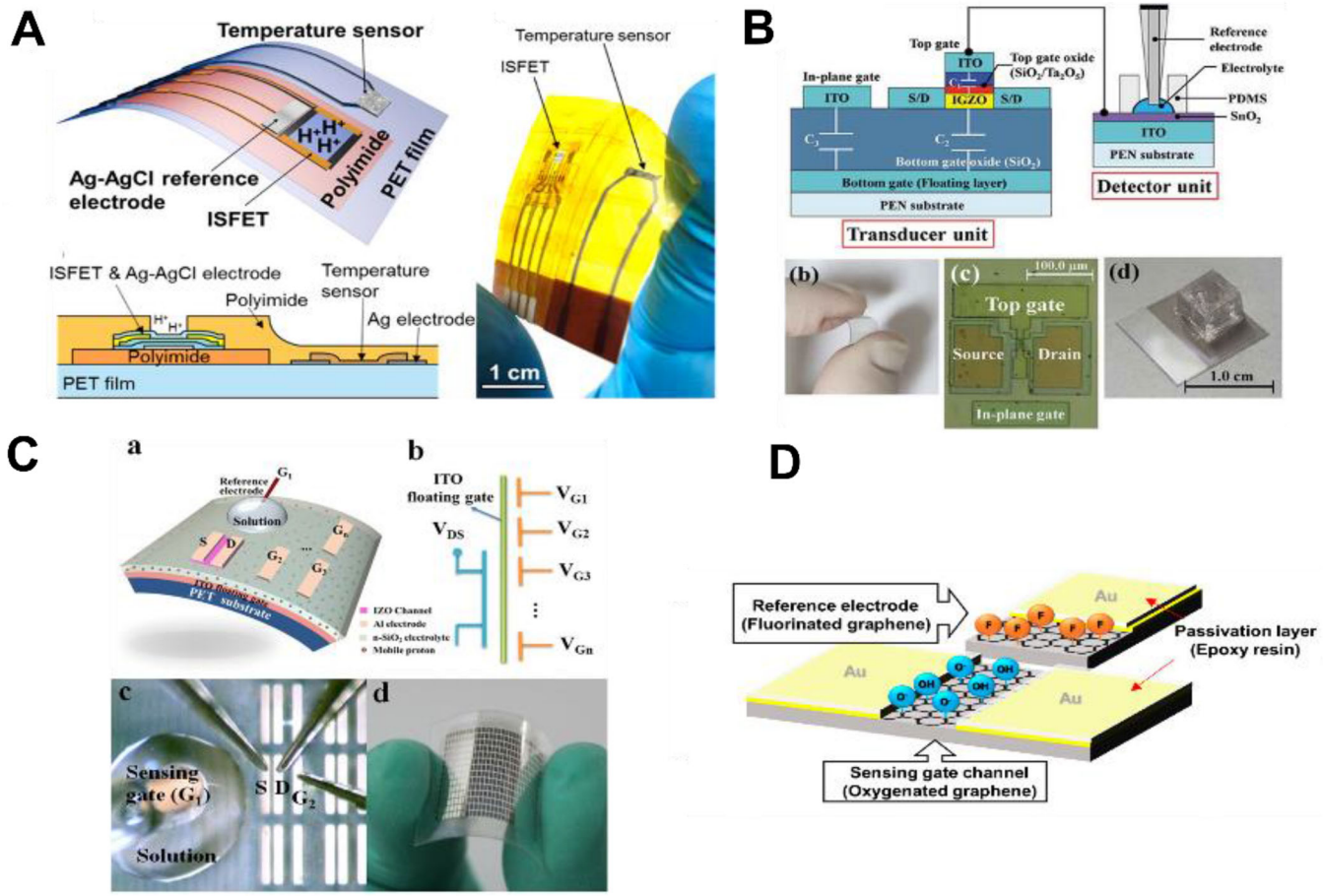

FIGURE 3 Flexible ISFET architectures. (a) pH-Temperature sensor fabricated on PET. Adapted with permission from Ref. [67]. Copyright 2017, American Chemical Society, (b) ISFET with in-plane gate coupling on PEN. Adapted with permission from Ref. [68]. Copyright 2020, Taylor & Francis, (c) Multielectrolyte-gated neuromorphic ISFET on PET. Adapted with permission from Ref. [56]. Copyright 2015, Nature, (d) Flexible ISFET with coupled graphene reference electrode.[69] Copyright 2020, MDPI

development of wearable, stretchable, and biocompatible CMOS-based ISFET 2D-arrayed systems, a 4 × 4 CMOS-compatible ISFET array has been reported in a custom 2 μm process with flexible and stretchable interconnects using parylene as biocompatible encapsulation while exposing the ion-selective membrane using localized ablation of parylene.[78]

The appealing characteristics of inorganic semiconductor transistors primarily fabricated on silicon, such as high mobility, thermal resistance, long-term stability, low sub-threshold slope, high I_{ON}/I_{OFF} ratio, accurate control of threshold voltage, and relatively low process variability make them a continuing attractive choice for device development. Furthermore, CMOS compatible ISFETs can be fabricated with on-chip signal conditioning and readout circuits at reasonable costs on a single substrate and are preferred. In order to achieve flexible ISFETs fabricated using CMOS compatible materials, it is important to generate flexibility via alternate routes such as wafer or chip thinning, etching, grinding, and lapping.[79] This provides the added advantage of increasing ISFET performance by reducing its non-ideal response comprising of low-frequency diffusion-based drift via compensation by thin chip bending accomplished through exploiting the large in-plane stresses developed in Si leading to breaking of valley degeneracy.[54]

The process of thinning high-quality wafers or chips without disturbing the surface morphology, trap density, crystal properties as well as the structure due to abrasive wear continues to pose a challenge in the development of inorganic flexible ISFETs of which the sensitivity and accuracy is strongly dependent on channel and surface properties of the sensor. This bottle-neck has led to the development of hybrid ISFETs wherein the sensing (ion-sensitive membrane) and transducing (FET) units are separated thus enabling efficient capacitive coupling while the sensing topology is fabricated on flexible materials made of plastic with comparatively in-expensive fabrication.[80] However, thin-film transistors continue to exhibit inferior electrical properties as compared to their bulk

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inorganic substrate counterparts with diffused channels.[81] In this regard, the development of ISFETs in the context of CMOS technology on semiconductors is discussed in the following subsection. A perspectival overview of chip thinning technology is provided in the context of ISFETs and intrinsic compensation techniques utilized in reducing non-idealities.

3.1 | Flexible ultra-thin ISFETs-on-semiconductors

Fabrication of bendable transistors and their associated circuits can be carried out on monocrystalline high-quality substrates via thinning methodologies leading to ultra-thin chips (UTCs) with thickness lower than 50 μm. Furthermore, thinning of ISFET integrated circuits enables stacking of multiple chips that is necessary for improving density without increasing the occupied area. It is important to take into account the variations in carrier mobility and threshold voltage due to the bending of piezoresistive materials such as Si and Ge in order to design appropriate CMOS circuitry on the same substrate. It is known that local and global uniaxial strains within both elemental and compound semiconductors such as Si, Ge, and GaAs affect their quantum-level characteristics leading to an overall improvement in the transfer characteristics of the transistors fabricated on these building blocks.[85] Furthermore, heterostructures such as Si/SiGe generate on-wafer stresses of approximately 700 MPa in magnitude.[86] In addition to the materials, stresses associated with layouts for instance shallow trench isolation (STI) structures that are utilized to prevent conductive paths between a device on the same chip, vary the effective threshold voltage of the devices due to the generation of compressive stresses more than 750 MPa.[87]

Fabrication protocols that are utilized for thinning of chips can be classified based on the step at which they are implemented, that is, via post-processing or pre-processing of the chip, a complete review of which can be found elsewhere in the context of active devices.[79] Among the post-processing steps, grinding (back grinding, dicing before grinding, and TAIKO), dry etching and layer transfer (controlled spalling and proton-induced exfoliation) constitute the primary techniques for Si substrates. Thinning procedures that require preprocessing constitute directional wet etching and epitaxial thinning wherein additional protective masks and etch stop layers need to be fabricated to control the thinning procedure without damaging the active devices.[79] Rigid ultra-thin bodied wafers with buried oxides and supporting semiconductor layers can be further converted into flexible substrates via SOI box/bulk removal.[79] It must be noted that the resulting mechanical and electrical properties of the substrate after thinning significantly depend on the procedure and the resulting defect state density as well as the inherent anisotropic stresses produced. For example, a 15-20 μm UTC obtained via reactive ion etching exhibits a high stiffness of 2.34 GPa and can bend down to 2.5 mm bending radius without fracturing. Whereas a UTC obtained by grinding and polishing can bend down to 33 mm bending radius without braking and a UTC obtained by dicing-before-grinding technique exhibits a strength between 1.6 and 2.7 GPa for a 48 μm die. It is worth mentioning that during the abrasive back-grinding process there are defects induced at the backside of the chip that leads to residual stresses.[88] These defects can be removed by polishing steps to reach a defect-free surface. In the domain of ISFET thinning, it becomes exceedingly crucial to devise thinning protocols wherein the sensing layer of the ISFET is unaffected by the thinning process via the introduction of surface traps and impurities. A summary of the available thinning techniques in the context of ISFET module fabrication is presented in Table 2. Current CMOS ISFETs are primarily fabricated by stacking of metal pads reaching the top surface of the device through vias. Herein, the passivation layer composed of Silicon Nitride that is commonly used to protect chips from the external environment is also utilized as the sensing membrane composed of silanol and primary amine binding sites. The effect of bending on CMOS ISFETs is mainly reflected as a variation in the electrical characteristics of the transducing unit of the ISFET, that is, the MOS transistor.

Furthermore, the mechanical strength of UTCs also depends on the packaging and the amount of on-chip electronics. More specifically, it has been observed that UTCs mounted on flexible polymeric substrates using low-stress epoxies can undergo multiple reversible bending cycles. Also, the fracture strength of encapsulated UTCs has been increased up to 190% allowing an 85% increase in the bending radius compared to UTCs that are not embedded in flexible supporting substrates.[54,89–91] Similarly, the mechanical strength of UTCs is also related to the amount of on-chip electronics and the amount of processing the chip has undergone. For instance, it has been observed that blank UTCs without any processing are mechanically stronger compared to UTC with CMOS circuitry.[92,93] UTCs may experience different types of deformation such as shearing, torsion, tension, or compression, which can be quantified in terms of stress in a uniaxial or biaxial geometry.[94] The first geometry considers that the device bends in just one direction, whereas the second geometry considers that the device bends in both orthogonal directions normally occurring when there is an elastic anisotropy or an applied constraint.

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TABLE 2 Summary of chip thinning techniques in the context of ISFETs

Thinning procedure	Key Characteristics	Challenges
Back grinding	• Wafer surface with devices protected by laminated tape. • Often require UV for tape removal after grinding is complete. • Dicing carried out after process completion. • Bonded abrasive is utilized during polishing.	• UV illumination may damage ion-sensitive layer in addition to tape residue after tape removal. • Difficult to achieve thickness lower than 50 μm without additional process steps reducing ISFET bendability. • Introduction of defects and imperfections after dicing at thickness less than 50 μm thus affecting binding site density.
Dicing before grinding (DCB)	• Partial grooves created in substrate prior to grinding • Lower probability of wafer fracture in the ultra-thin regime (< 50 μm) • Suitable for wafers with large diameter (> 300 μm) enabling high-density ISFET fabrication.	• UV-illumination of top surface step is nevertheless required (can be replaced by non-UV curable materials which require cleaning with water to remove residues) • Large-area ISFETs with interconnects might be damaged to large-diameter saws
Ion Etching (IE)	• Dry as well as wet etching can be used. • Dry etching: Physical removal of material via bombardment (PIE) or via reactive species which chemically interact with substrate (RIE). • Wet etching: Anisotropic removal of bulk substrate using hydroxides.	• Charge build-up during RIE will affect the properties of sensing layer as well as dielectric if not encapsulated well. • Re-deposition during PIE affects surface properties of ISFET. • Under-cutting during wet etching might lead to removal of sensing layer due to low selectivity
Selective epitaxy	• Growth of epitaxial layer over wafer • Bulk removed via one of the above thinning processes with epitaxial layer acting as etch stop surface	• Impurity diffusion from bulk to epitaxial layer might affect channel properties of ISFET due to mobility variation. • Higher cost of fabrication
SOI Buried Oxide (BOX) removal	• Bottom silicon wafer detached from top active layer via generation of trenches in the oxide layer.	• Trenching requires fluoride etching which might reduce sensitivity of ISFET devices. • Damage of ISFET chips without adequate support on detachment • Higher cost of fabrication

The effects of mechanical deformation due to uniaxial or biaxial bending stress change the electrical resistivity of silicon that is translated into direction-dependent effective carrier masses, which effectively contribute to direction-dependent carrier mobility. This effect termed as the piezoresistive effect, which has as macroscopic effect the change in MOS transistors (MOSTs) drain-current and speed have found many applications such as the integration of pressure and strain sensors with CMOS circuits or the exploitation of bending to enhance the performance of CMOS circuits sensors.[89,95–97]

In our previous study,[89] the piezoresistive nature of silicon was exploited demonstrating real-time active drift compensation. More specifically, as the sequential externally applied dynamic strain on ultra-thin silicon substrate is increasing, the energy of the split conduction sub-band Δ4 reduces with respect to Δ2. The splitting and lowering of bands decrease the effective carriers' mass, which subsequently changes the surface carrier mobility resulting in a relative change of drain-current. Therefore, the CMOS ultra-thin ISFET-based chip can be transformed into a controllable and reversible electrical conductance modulator through fine control of the Si-substrate's bending radius. As a result, the externally applied stress-induced mobility variation can be used as a new degree of freedom to further improve the performance of nanoscale devices.

4 | CHALLENGES AND OPPORTUNITIES

A major challenge associated with achieving monolithic heterogeneous integration of low power flexible ISFETs and their associated read-out circuit on bent semiconductor chips is the electrical response of strained CMOS circuitry that might affect the overall pathway of the signal. Hence, it is important to highlight the current techniques utilized in signal conditioning of ISFET(s) output voltage or current.

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4.1 | Read-out topologies of ISFETs

Classification of read-out configurations is carried out on the basis of single-ended and differential designs mainly attributed to individual ISFETs and their arrays biased via an on-chip reference electrode.[36] These systems can be then further be subdivided as current or voltage mode wherein the former entails keeping the drain-source voltage fixed while allowing the output current to vary as a function of pH. Current-mode readouts are the preferred pathway towards obtaining rapid signal conditioning and processing, often used in miniaturized transistors due to their linear transfer characteristics in the velocity saturation regime and low power operation in the subthreshold regime.[98,99] Control of reference electrode potential is carried out electronically via amplifiers connected in the negative feedback mode.[100] The differential read-out architectures assist in partially reducing stochastic non-idealities such as drift as well as variations of pH due to temperature. As an example, a differential mode ISFET/ISFET pair circuit was designed wherein one pair was immersed into a solution of known pH acting as the buffer while the other pair performed real-time pH recordings as shown in Figure 4a.[101] The difference in the outputs was utilized for further processing hence rejecting the common non-idealities between the two pairs.[101] In the context of circuit-integrated REFETs, the design criteria must be altered to include a floating gate isolated from the solution for efficient referencing via encapsulation leading to the ISFET/REFET topology seen in Figure 4b.[102] Challenges in the utilization of reference electrode FETs remain in regards to ionic diffusion through polymeric encapsulations that in turn would lead to unwanted variations in the output.

At lower channel dimensions, the flicker noise of the transistor can lead to unwanted changes in the outputs associated with comparatively low-frequency variations of the ambient pH via superposition of the signals. This issue can be addressed via incorporation of choppers into the circuit. Techniques such as ISFET/MOSFET pair with chopping stabilization have been utilized to reduce the flicker noise while simultaneously resetting the surface potential of the floating gate of the ISFET in order to eliminate any trapped charges within the buried sites.[103] Drift constitutes another low-frequency non-ideality and can be accounted for at a circuit level via correlated double sampling (CDS) and requires careful design of switching conditions so as to not additionally filter out useful signals comprising low-frequency pH variations.[104] As an improvement to CDS, in-pixel chopper-stabilized drift compensation has also been carried utilizing low leakage resetting switches.[105] A programmable ISFET/MOSFET, highlighted in Figure 4c, shows voltage modulation of the input floating gate carried out via an extra capacitor at the cost of increased attenuation.[106] The aforementioned read-out topologies are fabricated using standard CMOS processing which is carried out on rigid semiconductor and semiconductor-on-insulator substrates. Hence, it is vital to reduce their thickness, without compromising the transfer characteristics of the device, for efficient integration on curvilinear substrates. Furthermore, this paves the way towards exploiting the intrinsic electrical variations within the semiconductor on bending thus bringing strain engineering and chemical sensing together toward the development of the next generation of ISFETs. Low-frequency drift, due to ionic diffusion as well as temperature, in CMOS ISFETs can be further addressed at the circuit level via dynamic adjustment of ISFET bias which is not suitable for large density ISFET arrays.[53] In order to account for the offset in the sensing membrane of ISFETs various compensation techniques have been proposed such as exposure of the sensing layer to UV radiation,[107] gate voltage modulation via inserting an extra capacitor at the floating gate,[108] and switched feedback resetting through an additional transconductance amplifier.[109]

To identify architectures suitable for using ISFETs in flexible electronics, we need to consider that the bending-induced variations in the transistor parameters should be compensated. In this regard, many of the circuits discussed above in relation with ISFET readout architectures could be used as they are already designed to compensate for low-frequency variations. Also, the topologies intended to compensate for threshold voltage offsets, for example, due to process-induced trapped charges, could potentially be used to compensate for changes in this parameter during mechanical deformations of the IC. These include using CDS,[110,111] applying an additional voltage to the gate using a programmable gate,[108] compensation through the source voltage,[112] or an automatic gain control (AGC).[113] Architectures aimed at temperature compensation through a reference current subtraction could also be repurposed.[114,115]

However, it should also be considered that since each MOST will be individually affected by bending, it is analog architectures that require precise parameter ratios that will be most significantly affected. This suggests that differential architectures, which incorporate reference devices to reject common-mode non-ideal effects are more appropriate for dealing with mechanical variations. These would not necessarily need to use REFETs as described previously, as the common effects are not part of the electrochemical system, but could make use of differential architectures designed to reduce PVT variations.[103,106,116,117] The layout is also an important consideration for these circuits. Using techniques such as compensation and considering the orientation of devices with respect to the expected

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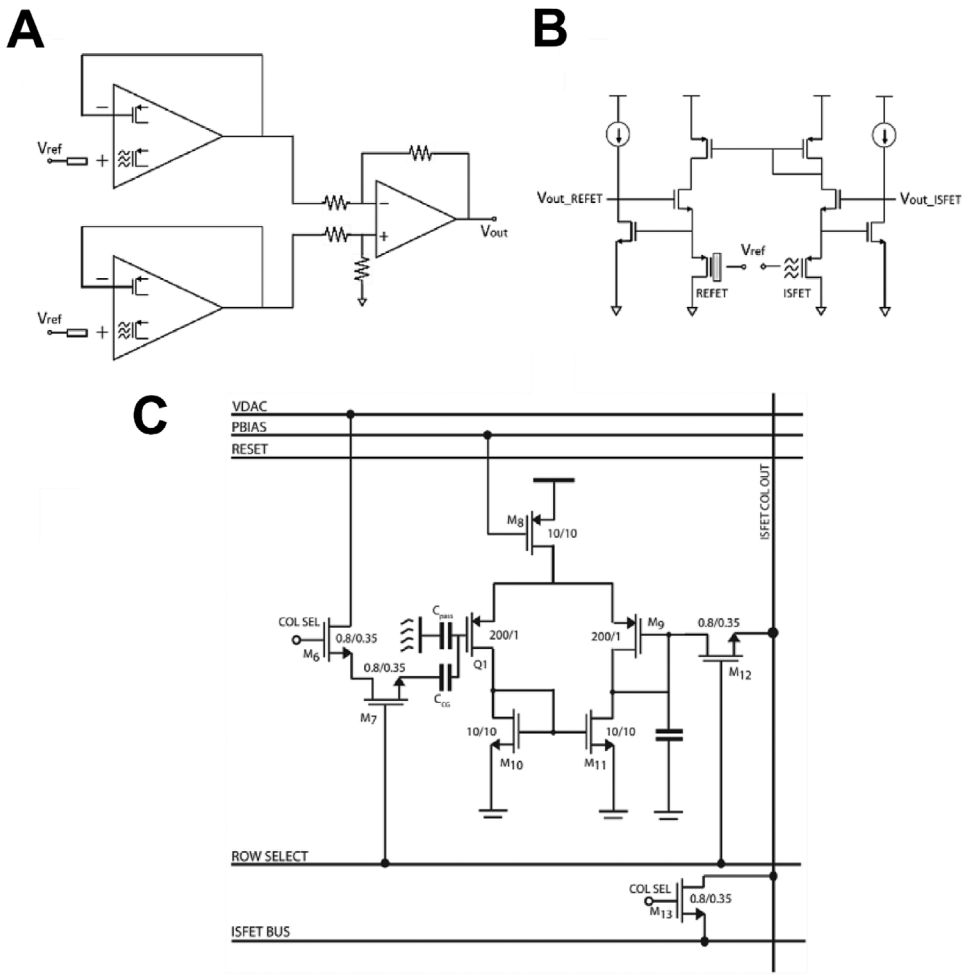

FIGURE 4 (a) The ISFET/ISFET differential amplifier configuration.[101] (b) ISFET/REFET voltage clamped topology.[102] (c) Programmable gate ISFET/MOSFET differential amplifier[106]

bending axis could help to alleviate the effects of mechanical deformation.[77] Overall, there is limited investigation into circuit techniques for compensating mechanical deformation, presenting an opportunity for researchers in this space.

5 | CONCLUSION

Overall, it is clear that there is a need for flexible electrochemical sensors, and flexible ISFETs could provide a number of opportunities in this application space. However, there are several challenges to enable these next-generation electrochemical sensors. First is to overcome errors in the circuitry due to mechanical deformation of ultra-thin Si-dies. Circuit techniques can be implemented on the front-end to overcome these errors, but modeling and characterization is also an important step. Furthermore, the optimization of on-chip architectures will reduce the power consumption and the inclusion of on-chip microcontrollers and transceiver circuits will improve the functionality and programmability of the IC allowing wireless communication with portable electronic devices. Thus, the system can become lighter and easier to be integrated on smart wearables, such as wristbands, contact lenses, and smart rings, as well as on ingestible systems, such as smart pills. In addition, it is important to develop appropriate bonding techniques to acquire reliable and robust connections from the bonding pads of the ultra-thin ICs to the pads on flexible PCBs. At the same time, the ICs should be able to mechanically deform, if required, without compromising the continuity of the connections. Promising techniques seem to be the printing and photolithography techniques. Also, flip-chip bonding of UTCs on flexible polymeric substrates via through-silicon vias (TSVs) is another promising approach. As an alternative, the ICs could also wirelessly communicate with off-chip components allowing data transmission and powering of ICs through indicative coupling reducing to the bare minimum the need of bond-pads and wire-bonds.

Besides, the development of appropriate packaging is also critical for the realization of mechanically bendable ultra-thin chips that can be used in aqueous environments. A polymeric and passivating coating, such as polyimide or PDMS that can be patterned to expose the sensing area to the aqueous solution while keeping the wire-bonds and bond-pads passivated could be a promising solution. Leakages of aqueous solutions through the interface of the polymers with the ICs or leakages through the bulk of the polymers should also be examined. Finally, the development of miniaturized 2D reference electrodes at the surface of ultra-thin ICs is another important aspect of an ISFET-based sensing microsystem. Next-generation wearable or implantable ICs with integrated biochemical sensors, such as ISFETs, require an on-chip reference electrode to ensure robust measurements as the bulky and glass reference electrodes are not suitable in these applications. Similar to the case of wire-bonds, the reference electrodes can be developed using either printing or photolithography techniques. While the latter requires specialized and expensive equipment, cleanroom facilities, and several processing steps, fine electrohydrodynamic printing could also be a promising alternative as Ag/AgCl can be directly printed at the surface of ultra-thin dies creating predefined patterns without the need for lift-off or etching processes.

CONFLICT OF INTEREST

The authors declare no conflict of interest.

DATA AVAILABILITY STATEMENT

Data sharing not applicable to this article as no datasets were generated or analyzed during the current study.

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