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Design of Terahertz InP pHEMT Using Machine Learning Assisted Global Optimization Techniques

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Abstract — This paper presents an optimal design of terahertz InP-based pseudomorphic high electron mobility transistors (pHEMT) powered by an artificial intelligence (AI) technique. Unlike the traditional physics-based design optimization methods, the new technique employs a machine learning-assisted global optimization algorithm. A state-of-theoperating at millimeter-wave art commercial pHEMT frequencies was used to calibrate the physics-based model. Based on the pHEMT, the proposed machine learning-assisted optimization method was implemented with the constraint of gate length, i.e., 100 nm. The simulation results show significant improvement in terms of cut-off frequency, i.e., 57%, and maximum oscillation frequency, i.e., 30%, compared to the commercial design. To the best of our knowledge, this is the first time to employ machine learning-assisted global optimization techniques to pHEMT design, showing high potential in terms of numerical simulation and device design for ultrafast semiconductor devices.

Keywords — pHEMT, terahertz, machine learning, global optimization.

I. INTRODUCTION

Terahertz (THz) frequency, covering 100 GHz to 3 THz, has attracted attention in many applications, including security screening [1], next-generation autonomous radars [2], and high data rate mobile communications beyond 5G [3]. Transistors are the core devices in the front-ends of RF systems, and indium phosphide (InP)-based pseudomorphic high electron mobility transistors (pHEMTs) have a cut-off frequency $f_{\rm T}$ over 700 GHz and a maximum oscillation frequency $f_{\rm max}$ close to 1.5 THz [4]. This makes them ideal enabling technologies for terahertz monolithic integrated circuits, which have the advantages of low cost, ease of integration, and small size over other technologies.

However, the design of pHEMTs is not trivial, which involves both material (epitaxial layers) and structure (mainly electrodes) optimization. The total number of parameters to be optimized could be more than 20. For example, to achieve the highest operating frequency, one should first optimize materials including material composition, layer thickness, and doping method and level for as high electron mobility as possible and then optimize transistor structure, including gate length, gate shape, source-drain separation, the gate to drain/source distance, etc. to reduce parasitic capacitance. In addition, metal alloys/stacks for gate and source/drain contacts should also be optimized. In the past, the above optimization process mainly relied on trial-and-error with fabricated devices. Clearly, it is a time-consuming and costly method and may also obtain suboptimal results. Recently, numerical simulation models have become available. However, the drawbacks on efficiency and optimization quality of the trialand-error method still exist. This calls for the need to employ modern optimization techniques.

This paper introduces a state-of-the-art machine learningassisted global optimization method to design pHEMTs for the first time. The employed algorithm is called surrogate model assisted differential evolution for antenna synthesis (SADEA), initially developed for antenna design [5]. We employ SADEA to a commercial pHEMT structure and obtain the optimized new design, showing 57% and 37% improvements on f_T =336 GHz and f_{max} =770 GHz, respectively, without changing the gate length. The optimization time using a normal desktop computer is 16 hours, significantly shorter than the conventional methods, which may take several days. The new method shows great potential in terms of efficiency and optimization quality for ultrafast transistor design. It could also be extended to other advanced semiconductor devices and circuits.

The remainder of this paper is organized as follows. In Section II, the physical model of pHEMTs and the SADEA algorithm are first introduced. In Section III, a case study of optimizing commercial InP pHEMTs using the SADEA is demonstrated. Conclusions are finally provided in Section IV.

II. SADEA-BASED PHEMT DESIGN OPTIMIZATION METHOD

Depending on applications, the design focus of HEMTs varies. For ultrafast applications, $f_{\rm T}$ and $f_{\rm max}$ are the two main figures of merit and should be maximized wherever possible. This section will introduce pHEMTs, the conventional design method, and the SADEA-based design method.



Fig. 1. Illustration of epilayers and electrodes of a pHEMT.

A. Introduction to pHEMTs

Fig. 1 shows a typical InP pHEMT. The epilayers are grown on a semi-insulating InP substrate using either Metal-Organic Chemical Vapor Phase Deposition (MOCVD) or Molecular Beam Epitaxy (MBE). The channel layer, made of In_yGa_{1-y}As where y indicates indium mole fraction, is sandwiched by two wider bandgap In_{0.52}Al_{0.48}As layers. A quantum well is formed in the channel, making electrons well confined. The top $In_{0.52}Al_{0.48}As$ is further divided into halves by a silicon delta doping layer that provides electrons to the channel. The lower In_{0.52}Al_{0.48}As adjacent to the channel is a spacer that separates electrons from the dopants (i.e., silicon), reduces the scattering of impurities, and improves electron mobility in the channel. The upper $In_{0.52}Al_{0.48}As$ is a barrier where the gate sits, controlling the channel's electron flow. A heavily doped n-type In_{0.53}Ga_{0.47}As layer above the barrier forms the ohmic contacts for low contact resistance. The cap layer under the gate is removed to allow the formation of a Schottky barrier.

The epilayers play a significant role in determining the electron mobility and the sheet resistance of the channel, contact resistance, parasitic capacitance, $f_{\rm T}$ and $f_{\rm max}$. Researchers have attempted to improve carrier mobility by optimizing the thickness, mole fractions, and material compositions in the barrier, spacer, and channel. For example, lattice-matched InAlAs/InyGa_{1-y}As/InAlAs (*y*>0.53) composite channel with high indium mole fraction was investigated in [6]. InGaAs/InP composite-channel HEMT was found to have mobility as high as 11,000 cm²/Vs⁻¹ [7]. Recently, InAs/InGaAs composite-channel HEMT was reported with electron mobility approaching 15,000 cm²/Vs⁻¹ [8].

Apart from materials, electrodes also play a significant role on $f_{\rm T}$ and $f_{\rm max}$. The smaller the gate length L_g , the lower the gate resistance, leading to higher $f_{\rm T}$ and $f_{\rm max}$. As shown in Fig.1, a T-shaped Schottky gate is often used to balance current capacity, narrow gate length, and parasitic capacitance. However, the gate foot shorter than 50 nm becomes challenging to make. A 10 nm T-gate has been demonstrated [9], but its mechanical support provided by the foot is not sufficiently strong, and therefore the yield becomes comparatively low. In this work, the foot length of the T gate is kept at 100 nm.

B. State-of-the-art pHEMT design optimization

A widely used method for simulation-based pHEMT design optimization is based on equivalent circuits, as shown in Fig. 2. Equations (1) and (2) give the main parameters from the small-signal equivalent circuit that affects $f_{\rm T}$ and $f_{\rm max}$, and Table 1 explains those parameters. Deriving such a circuit relies on accurate measurement, which is known notoriously time-consuming. Hence, most foundries can only provide equivalent circuit models for a few biasing conditions. This restricts the flexibility of optimization and often obtains sub-optimal results.

An alternative method is modeling devices using physicsbased CAD tools (e.g., Sentaurus). The advantages over circuit models include high accuracy and flexibility. However, the



Fig. 2. The complete small-signal equivalent circuit of a pHEMT.

$$f_{T} = \frac{g_{m}}{2\pi (C_{gs} + C_{gd})(1 + \frac{(R_{s} + R_{d})}{R_{ds}}) + C_{gd}g_{m}(R_{s} + R_{d})}$$
(1)
$$f_{max} = \frac{f_{T}}{2\sqrt{\frac{R_{g} + R_{i} + R_{s}}{R_{ds}} + 2\pi f_{T}R_{g}C_{gd}}}$$
(2)

Table 1. The main parameters from the small-signal equivalent circuit affect the operating frequencies.

Description
Source-gate capacitance
Drain-gate capacitance
Parasitic source resistance
Parasitic drain resistance
Output resistance
Intrinsic channel resistance
Transconductance

drawbacks located in the optimization methods. Most available methods neither have sufficient optimization ability (e.g., quasi-Newton method) nor efficient (e.g., genetic algorithm). Note that the simulation of a physics-based device model needs numerical techniques (e.g., finite element analysis), which is computationally expensive, and standard global optimization methods such as genetic algorithms often need thousands to tens of thousands of such simulations.

C. pHEMT design optimization by SAEDA

To reduce the optimization time to a practical level while maintaining the optimization quality as standard global optimization algorithms, surrogate model-assisted evolutionary algorithms (SAEA) are introduced into pHEMT design in this work. In SAEA, the surrogate model mapping the inputs (i.e., design variables) and outputs (i.e., performances) are often constructed by machine learning techniques. By replacing the computationally expensive Sentaurus simulations with computationally cheap surrogate model predictions, the optimization time can be considerably reduced. In this paper, the selected algorithm is SADEA. SADEA is initially designed for microwave antenna design exploration; however, good performances are also found in other applications. This is the first attempt to implement the algorithm on HEMTs. Fig. 3 illustrates how MATLAB, which runs the SADEA code, collaborates with Sentaurus, which





Fig. 4. The flow diagram of SADEA.

runs HEMTs' simulation.

In SADEA, the machine learning method is Gaussian process (GP), the evolutionary algorithm is differential evolution (DE), and the model management method is surrogate model-aware evolutionary search framework [10]. The flow diagram of SADEA is shown in Fig. 4. Here is how it works. A Latin hypercube sampling is first implemented to initialize the design space. Then, in each iteration, the k topranked candidate designs are selected to form the parent population. From the parent population, the new population is generated by applying DE mutation and crossover operators. The used operator here is DE/best/1 [11], showing fast convergence speed. Then, GP surrogate models are built for each candidate design in the generated new population. The training data are the nearest designs (based on Euclidean distance) from the simulated designs. Then, a prescreening method, lower confidence bound [12], is used to consider both prediction uncertainty and performance to find the expected most promising design in the current iteration, which will then be simulated by Sentaurus. This process continues until the stopping criterion is met. More details about SADEA can be found in [5].

III. CASE STUDY

In this case study, our optimal design is compared with a commercial pHEMT by Diramics [13]. We will first calibrate the device model using the data provided by Diramics, then SADEA is employed to optimize the design parameters. Note gate length is not optimized in this work.

A. Model Calibration

Commercial pHEMT's datasheet is available from [13]. The models used in Sentaurus include Hydrodynamic transport models for electrons, High-field mobility, and the Recombination model includes Shockley–Read–Hall (SRH), Auger, and Radiative. The ohmic contact or Schottky contact are specified. Table 2 lists material properties used in the simulation. All the parameters are referred to room temperature conditions. To guarantee the accuracy of the simulation model, the mesh density below the gate region is set high.

Table 2. List of main semiconductor parameters used in the modeling.

Parameter	InP	Ino.53Gao.47As	Ino.52Alo.48As
Lattice constant (Å)	5.86	5.86	5.86
Band gap (eV)	1.34	0.72	1.48
Dielectric constant	12.4	14.3	12.4
(static)			
Electron affinity (eV)	4.44	4.55	4.27
Effective mass m_e^* / m_0 at	0.079	0.047	0.081
central vallev			

The simulated DC (Fig. 5) and RF (Table 3) show good agreement with the experimental results [13]. The final thickness of the epilayers is shown in Fig. 1.



Fig. 5. IV characteristics and transconductance of the experimental (Diramics) and simulated 100 nm pHEMT at ambient temperature, Vds=0.9 V.

B. Device Optimization

In this study, 16 design parameters are selected for optimization. Table 4 shows the search range of the parameters. To ensure the optimized parameters are physically realizable, geometric constraints are set as follows: let x denote the design parameters, and the pHEMT design optimization problems can be described as follows.

C. Results

The optimized 100 nm pHEMT design is shown in Table 4, the optimization results show that the Diramics model is within a reasonable boundary value range. The values of the epitaxial layer and structure of the device tend to the boundary

Table 3. Key performances of 100 nm pHEMT between the Diramics, simulated and optimized.

Performance	Diramics	Simulated	Optimized
Transconductance (mS/mm)	1250	1255	1672
Drain Current (mA/mm)	700	675	775
f _T (GHz)	220	215	336
f _{max} (GHz)	550	542	770
C_{gs} (fF)	38	10-22	30-53
C_{gd} (fF)	11	3-24	3-17

Table 4.	The search	ranges o	f the	design	parameters	and	the of	ptimized	value.

x	Parameter name	Search range	Optimized value
1	Substrate thickness (um)	50-100	61
2	Buffer thickness (um)	0.2-0.8	0.2
3	Channel thickness (nm)	4-20	4
4	Spacer thickness (nm)	2-10	2
5	Barrier thickness (nm)	8-15	8
6	Cap thickness (nm)	8-25	8.5
7	Delta-doping concentration	1×10 ¹² -	9.4×10 ¹²
	(cm^2/Vs^{-1})	1×10 ¹³	
8	Indium fraction of channel	0.6-0.85	0.85
	layer		
9	Location of delta doping (nm)	4-21	7
10	Passivation thickness (nm)	40-100	40
11	Recessed thickness (nm)	0-7	5
12	Gate foot location (um)	0.45-1.05	0.47
13	Gate-source separation (um)	0.1-0.6	0.1
14	Gate-drain separation (um)	0.1-0.6	0.1
15	Schottky barrier (eV)	0.6-1.5	0.6
16	Contact resistance (ohm·um)	30-120	30



Fig. 6. IV characteristics and transconductance of the experimental (Diramics) and the optimized 100 nm pHEMT at ambient temperature, $V_{ds}\!\!=\!\!0.9$ V.

conditions and good results can be obtained. The $f_{\rm T}$ and $f_{\rm max}$ are improved to 336 GHz and 770 GHz compared to 220 GHz and 550 GHz that are obtained by Diramics, respectively. In addition, Fig. 6 shows the transfer characteristic of the transistor of the optimized HEMT is higher than the Diramics and demonstrates its lower at a higher frequency. It can be seen that after optimization: (1) the indium content in the channel layer is increased to 85%; (2) the mobility approaches to 14000 cm²/Vs⁻¹; (3) the parasitic capacitance is reduced by the asymmetric structure. Therefore, this optimized pHEMT

has a higher operating frequency in $f_{\rm T}$ and $f_{\rm max}$. The results are summarized in Table 3.

IV. CONCLUSION

machine learning-assisted In this paper. global optimization techniques are introduced to design pHEMT. Remarkably, the Diramics' 100 nm pHEMT is optimized from its epitaxy layer and device structure. After optimization, the cut-off frequency and maximum oscillation frequency are improved from 215 GHz to 336 GHz and 542 GHz to 770 GHz, respectively. Moreover, the transconductance and current are improved to 1.6 S/m and approach 0.8 A/mm, respectively. The total number of Sentaurus simulation iterations is 240, costing 16 hours in a normal desktop computer. This new method shows high potential in terms of efficiency and optimization quality for transistor design.

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