Stability and $V_{\min}$ Analysis of Ferroelectric Negative Capacitance FinFET Based SRAM in the Presence of Variability

Tapas Dutta*†‡, Vihar Georgiev*†, Asen Asenov*†
*Device Modeling Group, University of Glasgow, Glasgow G128LT, UK.
†Semiwise Ltd., G128LT, UK.
‡e-mail: tapas.dutta@glasgow.ac.uk

***Abstract*—For the first time, we analyse SRAM cells made of ferroelectric based negative capacitance (NC) FinFETs considering both global and local variability via Monte-Carlo circuit simulations. First we compare and explain the impact of variability on the device characteristics and the extracted figures of merit of conventional and NC transistors. Then we show that suppressed relative variability in NCFETs leads to lowering of the static $V_{\min}$ (minimum supply voltage needed for SRAM operation) compared to conventional FinFET based SRAM. We use a physics based compact model for negative capacitance FinFETs realized by a self-consistent coupling of the standard BSIM-CMG compact model for FinFETs with the Landau-Khalatnikov (L-K) model of ferroelectrics. We demonstrate that on including the variability in the ferroelectric thickness and material parameters as well, the advantage of NCFETs diminishes. For the baseline FinFET, we have used model cards from a freely available predictive process design kit (PDK) for the 7nm technology node where the parameters are optimized for SRAM applications.**

***Keywords*—Negative Capacitance, NCFET, FinFET, SRAM, n-curve, $V_{\min}$, ferroelectric, variability**

I. Introduction

The Static Random Access Memory (SRAM) is an important component in system on chips and it occupies a major portion of the silicon real estate. However, in recent years, the scaling of SRAM has slowed down due to issues of stability and difficulty in scaling down the supply voltage at advanced technological nodes. Since the introduction of FinFETs, the corresponding SRAM design has been researched extensively during the last decade [1], [2]. As increased power consumption is a major issue in the semiconductor industry, a lot of work has been done on steep slope devices with an aim to be able to lower the supply voltage. For example, impact ionization MOSFET (IMOS) [3], tunneling based FET (TFET) [4], [5], nanoelectromechanical (NEM) relays [6], hybrid phase-transition FET (Hyper-FET) [7] etc. have been explored, but none of these have been able to prove to be a worthy successor to the conventional Si MOSFET and its multi-gate avatars. Meanwhile, the use of the negative capacitance effect of ferroelectrics to realise sub-thermionic switching in MOSFETs [8] has been pursued with a lot of interest both in the academia and the industry during the past decade. The key idea is that having a negative capacitance in the gate stack of a MOSFET can lead to effective amplification of the applied gate bias and hence steep subthreshold slopes can be achieved, thus surpassing the Boltzmann limit of 60 mV/decade at room temperature. This enables more aggressive supply voltage ($V_{\rm DD}$) scaling and hence lower leakage without losing drive current. Without drastic changes required in the existing process-flow, and with the discovery of ferroelectricity in nanoscale layers of HfO_2 which is CMOS-compatible, the NCFET is indeed an attractive option.

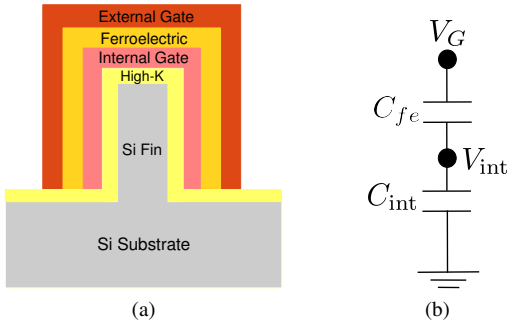


Fig. 1. (a) Cross-sectional schematic of the NC-FinFET with baseline dimensions corresponding to the ASAP7 PDK's SRAM FinFETs. (b) Equivalent Capacitance Representation

Here it is worth mentioning that the physical understanding of the negative capacitance mechanism and associated device engineering are still far from being mature [9], and the future of NC technology and the degree of advantage it can deliver over existing state-of-the-art CMOS technology is debatable [10]. However, consistent experimental demonstrations of NCFET devices and circuits showing improved performance over conventional FETs have been quite promising and reassuring [11], [12].

Various modeling approaches for NCFETs and studies on the impact of their improved transistor characteristics on circuits have been reported. In particular, performance of 7nm node NC-FinFET based SRAM was reported in [13]. Further,

NC transistors have been shown to offer variability suppression [14]–[17] which is expected to improve the minimum supply voltage for SRAM operation ($V_{\min}$). In this work we examine the NC-FinFET based SRAM stability through circuit simulations using a physics based compact model of NC-FinFETs and evaluate read and write $V_{\min}$.

II. Device Description, Modeling Approach, and Simulation Methodology

A. NC-FinFET

Fig. 1(a) shows the cross-sectional schematic of the NC-FinFET with the ferroelectric layer sandwiched between the internal gate of the baseline 7nm node FinFET, which floats, and an external metal gate, to which the gate bias is applied. This Metal-Ferroelectric-Metal-Insulator-Semiconductor (MFMIS) architecture is easy to model as the ferroelectric capacitor and rest of the device (the baseline FinFET) can be considered as elements connected in series. This connected capacitor representation is shown in Fig. 1(b). Here V_{int} is the voltage available at the internal gate (i.e. the gate of the baseline FinFET). NC-FinFETs have improved electrostatics due to the internal voltage gain, given by:

$$A_V = (1 - C_{\text{int}}/|C_{fe}|)^{-1}, \tag{1}$$

where C_{fe} is the ferroelectric capacitance (conditionally negative) and C_{int} is the positive capacitance of the internal MOSFET including the gate insulator capacitance (both are bias dependent). This forms the basis of the NC transistor operation. Table I lists the key structural parameters of the device, with the values for the reference FinFET having been taken from [18], and the ferroelectric parameters from [19].

TABLE I. Device Details

Parameter	Value
(a) Reference FinFET [18]	
L_g	21 nm
T_{fin}	6.5 nm
H_{fin}	32 nm
EOT	1 nm
$V_{t,n}$	0.25 V
$V_{t,p}$	-0.20 V
(b) Ferroelectric Layer (Doped HfO_2)	
t_{fe}	1-4 nm
P_r	5 μC/cm^2
E_c	1 MV/cm.

B. Compact Modeling of NC-FinFET

The compact modeling approach employs a self-consistent coupling of the industry standard BSIM-CMG model [20] with the ferroelectric model written in verilog-A [21]. The key equations and assumptions have been included in the flowchart in Fig. 2. The free energy density of the system (G) is a function of the polarization (P) and the electric field across the ferroelectric (E). The dynamics of the system is described by the Landau-Khalatnikov equation [22] relating the derivative of polarization with respect to time and that of free energy density with respect to polarization. For the ferroelectric material used in this work, with γ = 0, the Landau coefficients α and β can be expressed in terms of the coercive field (E_c), and remanent polarization (P_r) as [23]: $\alpha = -(3\sqrt{3}/4)E_c/P_r$, and $\beta = (3\sqrt{3}/8)E_c/{P_r}^3$.

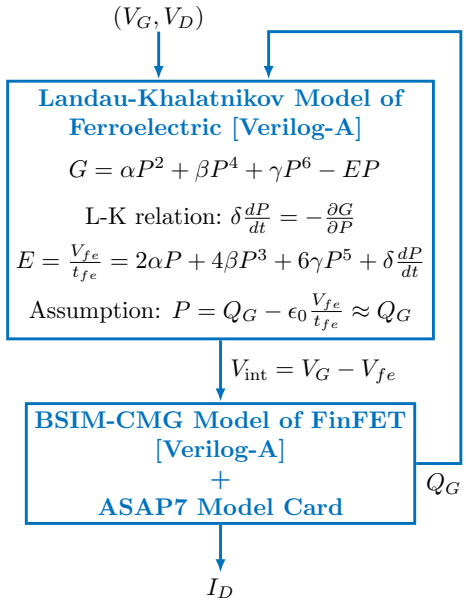
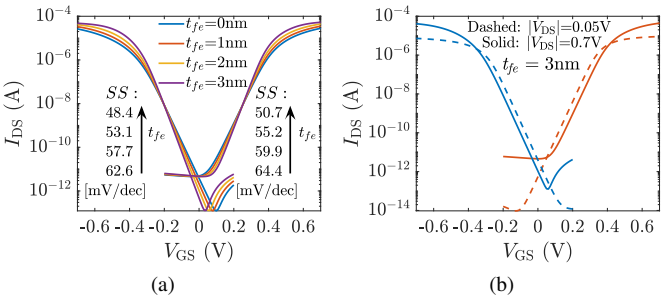


Fig. 2. NC-FinFET Compact Modeling Approach. P = polarization, G = total free energy density, E = electric field, V_{fe} = voltage drop across the ferroelectric, t_{fe} = ferroelectric thickness, δ = ferroelectric damping factor, Q_G = gate charge density, and α, β, γ: Landau coefficients.

The self-consistent scheme works as follows: the gate charge density, Q_G obtained from the BSIM-CMG model is fed into the L-K model which outputs the voltage drop across the ferroelectric (V_{fe}), which in turn is used to calculate V_{int}, the effective voltage at the internal gate, which finally is an input back to the BSIM-CMG model. $V_{\text{int}} = V_G - V_{fe}$, where V_G is the applied gate bias.

We would like to note that a major contention to the phenomenological modeling approach using Landau theory of phase transitions was the absence of direct experimental evidence of the S-shaped $P-E$ curve which is at the heart of the negative capacitance modeling used here. Direct observation of steady state negative capacitance and the S-shaped curve has recently been demonstrated experimentally [24], [25], which gives more credence to this approach. Although simple, the model has so far been able to explain all of the observed behaviours characteristic of the negative capacitance transistors unlike some other models [26]. The L-K model has been shown to be able to reproduce experimental results including circuit performance in NC-FinFETs with ultra scaled ferroelectric layers, e.g. ferroelectric thikness of 1.5nm in [27], and 3nm



(a) (b)

Fig. 3. (a) Nominal $I_{\rm DS} - V_{\rm GS}$ characteristics of n and p type Ref. FinFETs and NC-FinFETs with different t_{fe} at $V_{\rm DS}$=$V_{\rm DD}$=0.7V at iso-V_t. The subthreshold swing values for the devices have also been included. (b) Demonstration of Negative DIBL in NC-FinFETs with t_{fe}=3nm considering $I_{\rm DS} - V_{\rm GS}$ characteristics at $V_{\rm DS}$=0.05V, 0.7V.

in [12]. Further, [12] suggests that the NC effect does not inherently lead to any additional switching delays.

Fig. 3(a) shows the nominal transfer characteristics of the reference FinFETs and NC-FinFETs with varying t_{fe} where the nominal FE parameters for all thicknesses have been assumed to be the same. All the nominal NC-FinFETs have been set to the same threshold voltage as that of the reference FinFET. The NC-FinFETs show superior characteristics with steeper subthreshold swing (sub-60 mV/decade) and higher drive current compared to the reference FinFET. These improvements are enhanced as the ferroelectric thickness increases. Fig. 3(b) shows the negative DIBL in the NC devices, demonstrating the capability of the compact model.

C. Statistical Simulation Methodology

Fig. 4 describes the overall simulation methodology used in this work. In contrast to [28], where we simulated statistical variability using TCAD and used the extracted standard deviation in V_t to generate a statistical distribution of the VTH0 parameter alone in the compact model card for the Bulk NCFET, here we take a different approach. Firstly, BSIM-CMG is not a threshold voltage based model unlike BSIM4 used for the bulk MOSFET. Also, considering only V_t variability may not be sufficient for FinFETs. In the present work we use the compact model approach and directly apply process variability in device parameters in the circuit simulator using Monte-Carlo techniques [29] for both the baseline transistor as well as the ferroelectric layer. We consider both global variation as well as local variation (mismatch). If P_0 denotes the nominal process parameter, then the overall process parameter for any transistor instance considering variability can be expressed as [30]:

$$P = P_0 + \Delta P_{\rm GV} + \Delta P_{\rm LV}, \tag{2}$$

where $\Delta P_{\rm GV}$ and $\Delta P_{\rm LV}$ are the global (correlated) and local (uncorrelated) variations. In any Monte-Carlo run, $\Delta P_{\rm GV}$ is the same for all the six transistors in the SRAM cell, while $\Delta P_{\rm LV}$ is different for each.

III. Variability Suppression in NC-FinFETs

The improved electrostatics in NCFETs can lead to a suppression of statistical variability. This has been shown using TCAD simulations as well as compact modeling approaches. In particular, it has been shown earlier that compared to regular FinFETs, NC-FinFETs can be less sensitive to process parameter variations, enhancing further the promise of these steep slope devices. For example, the immunity to process-induced threshold voltage increases with increase in the FE thickness due to a stronger NC effect [14] even in the presence of variability in the FE layer. NC-FinFET based CMOS ring-oscillator circuits were also shown to be more immune to variability effects compared to conventional FinFET circuits. Concerning SRAMs, analysis of the bulk NCFET based SRAM in [28] showed excellent $V_{\rm min}$ reduction, however, variability in the ferroelectric material was not considered.

In the absence of experimental data on the variability in the ferroelectric thickness and parameters, the present work, for the purpose of demonstration, we consider a standard deviation of 5% in $T_{\rm fin}$, L_g, and EOT; as well as in t_{fe}, E_c, P_r relative to their nominal values. The gate workunction (WF) variability is the major contributor to transistor variability at the FinFET based technology nodes, and we have assumed the standard deviation to be 20mV for n-FinFETs. For the p-type devices we apply the same relative standard deviation to the WF. We have considered only local variation of the WF. As shown previously [14], for the NCFETs, the variability in ferroelectric thickness and properties can significantly affect the transistor variability trends. Fig. 5 shows the ensembles of the transfer characteristics of the reference FinFETs, and NC-FinFETs with and without considering variability in the ferroelectric layer thickness and properties at the nominal supply voltage. Further, in order to quantify the impact of variability on the key figures of merit, we calculate the absolute and relative variability in V_t, $I_{\rm ON}$, and $I_{\rm OFF}$. as shown in Fig. 6.

From these figures, it can be seen that the NC-FinFET clearly shows lesser variability compared to the reference FinFET when the variability in the FE layer is turned OFF. The NC-FinFETs have smaller absolute and relative variation in V_t and $\log_{10}(I_{\rm OFF})$. Noticeably, for $I_{\rm ON}$ the absolute variation is larger for NC-FinFETs, but the relative variation (σ/μ) which is more relevant due to the large increase in the mean value of $I_{\rm ON}$, remains smaller. However, when the variability in the FE layer is included, the variability suppression may weaken, especially in case of $I_{\rm ON}$ with an increase in the absolute standard deviation and decrease in the mean value. To understand this, we have plotted the absolute and relative variability in the internal voltage gain (A_V) at different regions of operation including and excluding the variability in the FE layer in Fig. 7. We notice that the impact of the variability in the FE layer is more significant at high gate bias. This can be attributed to the fact that in strong inversion C_{fe} is highly non-linear and its magnitude increases sharply with increasing gate charge, leading to increased fluctuation in capacitance matching and A_V in the presence of ferroelectric variability, in contrast to the low gate bias regime.

For SRAMs, which consist of cross-coupled CMOS inverters, the device output characteristics, particularly the saturation region and the region of transition from linear to saturation, have a direct impact on the magnitude of the noise margins that can be achieved. The role of NDR (negative differential

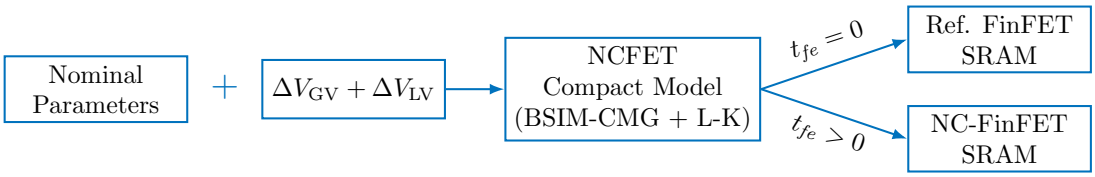


Fig. 4. Flow of the overall methodology used in this work.

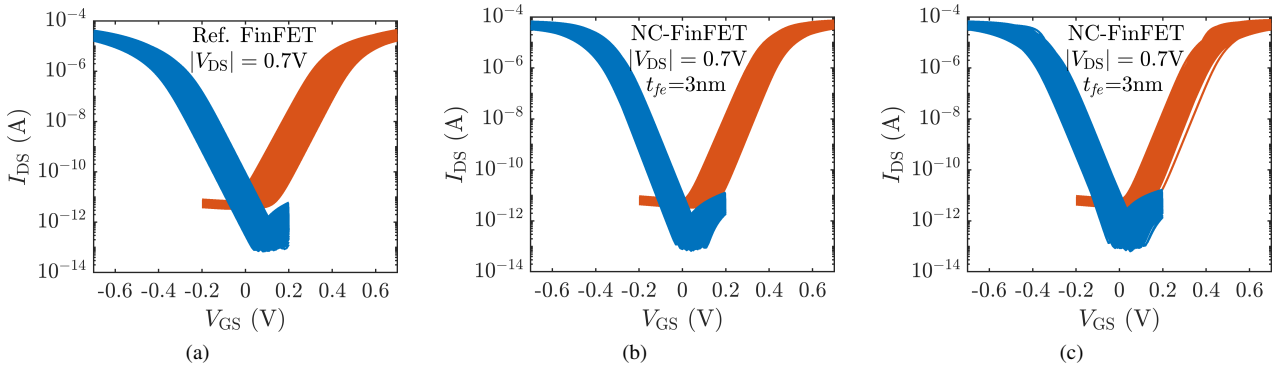


Fig. 5. Statistical ensemble of 5000 $I_{DS} - V_{GS}$ characteristics of n and p type single fin devices obtained from Monte-Carlo SPICE simulations: (a) Ref. FinFETs, (b) NC-FinFETs without considering ferroelectric variation (c) NC-FinFETs considering ferroelectric variation. For the NC-FinFETs t_{fe} = 3nm. V_{DS}=0.7V.

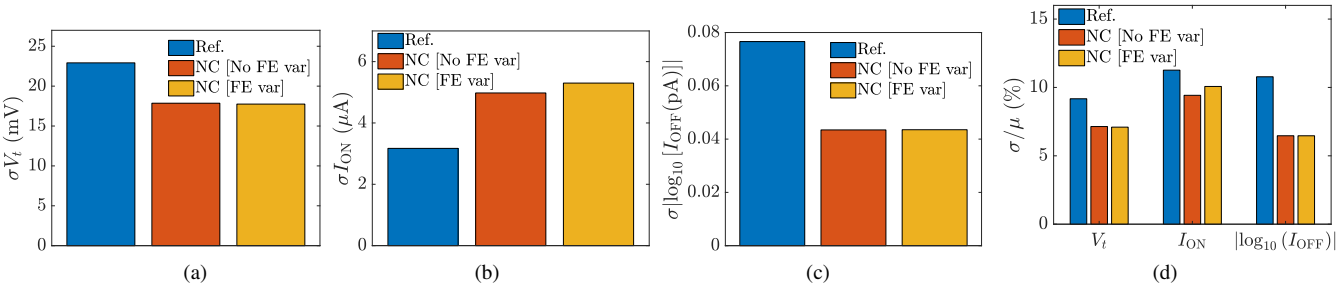


Fig. 6. Standard deviation in (a) threshold voltage, (b) ON-current, and (c) logarithm of OFF-current, extracted from the statistical simulation results of the n type transistors shown in Fig. 5. (d) shows the ratio of standard deviation to the mean (σ/μ). t_{fe}= 3nm.

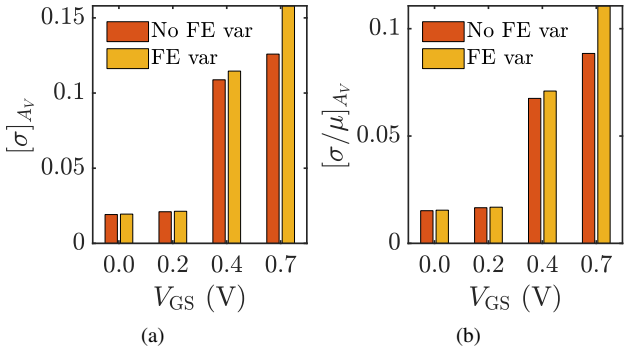


Fig. 7. (a) Standard deviation (σ), and (b) relative standard deviation (σ/μ) in the internal voltage gain (A_V) at four different gate voltages with and without considering ferroelectric variability in the NC-FinFET. The FE variability impacts the A_V fluctuations more strongly in the inversion region. t_{fe}= 3nm.

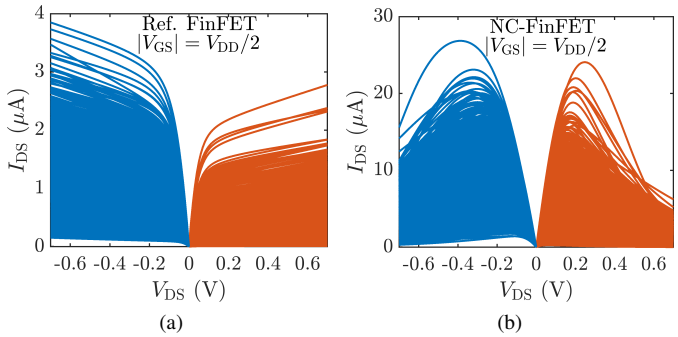


Fig. 8. Statistical ensemble of 5000 $I_{DS} - V_{DS}$ characteristics of n and p type Ref. FinFETs and NC-FinFETs (FE variation enabled) with t_{fe}=3nm. V_{DD}=0.7V.

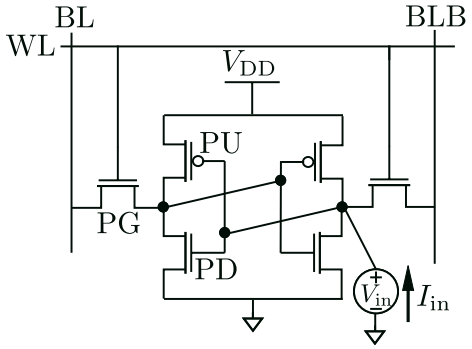


Fig. 9. Schematic of the 6-T SRAM cell including the arrangement for the n-curve measurements. Fin ratio of the transistors, PU:PG:PD = 1:2:3.

resistance) which leads to better noise margins, on nominal NC-SRAMs was investigated in [13]. In Fig. 8(b) we have shown a comparison of the statistical ensemble of $I_{\rm DS} - V_{\rm DS}$ characteristics of n and p type reference FinFETs and NC-FinFETs with FE variation enabled at $V_{\rm GS}$=$V_{\rm DD}/2$. The NC-FinFET current levels are much higher, and the characteristics clearly show the NDR effect, with the characteristics having higher spread in the linear to saturation transition region compared to the high $V_{\rm DS}$ region.

IV. Statistical SRAM Simulations

A. Simulation Setup Description

Variability in the transistor characteristics can have a drastic impact on the circuit operation. In this section we compare the $V_{\rm min}$ of the 6-T SRAM cells designed using NC-FinFETs and the conventional reference FinFETs. We have simulated a high performance SRAM cell, where the number of fins in the Pull-Up (PU), Pass-Gate (PG) and Pull-Down (PD) transistor are in the ratio 1:2:3. We have considered both global and local variation sources as described in section III assuming Gaussian distribution of the parameters. We run Monte-Carlo circuit simulations with a statistical ensemble of 1000 instances of the 6-T SRAM circuit.

We have focused on the evaluation of the read stability and write ability in terms of the critical currents ($I_{\rm crit}$ and $I_{\rm critw}$) under read (BL = BLB =$V_{\rm DD}$) and write conditions (BL = $V_{\rm DD}$, BLB = 0) obtained from the analysis of the respective n-curves [31]. The schematic of the 6T-SRAM cell along with the arrangement for the n-curve measurements is shown in Fig. 9. The n-curves are plots of the current going into the storage node as a function of the applied voltage. The critical current signifying the read stability ($I_{\rm crit}$) is defined as the minimum current that can cause a destructive read, and is given by the peak current from the read n-curve. The critical write-ability current ($I_{\rm critw}$) is obtained as the magnitude of the valley minimum in the write n-curve.

It has been previously shown that for the variability-free case, the NC-SRAM offers higher $I_{\rm crit}$ under READ condition as well as higher $I_{\rm critw}$ under WRITE condition at the nominal supply voltage [13]. Fig. 10 and 11 show the ensemble of $I_{\rm crit}$ and $I_{\rm critw}$ extracted from the circuit simulations for the reference SRAMS, NC-SRAMs without considering the variability in the FE, and NC-SRAMs including the FE variability at $V_{\rm DD}$=0.6V. The NC-SRAM displays higher absolute standard deviations but higher mean values as well, and as a result yields smaller relative standard deviation (σ/μ) for both $I_{\rm crit}$ and $I_{\rm critw}$. The inclusion of FE variability leads to an increase in the standard deviation and a reduction in the mean values of the metrics relative to the case when FE layer is treated as variability-free. This is further illustrated in Fig. 12 which shows the probability distribution of $I_{\rm crit}$ at $V_{\rm DD}$=0.6V for the reference SRAM and the NC-SRAM with t_{fe}=3nm.

B. $V_{\rm min}$ Analysis

$V_{\rm min}$ is defined as the minimum supply voltage required for reliable SRAM cell operation. The methodology adopted for $V_{\rm min}$ calculation is as follows: We calculate $N_{\sigma,Fail} = \mu/\sigma$ as $V_{\rm DD}$ is varied. Here μ and σ are the mean value and standard deviation of $I_{\rm crit}$ and $I_{\rm critw}$ obtained from 1000 Monte-Carlo runs in the circuit simulator. A target $N_{\sigma,Fail}$ is then set. In this work, target $N_{\sigma,Fail}$ has been set to 5.4. The $V_{\rm DD}$ corresponding to the target $N_{\sigma,Fail}$ is the $V_{\rm min}$. This procedure is illustrated in Fig. 13 for both cases - with and without including FE variability. $V_{\rm min}$ is calculated corresponding to both $I_{\rm crit}$ and $I_{\rm critw}$. The higher of the $V_{\rm min}$ values obtained from these two metrics is the overall $V_{\rm min}$. $V_{\rm min}$ is critically constrained by both the mean values of these metrics as well as by their statistical spread. Therefore, NC-SRAMs due to the suppressed relative variability are expected to achieve lower $V_{\rm min}$ compared to the regular FinFET based SRAMs. In Fig. 14 we have summarized the relative improvement in $V_{\rm min}^{\rm Read}$ and $V_{\rm min}^{\rm Write}$. Although the inclusion of variability in the ferroelectric layer reduces some of the advantages of NC effect, we still find that the NC-FinFET based SRAMs have an improved $V_{\rm min}$ compared to their conventional FinFET counterparts. Further, we note that there is an expected trade-off between read and write $V_{\rm min}$ and that this particular cell is constrained by read $V_{\rm min}$ which decreases at high t_{fe}.

V. Conclusion

Ferroelectric based negative capacitance FinFETs have been modeled using a self-consistent coupling of the standard BSIM-CMG model of FinFETs with the Landau-Khalatnikov equations. We have explored the impact of different global and local sources of variation at transistor and circuit levels. We have shown that the superior transistor characteristics and reduction in the relative variability in the NC-FinFETs can result in lower $V_{\rm min}$ for NC-FinFET based SRAM cells, enabling aggressive supply voltage scaling. However, we have also found that the variability induced by the ferroelectric layer can diminish the above benefits significantly.

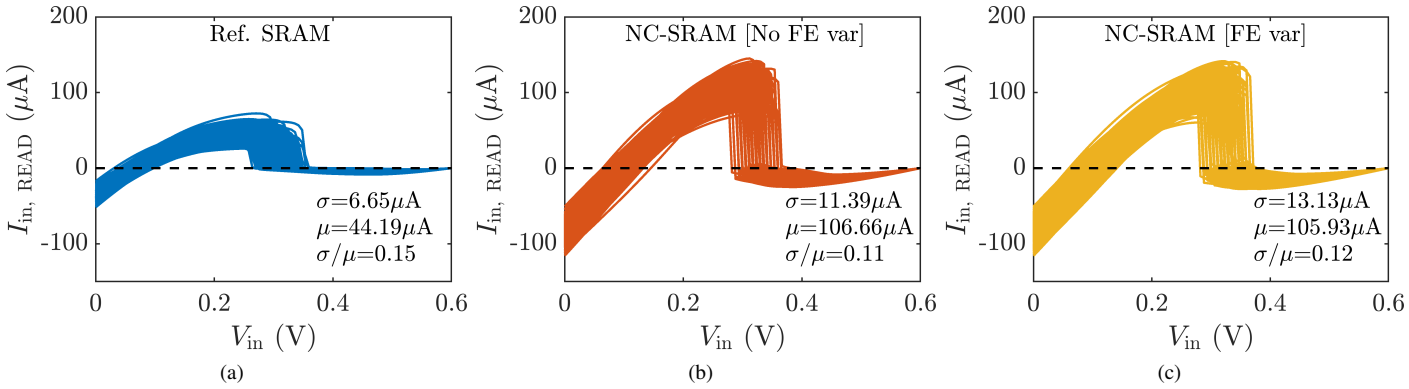


Fig. 10. Read n-curves obtained from the 1000 statistical simulations: (a) Reference SRAM (b) NC-SRAM with no variability in the FE layer (c) NC-SRAM including variability in the FE layer. The standard deviation (σ), mean (μ) and relative standard deviation (σ/μ) are inscribed inside the figures.$V_{\rm DD}$=0.6V

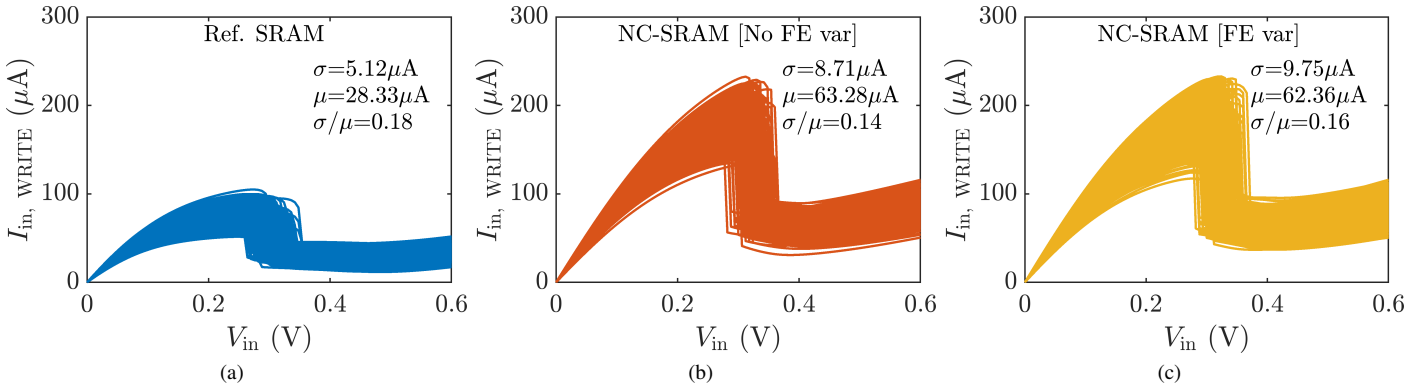


Fig. 11. Write n-curves obtained from the 1000 statistical simulations: (a) Reference SRAM (b) NC-SRAM with no variability in the FE layer (c) NC-SRAM including variability in the FE layer. The standard deviation (σ), mean (μ) and relative standard deviation (σ/μ) are inscribed inside the figures.$V_{\rm DD}$=0.6V

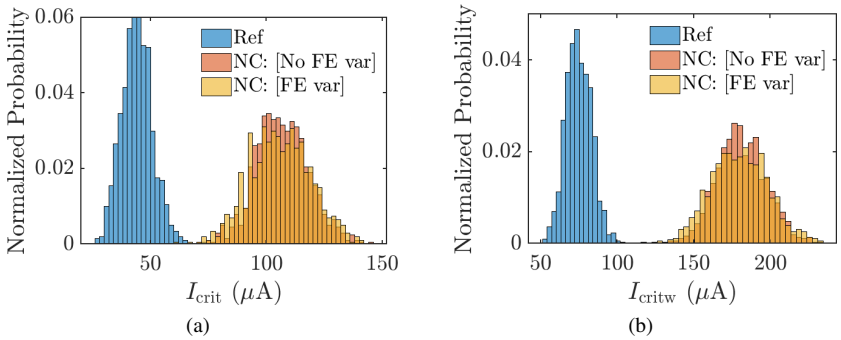


Fig. 12. Histograms showing the probability distribution of (a) $I_{\rm crit}$ and (b) $I_{\rm critw}$ for the reference SRAM and the NC-SRAMs with t_{fe}=3nm (with and without FE variability). $V_{\rm DD}$=0.6V.

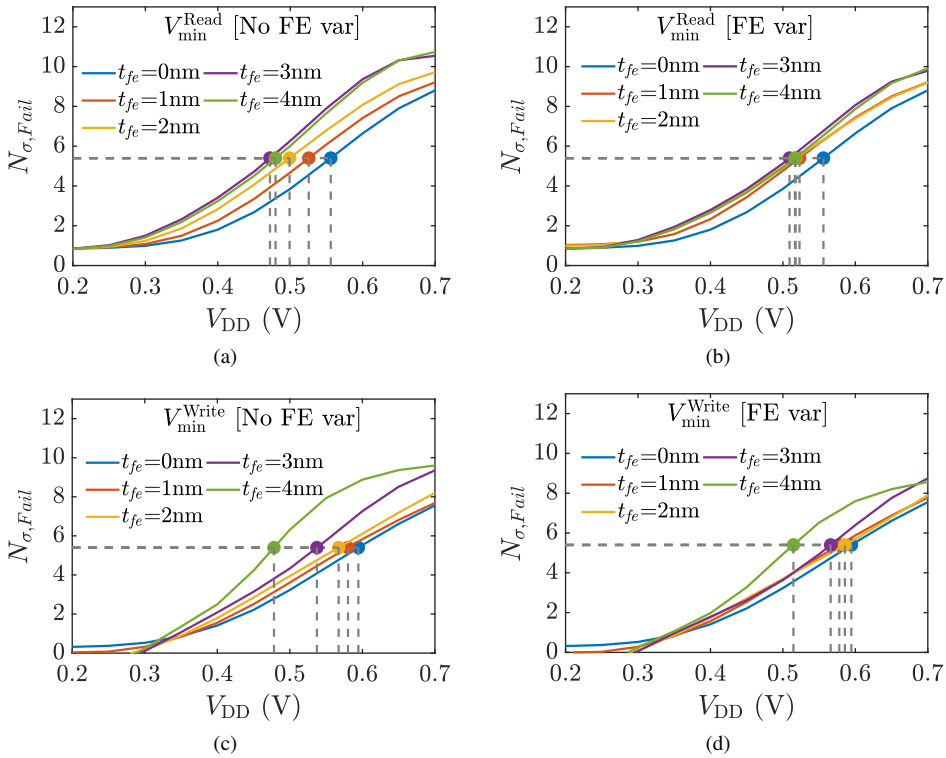


Fig. 13. Graphical illustration of the $V_{\min}$ calculation procedure for different nominal FE thicknesses. (a)-(b): Read $V_{\min}$, and (c)-(d): Write $V_{\min}$. The dashed horizontal line corresponds to $N_{\sigma,Fail} = \mu/\sigma$ of 5.4. The points where the vertical dashed lines meet the V_{DD} axis correspond to the $V_{\min}$.

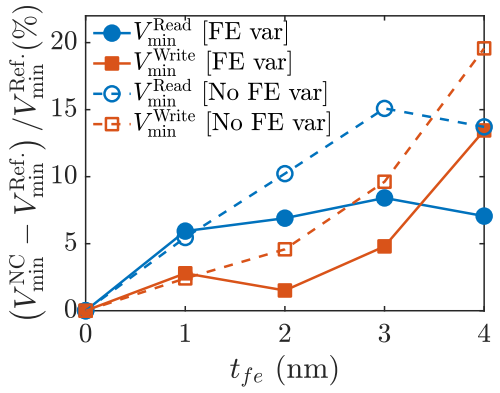


Fig. 14. Comparison of the percentage improvement in read and write $V_{\min}$ values obtained using I_{crit} and I_{critw} with and without considering variation in the ferroelectric for different nominal ferroelectric thicknesses.

REFERENCES

[1] S. K. Gupta and K. Roy, "Device-circuit co-optimization for robust design of FinFET-based SRAMs," *IEEE Design & Test*, vol. 30, no. 6, pp. 29–39, 2013.

[2] X. Zhang, D. Connelly, H. Takeuchi, M. Hytha, R. J. Mears, and T.-J. K. Liu, "Comparison of SOI versus bulk FinFET technologies for 6T-SRAM voltage scaling at the 7-/8-nm node," *IEEE Transactions on Electron Devices*, vol. 64, no. 1, pp. 329–332, 2017.

[3] K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer, "Impact ionization MOS (I-MOS)-part I: device and circuit simulations," *IEEE Transactions on electron devices*, vol. 52, no. 1, pp. 69–76, 2004.

[4] K. Boucart and A. M. Ionescu, "Double-gate tunnel fet with high-κ gate dielectric," *IEEE transactions on electron devices*, vol. 54, no. 7, pp. 1725–1733, 2007.

[5] A. Afzalian, C.-W. Lee, R. Yan, N. D. Akhavan, C. Colinge, and J.-P. Colinge, "Three-dimensional NEGF simulations of constriction tunnel barrier silicon nanowire MUGFETs," *ECS Transactions*, vol. 19, no. 4, p. 229, 2009.

[6] V. Pott, H. Kam, R. Nathanael, J. Jeon, E. Alon, and T.-J. K. Liu, "Mechanical computing redux: Relays for integrated circuit applications," *Proceedings of the IEEE*, vol. 98, no. 12, pp. 2076–2094, 2010.

[7] N. Shukla, A. V. Thathachary, A. Agrawal, H. Paik, A. Aziz, D. G. Schlom, S. K. Gupta, R. Engel-Herbert, and S. Datta, "A steep-slope transistor based on abrupt electronic phase transition," *Nature communications*, vol. 6, no. 1, pp. 1–6, 2015.

[8] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano Letters*, vol. 8, no. 2, pp. 405–410, 2008.

[9] M. Hoffmann, S. Slesazeck, U. Schroeder, and T. Mikolajick, "What's next for negative capacitance electronics?" *Nature Electronics*, vol. 3, no. 9, pp. 504–506, 2020.

[10] W. Cao and K. Banerjee, "Is negative capacitance fet a steep-slope logic switch?" *Nature communications*, vol. 11, no. 1, pp. 1–8, 2020.

[11] Z. Krivokapic, U. Rana, R. Galatage, A. Razavieh, A. Aziz, J.Liu, J.Shi, H. Kim, R. Sporer, C. Serrao, A.Busquet, P. Polakowski, J. Müller, W. Kleemeier, A. Jacob, D. Brown, A. Knorr, R. Carter, , and S. Banna, "14nm ferroelectric FinFET technology with steep subthreshold slope for ultra low power applications," in *IEEE International Electron Devices Meeting (IEDM)*, 2017.

[12] D. Kwon, Y.-H. Liao, Y.-K. Lin, J. P. Duarte, K. Chatterjee, A. J. Tan, A. K. Yadav, C. Hu, Z. Krivokapic, and S. Salahuddin, "Response speed of negative capacitance finfets," in *2018 IEEE Symposium on VLSI Technology*. IEEE, 2018, pp. 49–50.

[13] T. Dutta, G. Pahwa, A. R. Trivedi, S. Sinha, A. Agarwal, and Y. S. Chauhan, "Performance evaluation of 7-nm node negative capacitance FinFET-based SRAM," *IEEE Electron Device Letters*, vol. 38, no. 8, pp. 1161–1164, Aug 2017.

[14] T. Dutta, G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Impact of process variations on negative capacitance FinFET devices and circuits," *IEEE Electron Device Letters*, vol. 39, no. 1, pp. 147–150, Jan 2018.

[15] T. Dutta, V. P. Georgiev, and A. Asenov, "Random discrete dopant induced variability in negative capacitance transistors," in *Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)*, March 2018.

[16] H. P. Lee and P. Su, "Suppressed Fin-LER induced variability in negative capacitance FinFETs," *IEEE Electron Device Letters*, vol. 38, no. 10, pp. 1492–1495, Oct 2017.

[17] T. Dutta, V. P. Georgiev, and A. Asenov, "Interplay of RDF and gate LER induced statistical variability in negative capacitance FETs," in *International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, Sep. 2018, pp. 262–265.

[18] L. T. Clark, V. Vashishtha, L. Shifren, A. Gujja, S. Sinha, B. Cline, C. Ramamurthy, and G. Yeric, "ASAP7: A 7-nm FinFET predictive process design kit," *Microelectronics Journal*, vol. 53, pp. 105–115, 2016. [Online] http://asap.asu.edu/asap

[19] S. Mueller, J. Mueller, A. Singh, S. Riedel, J. Sundqvist, U. Schroeder, and T. Mikolajick, "Incipient ferroelectricity in Al-doped HfO_2 thin films," *Advanced Functional Materials*, vol. 22, no. 11, pp. 2412–2417, 2012.

[20] "BSIM-CMG Technical Manual." [Online] http://bsim.berkeley.edu/models/bsimcmg

[21] G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Designing energy efficient and hysteresis free negative capacitance FinFET with negative DIBL and 3.5X $I_{\rm ON}$ using compact modeling approach," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, Sept 2016, pp. 41–46.

[22] L. D. Landau and I. M. Khalatnikov, "On the anomalous absorption ofsound near a second order phase transition point," *Dok. Akad. Nauk SSSR*, vol. 96, pp. 469–472, 1954.

[23] D. Ricinschi, C. Harnagea, C. Papusoi, L. Mitoseriu, V. Tura, and M. Okuyama, "Analysis of ferroelectric switching in finite media as a landau-type phase transition," *Journal of Physics: Condensed Matter*, vol. 10, no. 2, p. 477, 1998.

[24] M. Hoffmann, B. Max, T. Mittmann, U. Schroeder, S. Slesazeck, and T. Mikolajick, "Demonstration of high-speed hysteresis-free negative capacitance in ferroelectric hf 0.5 zr 0.5 o 2," in *2018 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2018, pp. 31–6.

[25] A. K. Yadav, K. X. Nguyen, Z. Hong, P. García-Fernández, P. Aguado-Puente, C. T. Nelson, S. Das, B. Prasad, D. Kwon, S. Cheema *et al.*, "Spatially resolved steady-state negative capacitance," *Nature*, vol. 565, no. 7740, pp. 468–471, 2019.

[26] M. A. Alam, M. Si, and P. D. Ye, "A critical review of recent progress on negative capacitance field-effect transistors," *Applied Physics Letters*, vol. 114, no. 9, p. 090401, 2019.

[27] M. Lee, S.-T. Fan, C.-H. Tang, P.-G. Chen, Y.-C. Chou, H.-H. Chen, J.-Y. Kuo, M.-J. Xie, S.-N. Liu, M.-H. Liao *et al.*, "Physical thickness 1.x nm ferroelectric HfZrOx negative capacitance FETs," in *IEEE International Electron Devices Meeting (IEDM)*, 2016, pp. 12.1.1–12.1.4.

[28] T. Dutta, V. P. Georgiev, and A. Asenov, "$V_{\rm min}$ prediction for negative capacitance MOSFET based SRAM," in *Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)*, Sept. 2020.

[29] "HSPICE User Guide," *Synopsys, Inc. Mountain view, CA, USA*.

[30] D. D. Lu, C.-H. Lin, A. M. Niknejad, and C. Hu, "Compact modeling of variation in FinFET SRAM cells," *IEEE Design & Test of Computers*, vol. 27, no. 2, pp. 44–50, 2010.

[31] E. Grossar, M. Stucchi, K. Maex, and W. Dehaene, "Read stability and write-ability analysis of SRAM cells for nanometer technologies," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 11, pp. 2577–2588, Nov 2006.