

Review

CORNERSTONE's Silicon Photonics Rapid Prototyping Platforms: Current Status and Future Outlook

Callum G. Littlejohns ^{1,*}, David J. Rowe ¹, Han Du ¹, Ke Li ¹, Weiwei Zhang ¹, Wei Cao ¹, Thalia Dominguez Bucio ¹, Xingzhao Yan ¹, Mehdi Banakar ¹, Dehn Tran ¹, Shenghao Liu ¹, Fanfan Meng ¹, Bigeng Chen ¹, Yanli Qi ¹, Xia Chen ¹, Milos Nedeljkovic ¹, Lorenzo Mastronardi ¹, Rijan Maharjan ², Sanket Bohora ², Ashim Dhakal ², Iain Crowe ³, Ankur Khurana ⁴, Krishna C. Balram ⁴, Luca Zagaglia ⁵, Francesco Floris ⁵, Peter O'Brien ⁵, Eugenio Di Gaetano ⁶, Harold M.H. Chong ⁷, Frederic Y. Gardes ¹, David J. Thomson ¹, Goran Z. Mashanovich ¹, Marc Sorel ⁶ and Graham T. Reed ¹

- ¹ Optoelectronics Research Centre, University of Southampton, Southampton SO17 1BJ, UK; D.Rowe@soton.ac.uk (D.J.R.); h.du@soton.ac.uk (H.D.); kl@ecs.soton.ac.uk (K.L.); weiwei.zhang@soton.ac.uk (W.Z.); Wei.Cao@soton.ac.uk (W.C.); T.Dominguez_Bucio@soton.ac.uk (T.D.B.); xingzhao.yan@soton.ac.uk (X.Y.); m.banakar@soton.ac.uk (M.B.); d.t.tran@soton.ac.uk (D.T.); Shenghao.Liu@soton.ac.uk (S.L.); F.Meng@soton.ac.uk (F.M.); Bigeng.Chen@soton.ac.uk (B.C.); Y.Qi@soton.ac.uk (Y.Q.); xia.chen@soton.ac.uk (X.C.); m.nedeljkovic@soton.ac.uk (M.N.); Lorenzo.Mastronardi@soton.ac.uk (L.M.); f.gardes@soton.ac.uk (F.Y.G.); d.thomson@soton.ac.uk (D.J.T.); g.mashanovich@soton.ac.uk (G.Z.M.); g.reed@soton.ac.uk (G.T.R.)
- ² Biophotonics Lab, Phutung Research Institute, Goldhunga, Tarakeshor-5, Kathmandu 44611, Nepal; rm@pinstitute.org (R.M.); sb@pinstitute.org (S.B.); ad@pinstitute.org (A.D.)
- ³ Department of Electrical and Electronic Engineering and Photon Science Institute, University of Manchester, Manchester M1 3BB, UK; iain.crowe@manchester.ac.uk
- ⁴ Department of Electrical & Electronic Engineering, University of Bristol, Bristol BS8 1UB, UK; ankur.khurana@bristol.ac.uk (A.K.); krishna.coimbatorebalram@bristol.ac.uk (K.C.B.)
- ⁵ Photonics Packaging Group, Tyndall National Institute, T12 R5CP Cork, Ireland; luca.zagaglia@tyndall.ie (L.Z.); francesco.floris@tyndall.ie (F.F.); peter.obrien@tyndall.ie (P.O.)
- ⁶ School of Engineering, University of Glasgow, Glasgow G12 8LT, UK; Eugenio.DiGaetano@glasgow.ac.uk (E.D.G.); marc.sorel@glasgow.ac.uk (M.S.)
- ⁷ Electronics and Computer Science, University of Southampton, Southampton SO17 1BJ, UK; hmhc@ecs.soton.ac.uk
- * Correspondence: c.littlejohns@soton.ac.uk

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Featured Application: The CORNERSTONE silicon photonics rapid prototyping service can be used by academic and industry researchers alike. The platform targets those who require flexibility in their fabrication process flows for applications in datacoms, metrology, sensing and more.

Abstract: The field of silicon photonics has experienced widespread adoption in the datacoms industry over the past decade, with a plethora of other applications emerging more recently such as light detection and ranging (LIDAR), sensing, quantum photonics, programmable photonics and artificial intelligence. As a result of this, many commercial complementary metal oxide semiconductor (CMOS) foundries have developed open access silicon photonics process lines, enabling the mass production of silicon photonics systems. On the other side of the spectrum, several research labs, typically within universities, have opened up their facilities for small scale prototyping, commonly exploiting e-beam lithography for wafer patterning. Within this ecosystem, there remains a challenge for early stage researchers to progress their novel and innovate designs from the research lab to the commercial foundries because of the lack of compatibility of the processing technologies (e-beam

lithography is not an industry tool). The CORNERSTONE rapid-prototyping capability bridges this gap between research and industry by providing a rapid prototyping fabrication line based on deep-UV lithography to enable seamless scaling up of production volumes, whilst also retaining the ability for device level innovation, crucial for researchers, by offering flexibility in its process flows. This review article presents a summary of the current CORNERSTONE capabilities and an outlook for the future.

Keywords: silicon photonics; silicon-on-insulator; waveguides; modulators; mid-infrared; silicon nitride; integration; multi-project-wafer; rapid prototyping; foundry; fabrication; germanium-on-silicon; suspended silicon; MEMS

1. Introduction

Silicon photonics is the manipulation of light (photons) in Si based substrates in a comparable manner to electronics is the manipulation of electrons in Si based substrates [1,2]. Using light to transfer and manipulate data has many key advantages, most notably bandwidth and power. In addition, using Si as the substrate enables integration with electronics technology using the existing state-of-the-art complementary metal oxide semiconductor (CMOS) infrastructure.

Si photonics research and commercial markets have grown exponentially in the last decade. The Si photonic integrated circuit (PIC) industry is predicted to be worth \$3.9 B by 2025, with \$3.6 B of this market expected to be data center transceivers [3]. However, in recent years Si photonics has expanded into new application areas including sensing for healthcare and environmental applications, quantum photonics for computing and communication applications, imaging for light detection and ranging (LIDAR) and spectroscopy applications and artificial intelligence (AI) for agriculture and big data applications, to name but a few.

Mature Si PIC fabrication requires a huge investment of time and development of infrastructure and expertise in the multiple fabrication processes, which are required to build a Si PIC. Only with technological maturity of the processes are complex integrated systems enabled, and this is only achieved with optimized, well controlled fabrication processes. Fortunately, the Si photonics industry can exploit the vast knowledge and infrastructure developed in the electronics industry for the past several decades to achieve the required technological maturity. Over the past several years, many foundries have developed a Si photonics process line and offered access via a multi-project-wafer (MPW) service whereby many users' designs are fabricated on a single wafer, which is then diced into individual chips once fabrication is complete, so that each user only receives their own designs on their chips. This means users can share the fabrication costs thereby lowering the barrier to entry for researchers and fabless companies alike. This foundry model has majorly contributed to the growth and success of Si photonics in recent years [4,5]. There are three categories of Si photonics foundries that have emerged: (1) rapid prototyping foundries typically based in university cleanrooms using e-beam lithography (e.g., AMO [6], Applied Nanotools [7], Australian Si Photonics [8] and INPHOTEC [9]); (2) research foundries typically based on deep-UV (DUV) projection lithography (e.g., AIM Photonics [10], AMF [11], CEA-Leti [12], IHP [13], imec [14], IMECAS [15], Sandia National Laboratories [16] and VTT [17]) and (3) high volume foundries capable of mass production (e.g., CompoundTek [18], Global Foundries [19] and Tower Semiconductors [20]). The core technology offered by these foundries is silicon-on-insulator (SOI), although there is no standardization of the top Si layer thickness [21]. In addition to SOI based technology, several foundries are now offering Si nitride technology, either as a standalone platform or integrated with SOI to address different markets including those that utilize visible wavelengths (e.g., AIM [10], AMF [11], CNM [22], CompoundTek [18], imec [14], Ligentec [23] and LioniX International [24]).

CORNERSTONE [25], a collaboration between the Universities of Southampton and Glasgow, bridges the gap between the e-beam based rapid prototyping foundries, which offer a rapid turn-around using a non-scalable process and the research foundries, which offer scalable processes but typically lack process flexibility, which nurtures device level innovation. CORNERSTONE achieves this by offering an MPW+ service whereby users can customize certain steps within the MPW, with a technology based on scalable deep-UV lithography. This review article presents a summary of the current CORNERSTONE capabilities and an outlook for the future, with the availability of various platforms summarized below in Table 1. All showcases described throughout this review paper are available to all users either through the open source Process Design Kit (PDK) or by contacting CORNERSTONE via their website [25] (with the exception of the showcases described in Sections 2.4.1–2.4.3, which belong to CORNERSTONE users).

Table 1. Summary of CORNERSTONE rapid prototyping capabilities with approximate availability, which is subject to change. Bespoke fabrication batches are also available for all platforms on demand.

Platform	Availability
220 nm silicon-on-insulator (SOI)	2 MPW calls per year for active and/or passive devices
340 nm SOI	1 MPW call per year for passive devices
500 nm SOI	1 MPW call per year for passive devices
Silicon nitride	2 MPW calls per year for passive devices from summer 2021
Germanium-on-silicon	2 MPW calls per year for passive devices from summer 2021
Suspended silicon	2 MPW calls per year for passive devices from summer 2021
Electronic-photonic integration via bonding to SOI	2 MPW calls per year, aligned to SOI calls from summer 2021
Light source integration to SOI via pick-and-place	2 MPW calls per year, aligned to SOI calls from summer 2021
Deep-UV lithography service	On demand

2. Current CORNERSTONE Platforms

This section provides some research highlights from the various SOI platforms that CORNERSTONE currently offers via its MPW service, including both passive [26,27] and active devices [28–32], and other components, which have been demonstrated by research groups around the globe. Since the optimal platform is dependent on the application, CORNERSTONE offers three different top Si overlayer thicknesses: 220 nm, 340 nm and 500 nm, with the 220 nm thickness targeting datacoms applications, the 340 nm thickness targeting low loss applications such as quantum photonics, and the 500 nm thickness targeting mid-IR (MIR) applications. CORNERSTONE technology is based on 248 nm DUV projection lithography enabling feature sizes of 250 nm and above to be patterned, but also offers the unique capability to pattern certain layers using high resolution e-beam lithography with feature sizes of 50 nm and above. This can be exploited, for example, for the fabrication of high efficiency grating couplers (see Section 2.4.1).

2.1. Passive Devices

The passive devices discussed in this section refer to photonic devices, which do not generate, amplify, modulate or detect light. Dielectric optical waveguides [33] based on total internal reflection are the most common light guiding structures for long distance communications, i.e., the optical fiber. Yet unlike optical fibers, Si photonic waveguides are rectangular owing to the planar substrate and the fabrication process. Si waveguides can be partially etched, so-called rib waveguides, or fully etched, so-called strip waveguides, both of which are continuous along the propagation direction. A cross section of these two types of waveguides are schematized in Figure 1a,b, respectively. Optical mode profiles of the fundamental transverse electric (TE) mode are overlapped on the cross sections, which are denoted by the electric field intensity. Theoretically, the rib waveguide has weaker optical confinement than the strip waveguide with the same width and height. Usually, a rib waveguide has more light in the slab layer and therefore has lower propagation loss than a strip waveguide but requires a larger bending radius due to the weaker confinement. When working at telecommunication wavelengths, the propagation loss mostly generates from radiation loss and scattering loss. The radiation loss is

determined by the waveguide dimensions, whilst the scattering loss is mainly caused by waveguide sidewall roughness [34], which is determined by both the lithography process used to define the waveguide in the horizontal and propagation direction, and the etch process used to define the waveguide in the vertical direction.

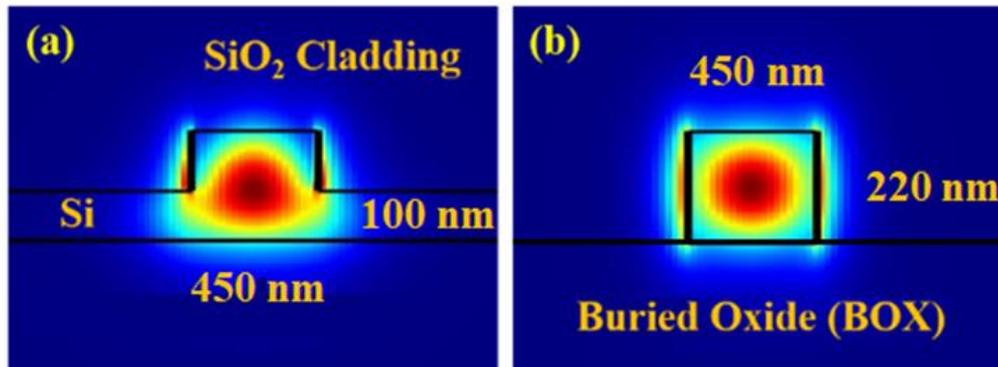


Figure 1. Schematic and transverse electric (TE) mode profiles for a (a) single mode rib waveguide, and (b) single mode strip waveguide, at $\lambda = 1.55 \mu\text{m}$. The Si thickness is 220 nm in both cases, with the slab thickness equal to 100 nm for the rib waveguide. Waveguide width = 450 nm. Note that the x -axis and y -axis scales are not equivalent.

A typical standard single mode (SM) waveguide width is 450 nm for $\lambda = 1550 \text{ nm}$ and 400 nm for $\lambda = 1310 \text{ nm}$, although this is dependent on the Si thickness. Typical insertion loss values of standard CORNERSTONE components for all platforms, which are available in an open-source, license free PDK, are shown in Table 2. As mentioned above, through the use of e-beam lithography CORNERSTONE users have the capability of fabricating high resolution devices, for example, subwavelength grating waveguides [35], slot waveguides [36] and photonic crystal waveguides [37].

Table 2. Typical insertion loss of standard CORNERSTONE devices in various SOI platforms at a wavelength of 1550 nm (TE mode). Single mode (SM) waveguide width = 450 nm. R = bend radius. D = etch depth. MMI = multi-mode interferometer.

Structure	220 nm SOI Platform	340 nm SOI Platform	500 nm SOI Platform
Single mode rib waveguide	3 dB/cm (D = 120 nm)	0.6 dB/cm (D = 140 nm) 2.8 dB/cm (D = 240 nm)	2.6 dB/cm (D = 300 nm)
Single mode strip waveguide	4.0 dB/cm	3.5 dB/cm	-
Rib waveguide 90° bend	0.03 dB (R = 25 μm)	0.02 dB (R = 25 μm)	0.03 dB (R = 25 μm)
Strip waveguide 90° bend	0.011 dB (R = 10 μm)	0.014 dB (R = 10 μm)	-
Grating coupler (uniform)	5.5 dB	5.0 dB	5.0 dB
Grating coupler (apodized) *	3.0 dB	1.0 dB	-
2 × 1 MMI	0.30 dB (strip)	0.20 dB (strip)	0.25 dB (rib)
2 × 2 MMI	0.30 dB (strip)	0.30 dB (strip)	0.25 dB (rib)

* The apodized grating coupler design is only available using e-beam lithography accessible by the multi-project-wafer (MPW)+ mechanism.

By way of comparison with other major foundries from around the world, Table 3 compares some publicly available data for various basic building blocks. Note that all of the compared foundries utilize 193 nm DUV lithography, which is a higher resolution, but more expensive technique.

Table 3. Performance comparison with other major foundries. $\lambda = 1.55 \mu\text{m}$ in all cases. Waveguide dimensions are not specified in the information published by the foundries.

Component	Foundry		
	AMF (220 nm SOI)	CEA-Leti (310 nm SOI)	Imec (220 nm SOI)
Rib waveguide	<1.5 dB/cm (waveguide configuration not specified)	<4.5 dB/cm	<1.4 dB/cm
Strip waveguide	<4 dB	<5 dB/cm	<0.6 dB/cm
Grating coupler	<4 dB	<2.5 dB	<2.5 dB
Reference	[11]	[12]	[14]

The two types of waveguides (rib and strip) can be integrated together using a rib-to-strip taper, which is fabricated using a two-step self-aligned etching process, the schematic of which is shown in Figure 2. A typical insertion loss of this component is 0.07–0.12 dB when the taper length varies from 50 to 10 μm , respectively.

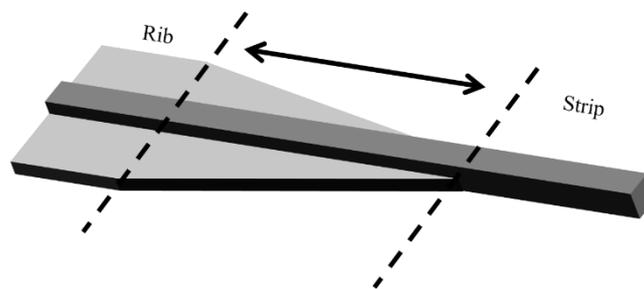


Figure 2. 3D schematic of a rib-strip transition.

Optical coupling both from external laser sources to the PIC chips and from the PIC chips to external detectors can be based on grating couplers or edge couplers. Generally, edge couplers have much wider bandwidth, whilst grating couplers have the flexibility of positioning anywhere on the PIC. Typically, grating couplers have straight teeth with a fixed pitch and filling ratio with feature sizes $> 250 \text{ nm}$ to be compatible with DUV lithography. These grating couplers are fabricated with long tapers with a length of 350 μm to taper from the coupler width of 10 μm to the SM waveguide width. A coupler width of 10 μm is used to closely match the mode profile of the optical beam exiting the fiber, which is used to input/output light. Alternatively, focusing grating couplers [38] have a much smaller footprint whilst maintaining compatibility with DUV lithography. If pursuing ultrahigh coupling efficacy, taking the advantage of e-beam lithography compatibility in CORNERSTONE, one can make subwavelength and apodized grating couplers [39,40] (also see Section 2.4.1). The 1 dB bandwidth of both types of grating coupler design is typically about 35 nm. As for edge couplers, inverse taper couplers [41] are the most common, but these require accurate polishing of the waveguide facets for optimal coupling efficiency, yielding an approximate coupling efficiency of 2 dB per coupler with an inverse taper width of 200 nm measured in a wavelength range of 1265–1355 nm.

Beam splitters/combiners are key components in a PIC, for example to form Mach–Zehnder interferometers (MZIs) for use in switching networks [42] for programmable photonics applications [43]. Three of the most commonly used beam splitters/combiners are multimode interferometers (MMIs), which are based on the self-imaging mechanism [44,45], Y-splitters [46] and directional couplers (DCs) [47]. Generally, MMIs are more robust than both Y-splitters and DCs because they do not require accurately defined features. However, Y-splitters have a wider bandwidth and a smaller footprint, and DCs can be easily tuned to achieve arbitrary power splitting, for example for tapping off a fraction of the power (e.g., 5%) for a reference measurement or test point.

Wavelength-division (de)multiplexers (WDM) are irreplaceable components to transport large volumes of data. Common WDMs in Si photonics are the angled-MMI (AMMI) [48], arrayed waveguide grating (AWG) [49] and planar concave grating (PCG) [50], but all these devices have large footprints.

Generally, AMMIs are easier to design and have lower loss, yet on the other hand they usually have fewer channels. However, the channel count can be increased by interleaving two devices [51]. Furthermore, the AMMI can be operated bidirectionally (BAMMI) so that any drift in the device performance either from fabrication tolerances or from temperature fluctuations during operation are balanced on both the multiplexor (MUX) and de-MUX [52], as shown in Figure 3.

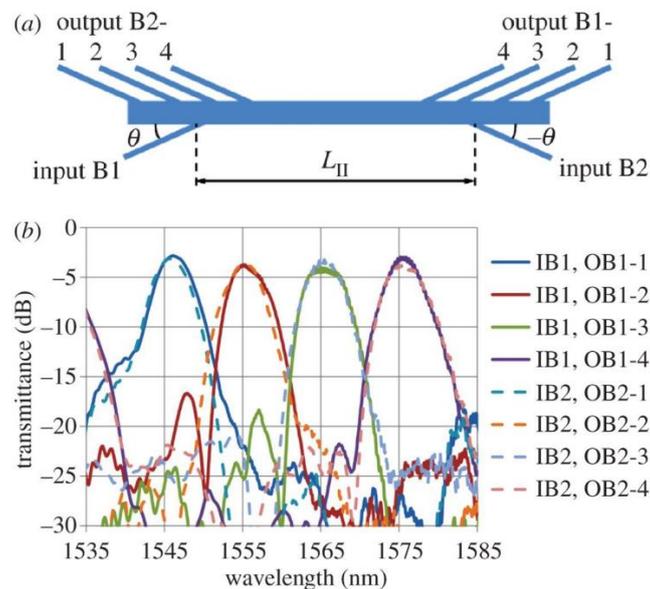


Figure 3. Bidirectional angled multimode interferometer (MMI) showing the (a) top-view device schematic and (b) measured device performance (reprinted from [52], Royal Society, 2015).

Photonic components with optical resonance are also commonly used in Si photonics platforms. For example photonic crystal cavities (PhC) [37] with a quality factor (Q -factor) as high as 600,000 have been experimentally measured on the SOI platform [53], or Fabry–Pérot (FP) cavities formed by Sagnac loops [54] or microring resonators [55] with Q -factors measuring several tens of thousands.

Many of the above mentioned components are available in an open source, license free CORNERSTONE standard design library [25], along with parametric components which are accessible in the CORNERSTONE PDK using Luceda Photonics' IPKISS software [56], e.g., parametric ring resonators and racetrack resonators with both an all-pass-filter and add-drop-filter. In order to facilitate circuit designers, the CORNERSTONE team is in the process of adding component models to their PDK.

2.2. Thermal Phase Shifters

The high thermo-optic coefficient of Si [57] can be both advantageous and disadvantageous for a PIC designer. For resonant devices in particular, the high thermo-optic coefficient typically requires temperature control to maintain the stability of the device, which introduces additional power consumption [58]. Alternatively, several athermal resonant device designs have been explored by other groups, but these typically deviate from standard CMOS processes [59].

On the other hand, the high thermo-optic coefficient of Si means that efficient thermal phase shifters can be fabricated on SOI substrates, typically using TiN based heaters [60]. The efficiency of the phase shifter is largely dependent on thermally isolating the Si waveguide structure so that the heat generated in the TiN heater is confined to the waveguide and does not dissipate through the substrate. This is demonstrated in Figure 4, which shows the electrical power required to achieve a pi phase shift reducing from $19.4 \text{ mW}/\pi$ for a rib waveguide configuration (Figure 4b) to $8.4 \text{ mW}/\pi$ for a strip waveguide configuration (Figure 4a). This is based on a $200 \mu\text{m}$ long, 600 nm wide and 50 nm thick TiN heater filament layer with Al + Au heater contact pads. The flip-side to the higher thermal isolation of the strip waveguide configuration is that the device has a lower switching speed

of 54 kHz compared to 69 kHz for the rib waveguide configuration (Figure 4c). Other groups have investigated methods of further improving the heater efficiency, for example by undercutting the Si substrate, which can result in a 50× improvement [61].

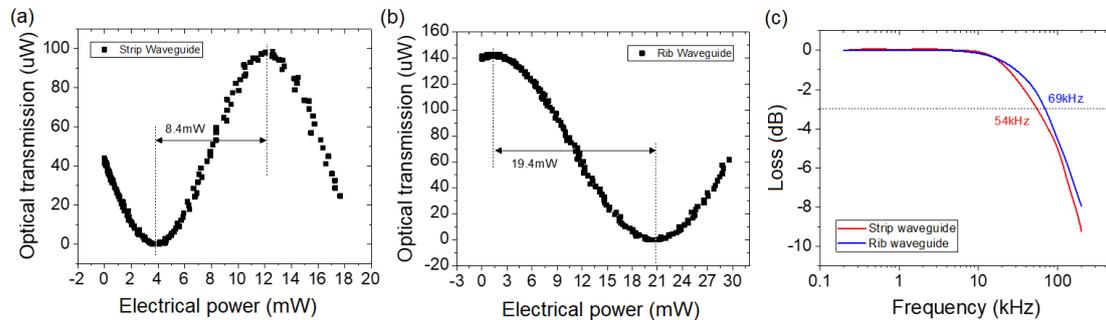


Figure 4. Typical performance of thermal phase shifters for (a) strip waveguide configuration, (b) rib waveguide configuration and (c) switching speed for both waveguide configurations.

2.3. Carrier Based Modulators

For datacom applications, high speed transmission is essential, for which a modulator is required to encode the electronic signal onto an optical carrier from a continuous laser source. Most high speed modulators in Si photonics are carrier based, exploiting the plasma dispersion effect [62,63]. A schematic of a typical Si carrier depletion modulator based on an MZI is illustrated in Figure 5. Due to the adverse effects of any *pn* junction misalignment [64], CORNERSTONE uses a self-alignment doping strategy [65] for the junction formation inside the Si rib waveguides. The *n*-type phosphorus implantation angle is set to 45° followed by −7° to implant a small region of *n*-type Si in the waveguide rib region, which is initially *p*-type doped by boron implantation. Using such an approach, the junction position is defined by the implantation energy as opposed to the lithography alignment accuracy (which varies from chip-to-chip on the wafer) because the top of the Si rib is protected by the same hard mask during *n*-type implantation that is used to etch the waveguide. The doping concentration for the *n*-type region is in the range $1.12\text{--}1.65 \times 10^{18} \text{ cm}^{-3}$ (region D and C in Figure 5a, respectively), and the *p*-type region has a doping concentration in the range $2.25\text{--}5.7 \times 10^{17} \text{ cm}^{-3}$ (region B and A in Figure 5a, respectively).

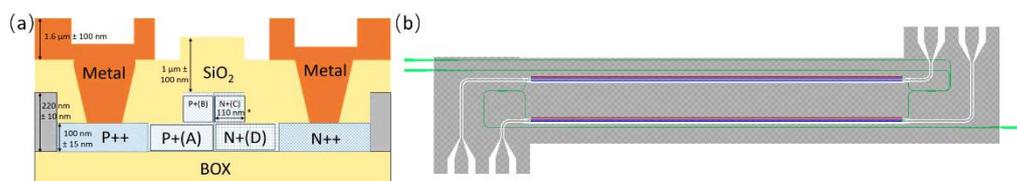


Figure 5. A typical Si Mach-Zehnder interferometer (MZI) depletion modulator (a) cross-section schematic and (b) GDS-II layout.

The $\lambda = 1.55 \mu\text{m}$ push-pull MZI modulator layout is shown in Figure 5b with a phase shifter length of 1.8 mm. A travelling wave electrode is used to ensure copropagation of the radio frequency (RF) and optical signals. The measured optical phase change efficiency changes from 1.35 to 1.9 V·cm (see Figure 6) when the direct current (DC) reverse bias voltage varies from 1 to 9 V.

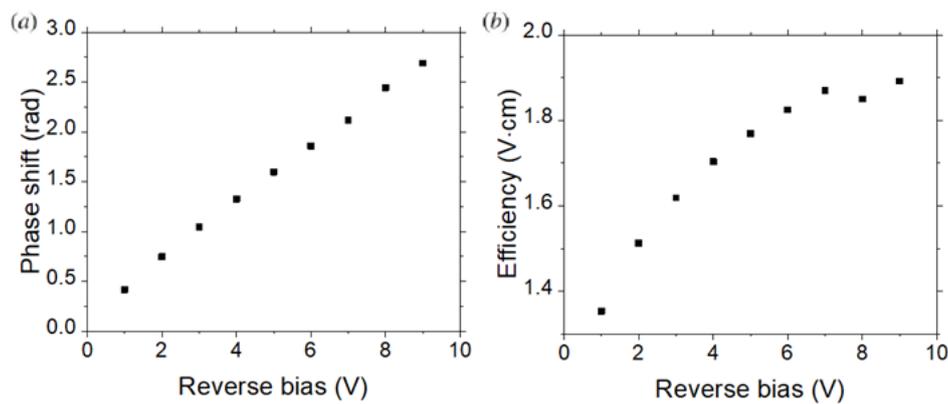


Figure 6. Measured DC performance of a 1.8 mm long Si depletion modulator. (a) Phase shift and (b) modulator efficiency.

A single side RF signal with swing voltage 6 V was applied to a high-speed ground-signal-ground (GSG) probe, with a DC bias of -8 V. The modulator is configured at the quadrature point resulting in a total optical insertion loss of approximately 5 dB. The travelling wave electrode pads were terminated with a 50Ω load. Figure 7 shows the measured optical eye diagram with a 3.9 dB extinction ratio and 40 Gb/s data rate for a 1.8 mm long device.

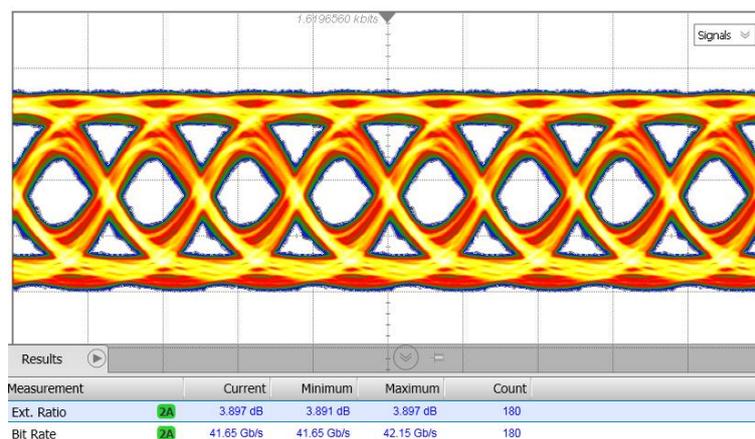


Figure 7. Measured 40 Gb/s optical eye-diagram of a Si photonic carrier depletion modulator.

The SOI platform is also compatible with a wavelength of $2 \mu\text{m}$, where hollow-core photonic bandgap fibers (HC-PBGFs) operate at their lowest predicted loss. This type of fiber exhibits substantially lower loss and nonlinearity than the best single mode fiber (SMF) [66]. Coincidentally, such a wavelength aligns well with the gain spectrum of thulium-doped fiber amplifiers (TDFAs). It therefore opens a new telecommunication window at $2 \mu\text{m}$ wavelength [67]. Such a window, when used in conjunction with spatial division multiplexing (SDM), can offer a revolutionary capacity boost.

SOI based detectors and modulators have both previously been demonstrated at $\lambda = 2 \mu\text{m}$ [68,69]. Here, we further optimized the modulator design and fabricated the device within the CORNERSTONE MPW active device run. The device design is comparable to that shown in Figure 5, with the waveguide width and other passive components optimized for $\lambda = 2 \mu\text{m}$.

Dedicated $2 \mu\text{m}$ equipment was used to characterize the devices, including: a Thorlabs TLK-L1950R tunable laser (1890 nm–2020 nm), an EOT ET-5000 high speed $2 \mu\text{m}$ InGaAs detector (with rated bandwidth of > 12.5 GHz and peak responsivity of 1.3 A/W at $2 \mu\text{m}$); an amplified low speed $2 \mu\text{m}$ InGaAs detector; and Thorlabs SM2000 silica fibers. A bespoke TDFA was also used to boost the optical power at the input.

The modulation efficiency at a reverse bias of 4 V was measured to be 2.89 V·cm at $\lambda = 1950$ nm. Under a DC bias of -4.5 V, with a peak-to-peak alternating current (AC) amplitude of 2 V applied to each arm (operating in push-pull configuration) the device modulates at 10 Gbit/s with an extinction ratio of 12.7 dB, as in Figure 8a. At 20 Gbit/s the extinction ratio is 10.3 dB, as in Figure 8b, and at 25 Gbit/s the extinction ratio is 6.25 dB, as in Figure 8c. The insertion loss of the Mach–Zehnder modulator (MZM) with a 2 mm phase shifter is 4.96 dB, and a similar MZI without doping and metal is also tested to have an insertion loss of 1.25 dB. Due to the bandwidth limit of the detector we were unable to obtain an eye diagram for data rates greater than 25 Gbit/s at 2 μm wavelength.

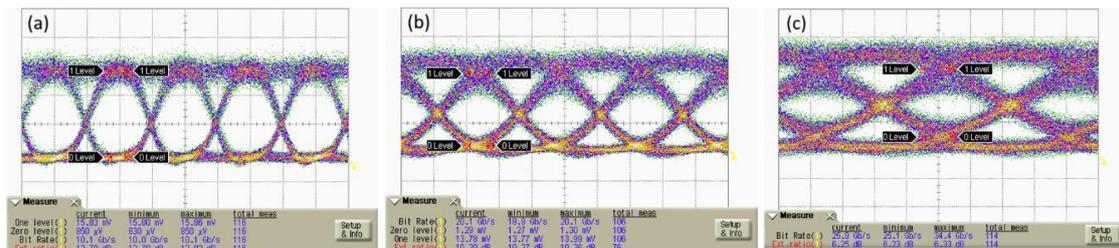


Figure 8. Eye diagram for MZI modulator at 1956.5 nm wavelength. (a) Data rate is 10 Gb/s and extinction ratio is 12.7 dB. (b) Data rate is 20 Gb/s and extinction ratio is 10.3 dB. (c) Data rate is 25 Gb/s and extinction ratio is 6.25 dB.

2.4. CORNERSTONE Partner Highlights

This section presents some research highlights from various CORNERSTONE partners who have used the rapid-prototyping platform for their own research.

2.4.1. CORNERSTONE Partner: Tyndall National Institute, Ireland—High Efficiency Optical Packaging

Photonics packaging is one of the major steps to bringing integrated photonics to huge volume markets mostly due to the high assembly cost and the constraints related with the optical and mechanical connections [70]. Grating couplers (GCs) are an appealing solution to overcome these issues due to the reasonably relaxed in-plane alignment tolerances (± 2.5 μm at 1 dB) and the possibility of placing these structures anywhere on the PICs without the need for a specific customized PIC design [70,71]. The main drawback regarding the packaging of GCs has so far been the mechanical limitations due to the bulkiness and fragility of glass fibers vertically interfaced with the PIC. This light coupling geometry is known as the vertical-fiber scheme (V-Fb), shown in the left panel of Figure 9. A more robust solution is represented by a horizontal light coupling scheme (H-Fb) shown in the right panel of Figure 9. However, up to now, no GCs have been optimized to minimize the insertion loss (IL) for the H-Fb scheme.

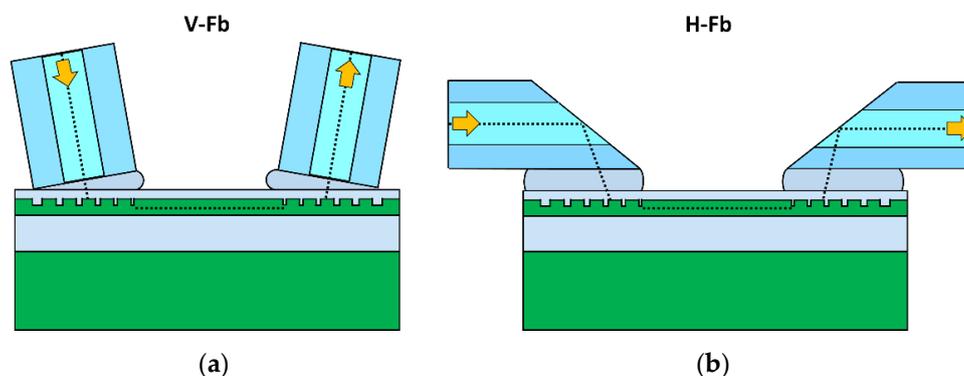


Figure 9. Light coupling geometries for (a) left panel, V-Fb, the vertical fiber scheme; (b) right panel, H-Fb, the horizontal fiber scheme.

To fill this technological gap, we designed GCs optimized in the C-band ($\lambda_c = 1550$ nm) for the H-Fb scheme to be competitive in terms of IL with the most used V-Fb scheme. Apodized GCs [72,73] represent the easiest and most efficient solution to achieve this goal and, consequently, e-beam lithography was targeted as the required technique to resolve the small features (around 55 nm).

A customized particle swarm optimization (PSO) algorithm [74] was implemented inside LumericalFDTD, a commercial software based on a finite difference time domain (FDTD) method. The SOI-platforms under investigation were either the 220 nm or the 340 nm Si thicknesses, which are considered the most interesting at the moment for the majority of applications in integrated photonics. For the sake of completeness, a 340 nm-thick SOI GC was also optimized for the V-Fb, and all the GCs were designed as focusing gratings [71] to reduce their footprints, which is a technological advantage for the scalability of PICs. An epoxy layer was used to secure the fiber position on the PIC surface, matching the refractive index between the core and the top oxide cladding, maximizing the amount of light shined on top of the GC.

The measured IL for both platforms are reported in Figure 10, where panel (a): 220 H-Fb refers to the GC optimized for the 220 nm SOI platform with the H-Fb scheme measuring an $IL(\lambda_c) = 2.5$ dB (56%); panel (b): 340 H-Fb denotes the structure optimized for the 340 nm SOI platform with the H-Fb scheme measuring an $IL(\lambda_c) = 0.8$ dB (83%), and panel (c): 340 V-Fb indicates the optimized structure for the 340 nm SOI platform with the V-Fb scheme measuring an $IL(\lambda_c) = 0.7$ dB (85%).

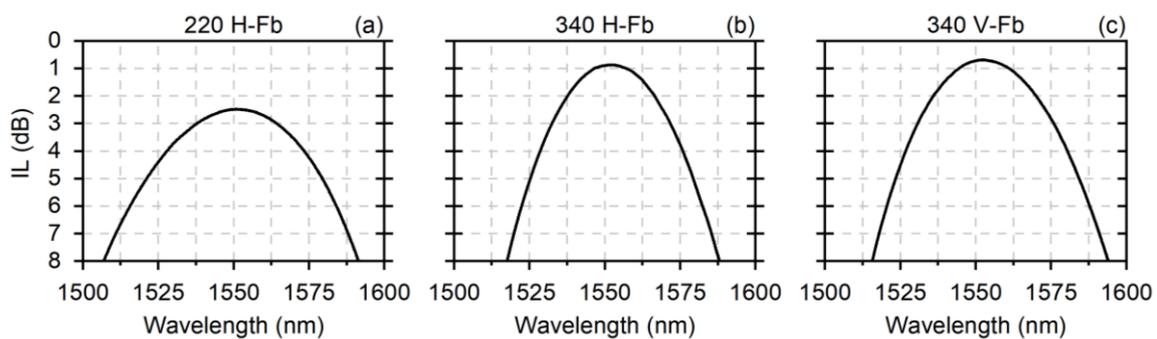


Figure 10. Insertion loss in dB for the apodized focusing grating couplers: (a) 220 nm platform optimized for the H-Fb scheme, (b) 340 nm platform optimized for the H-Fb scheme, and (c) 340 nm platform optimized for the V-Fb scheme.

The 220 nm SOI platform and H-Fb scheme shows an IL slightly higher (0.3 dB) with respect to the theoretical values reported in literature due to a wider mode field diameter proper of the H-Fb scheme. It is well-known that a thicker Si layer shows better performances; thus, for the 340 nm SOI platform the difference is reduced to 0.1 dB. Due to these differences, the H-Fb scheme can be considered a competitive solution for both platforms.

2.4.2. CORNERSTONE Partner: Phutung Research Institute, Nepal and University of Manchester, UK—Apodized Grating Couplers for Optical Coherence Tomography

Medical imaging technologies such as optical coherence tomography (OCT) have a potentially significant role to play in the early diagnosis and progress monitoring of lung disorders such as chronic obstructive pulmonary disease (COPD). Globally there are an estimated 235 million people suffering from COPD at any time, with over 3 million related deaths annually and more than 90% of these in low to middle income countries [75]. The incurable nature of COPD and its increasing latter stage severity means that early diagnosis is vital in reducing the impact of the disease. One way to achieve early diagnosis in suspected COPD cases is to image the wall tissues of the respiratory tract and deep bronchi. Techniques such as OCT offer a relatively inexpensive, alternative imaging modality to X-ray computed tomography (CT) or magnetic resonance imaging (MRI), where access to such facilities may

be limited. However, although OCT can provide the high axial resolution needed for such imaging, current systems are primarily benchtop, incorporating bulky external light sources and fiberoptic based interferometry. Translation of these bulky components to PICs offers the potential to realize a miniaturized, fully integrated OCT system on-a-chip, which provides both further cost benefits and reducing the overall system size to the millimeter range. One of the key requirements of such a PIC based OCT system is the ability to provide a focused spot at the biological sample plane, preferably without adding unnecessary complexity, i.e., by integrating focusing elements entirely within the PIC itself. Recent advances in fiber-based OCT systems have shown that the inclusion of nanophotonic meta-lenses can help suppress optical aberrations, although it is difficult to seamlessly integrate these with PIC platforms [76]. We have recently designed a fully integrated PIC based focusing element [77] that is similar to the circular grating coupler presented in [78].

Our design mitigates the need for completely circular gratings, rather the circumference of the grating structures we employ is 'broken up' into a combination of small arcs, which we refer to as "apodization" of the gratings, azimuthally. This essentially allows the manipulation of phase profiles into the structure as required, and more importantly facilitates a design that allows light to penetrate deeper into the circular grating structure (in a regular continuous grating structure the intensity of light decays exponentially from the entry point). This is critical because, for any integrated focusing component, a means for maximizing the intensity of light reaching the center of the structure, analogous to a conventional optical lens, is preferred. To achieve this, we apodize the gratings such that the arc lengths of the 'feed waveguides' increase exponentially from the outer portion of the circular grating structure.

The 'feed waveguides' and apodized circular grating structures were realized in a single CORNERSTONE fabrication run, from a standard 220 nm SOI starting wafer with a 2 μm buried oxide (BOX) layer. The design incorporates rib structures for our 'feed waveguides', etched to 120 ± 10 nm depth for efficient delivery of the light to the circular gratings, which themselves were etched 70 ± 10 nm. The length of the arc segments was limited only by the design rules of the particular fabrication run, which dictated a 200 nm minimum in the grating layer with a 250 nm minimum gap. The use of DUV lithography for fabrication ensures the PIC based OCT system with fully integrated focusing element can be scaled at acceptably low cost (one of the drivers for wide scale adoption and application, where access to such imaging facilities is severely restricted), due to its compatibility with the CMOS process. Access to the CORNERSTONE program further assisted with low-cost derisking of our prototype designs.

In characterizing the fabricated devices, we used a swept laser source (Santec HSL-20) with center wavelength 1300 nm, bandwidth 100 nm and measured average power output of 13 dBm. Initially, we used the swept laser as a broadband source, coupling the light into the guided mode of the 'feed waveguides' with a standard grating coupler design, which was provided in the CORNERSTONE PDK. The integrated output power from our integrated, apodized focusing device was measured, via a standard graded-index (GRIN) lens (Thorlabs GRIN2913, NA 0.46) mounted on ferruled couplers using a power meter (PM100D) via InGaAs detector (Thorlabs S154C). We determined the spatially resolved emitted power from the device in 2D arrays (laterally and vertically) by moving the GRIN lens point-by-point with a motorized xyz stage.

Prior to fabrication we modeled the device designs with a full 2D-FDTD simulation (using ANSYS/Lumerical FDTD Solutions). We obtained the prerequisite extinction coefficient, which drives the arc-lengths of the gratings, and combined with the fabrication parameter limits, determined the optimized design layout shown in Figure 11. The design includes arcs that extend between the fabrication process limits, i.e., extending from 200 nm, increasing with decreasing radius until the gap between two arcs reached 250 nm. Beyond this point, the gratings merged into a circular grating pattern. The diameter of the outermost circular section was 182 μm , with a grating period of 636 nm. The grating period decreased linearly to 500 nm, which allowed the diffraction angle to vary with

decreasing radius, thus achieving a focused spot. The duty cycle for the periods was kept constant throughout the grating structure at 50%.

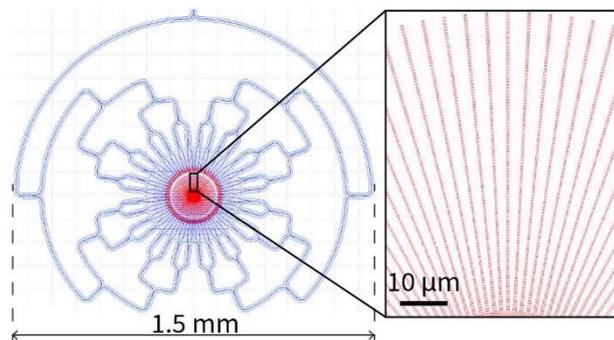


Figure 11. Schematic of the device, showing the details of apodized grating structure.

Figure 12 shows the measured 2D (x-z) power distributions for (a) the apodized and (b) non-apodized grating designs. The fact that the apodization allows light to penetrate deeper into the structure clearly yields a focused spot about 310 μm above the surface of the chip. For the non-apodized device, we see that this resulted in almost all of the light being diffracted within the first 15 μm . Figure 12c shows the measured 2D (x-y) power distribution (at $z = 310 \mu\text{m}$) revealing the spatial distribution of the focused spot, which is 10 μm in diameter. While these early results are limited to integrated power distributions over a broadband of wavelengths, we are currently working on a more complete characterization of the spectral dependence of the apodized focusing grating.

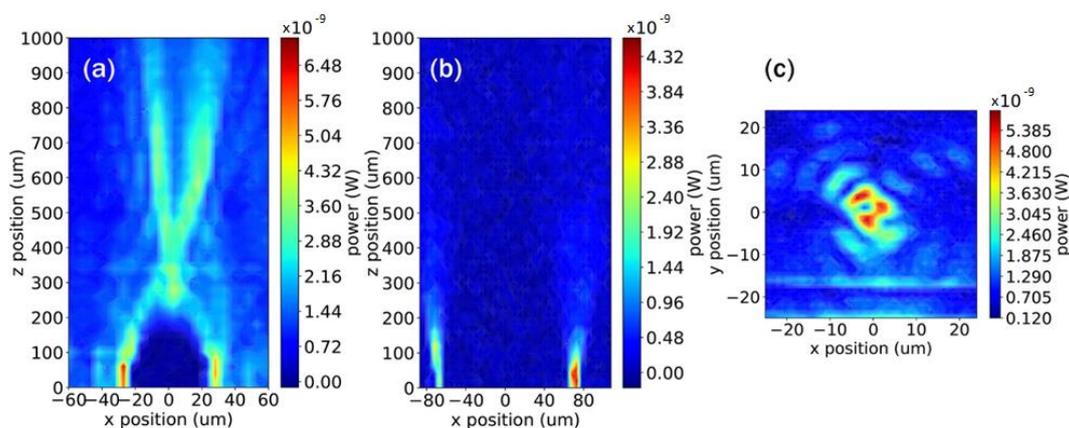


Figure 12. Side views (a,b) and top view (c) of the 2D emitted power distribution from the grating structures. Apodized gratings (a) allow for light to travel further into the device than the non-apodized gratings (b). Top view is the 2D power distribution in the (x-y) plane taken at a height, $z = 310 \mu\text{m}$ above the chip, showing a focus point 10 μm in diameter.

We were able to apodize the gratings in a circular structure, which increased the penetration depth of the light from 15 to 50 μm . This result is promising in developing a fully integrated PIC based focusing element, eliminating the need for external focusing devices in applications requiring off-chip delivery of light, e.g., in OCT or LIDAR. The tight focus size of 10 μm is encouraging, and the seamless integration of such a device indicates significant potential for realizing low cost, PIC based medical technologies such as on-chip OCT.

2.4.3. CORNERSTONE Partner: University of Bristol, UK—Microelectromechanical Systems (MEMS) Switches

The need for efficient, low-loss and scalable phase shifters has long been recognized in Si photonics. Traditional thermal phase shifters common in Si photonics typically dissipate 10 s of mW of electrical power to achieve π phase shifts. A wide variety of applications in areas ranging from integrated quantum photonics, programmable photonic integrated circuits and photonic implementations of artificial neural networks require 10^3 – 10^5 phase shifters on a chip, which makes the power dissipation prohibitive for scalability. Especially for quantum integrated photonics, the need for low loss, low dissipation phase shifters is critical, because these devices need to work at cryogenic temperatures, where the available cooling power is limited to begin with.

Microelectromechanical systems (MEMS) based phase shifters are a potential solution to this problem. MEMS-based switches and phase shifters have long been the standard in the RF domain on account of their low static dissipation. The same advantage applies to their photonic implementations: for example, while a Si thermo-optic phase shifter may consume $10\text{ mW}/\pi$ (Figure 4), and the power must be continuously applied to maintain the desired phase shift, a MEMS phase shifter has achieved 3π of phase shift with negligible continuous power consumption [79]. Although optical MEMS has a long and distinguished history, until recently [80] there has been very little effort at systematically implementing MEMS based devices in Si photonics foundries. This is because MEMS devices require a substrate release step, which is not compatible with current Si photonics manufacturing process flows. While it is possible to build proof of principle devices in academic cleanrooms, the only way to achieve the scale necessary to build 1000 s of these devices (and ensure adequate performance at this scale) is to perform postprocessing on an existing foundry process. At the University of Bristol, we have explored for the past couple of years MEMS based devices that are built around the standard CORNERSTONE passive photonics process. The photonic layers in the device are fabricated using the standard MPW design rules. After the chips arrive at Bristol, we removed the top cladding oxide, overlay metallic electrodes for actuation (using e-beam lithography) and undercut the oxide layer to suspend the MEMS devices.

While the standard Si photonics process is ideal for achieving scalability, it provides a few challenges from a MEMS device perspective. The first challenge is to accurately overlay metallic electrodes, which are not included in the MPW process. Since the Si device layer used for photonics is undoped, to achieve significant beam actuation at reasonable voltages requires accurate electrode overlays. To illustrate this, it is instructive to look at a MEMS based phase shifter implemented in the CORNERSTONE process (Figure 13a). The doubly clamped suspended hammerhead cantilever is pulled toward the signal electrode by applying a DC bias across the signal and ground pads (as the cantilever is deflected away from the microdisk resonator, it changes the effective index of the circulating whispering gallery mode, leading to a shift in the resonant wavelength). Overlaying the pads with metal ensures the field drops predominantly in the actuator gap between the cantilever beam and the signal electrode (Figure 13b). While it is reasonably straightforward to do these overlays with electron beam lithography, a self-aligned electrode process compatible with Si photonics is the more realistic long-term solution.

The second challenge is designing MEMS actuators with relatively large actuation gaps. The minimum feature size in current Si photonics processes is 200 nm, while typical MEMS capacitive gaps, defined by sidewall lithography, can be as small as 50 nm [81]. In the case of this phase shifter, the doubly clamped beam and signal electrode can be approximated by a parallel plate capacitor with a movable plate. The force on the movable plate scales roughly as $(1/d)$ where d is the interelectrode gap. Due to the 200 nm minimum feature size, this phase shifter requires bias voltages 50 V to achieve significant beam deflection (50 nm). The bias voltage could be reduced by making the beam longer, but this could result in unacceptable out-of-plane buckling and would reduce the mechanical resonant frequency. This tradeoff must be accounted for in the design of all MEMS devices. As Si photonics processes continue to improve and the minimum feature size is reduced, we are optimistic

that the deflection voltages can be reduced in the near future. Alternatively, one can move towards out-of-plane actuation, which allows for significantly reduced gaps, although that requires more extensive post-processing.

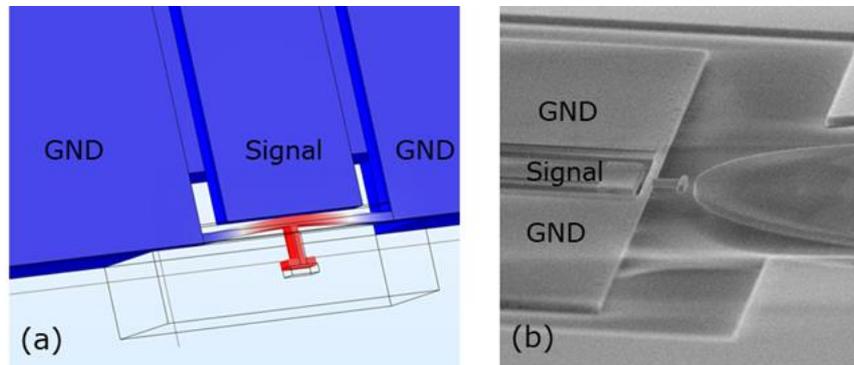


Figure 13. (a) Finite element simulation (FEM) of an electrostatically actuated doubly clamped hammerhead cantilever beam. The beam deflects 50 nm for an applied voltage of 50 V for a 250 nm starting gap. (b) Scanning electron microscope (SEM) image of a fully released MEMS device after metal overlay and oxide removal at Bristol.

While there are significant challenges to implementing efficient MEMS devices in standard unsuspending photonics processes, there are no fundamental reasons to believe that these devices cannot be built at scale. At Bristol, we are focused on extending our work in two main directions: cryogenic operation of MEMS devices and demonstrating MEMS-based phase shifters in waveguide geometry. While microdisk resonators (Figure 13b) are ideal for prototyping these ideas, long term acceptance of the MEMS platform as the default route for building on-chip phase shifters requires implementing phase shifts in non-resonant geometries such as waveguides. The main challenge that waveguides present is the requirement for suspending long ($>50\ \mu\text{m}$) beams while maintaining narrow gaps (200 nm) and avoiding beam buckling upon release. While this might seem at first sight very challenging, the high refractive index of Si enables us to tether rib waveguides without incurring significant additional scattering loss (see [82]) and suspend long tethered waveguide phase shifters without beam buckling (work in progress). We plan to use the new CORNERSTONE suspended Si platform to demonstrate MEMS devices in a foundry environment (see Section 3.3).

2.5. Process Control

As with any fabrication process, there is some degree of variation between devices on the same wafer, and from wafer-to-wafer. CORNERSTONE is a rapid prototyping capability that specializes in flexibility and rapid turn-around. One of the inevitable consequences of this specialty is that the process variation is slightly higher than achievable at other foundries. Nevertheless, with intelligent device design and/or active device tuning (e.g., thermal phase shifter for tuning phase errors in MZIs, which are required even with very precise dimensional control) these potential drawbacks can be largely alleviated. The following tolerances are typical between devices on different wafers, or on different chips from the same wafer, which are measured by critical dimension scanning electron microscope (CD-SEM) or ellipsometry: Si overlayer thickness on the SOI wafers: $\pm 10\ \text{nm}$; etch depth: $\pm 10\ \text{nm}$; feature size width: $\pm 20\ \text{nm}$ and alignment error between layers: $\pm 20\ \text{nm}$ (note that for modulators, a self-aligned process is used to remove the alignment error in the pn junction position within the rib waveguide).

2.6. Intellectual Property

Intellectual property (IP) is an important consideration for designers. All CORNERSTONE users retain full rights to their design IP and are not restricted in the use of IP generated with CORNERSTONE

in any way. By the nature of the open source model, none of the components shared in the PDK have associated IP and can therefore be freely used by designers.

3. Future CORNERSTONE Platforms

This section presents a review of the emerging Si photonics platforms, which will be integrated into CORNERSTONE's MPW service in 2021, and some research highlights from these platforms from the CORNERSTONE partners: University of Southampton and University of Glasgow.

3.1. Silicon Nitride

In recent years, silicon nitride has gained momentum as one of the preferred mid-index CMOS compatible materials for PICs. It is typically used in the form of hydrogenated amorphous films with thicknesses up to 1 μm . One of the most attractive characteristics of Si_3N_4 is its wider bandgap, which sets the lower limit of its transparency window to 450 nm in the visible spectrum and extends it all the way to the MIR [83]. This much larger bandgap results in negligible two-photon absorption (TPA) at 1550 nm, which makes Si_3N_4 a viable and more efficient material for non-linear processes, as it can support higher optical powers than Si with lower non-linear losses and a reasonable non-linear Kerr coefficient [84]. In terms of its physical properties, Si_3N_4 has a thermo-optic coefficient ($10^{-5} \text{ }^\circ\text{C}$), which is one order of magnitude lower than that of Si in the near-infrared regime [85]. As a result, Si_3N_4 devices exhibit spectral shifts as small as 11 pm/ $^\circ\text{C}$ under variable temperature environments [86], which is a feature that makes them attractive for applications that require a high tolerance to temperature variations. When combined with SiO_2 cladding, the refractive index contrast that can be achieved with Si_3N_4 is lower than that of the SOI platform. However, it is enough to achieve a good optical confinement (60–80%) with the added advantage of providing a lower sensitivity to dimensional variations and a higher tolerance to surface roughness [87,88]. Hence, Si_3N_4 devices represent a compromise between the level of integration and a flexible dimensional control, despite their increased footprint.

The different properties discussed above have made Si_3N_4 an ideal candidate for the realization of a various linear and non-linear PICs spanning from visible to mid-infrared wavelengths. Si_3N_4 has been widely used to demonstrate passive linear devices for datacom and visible wavelengths [89,90], including low loss waveguides [90,91], multimode splitters [83,92] and Mach–Zehnder interferometers [93]. Many research groups have worked on (de)multiplexers such as array waveguide gratings [94], angled-multimode interferometers [95,96] and echelle gratings [94,97]. These devices exploit Si_3N_4 to achieve a high tolerance to temperature variations for wavelength (de)multiplexing in datacom circuits and optical spectrometers [94,98]. Si nitride has also become one of the key materials for nonlinear applications and many efforts have geared towards the demonstration of wavelength conversion and optical parametric amplification in the telecom band. Additionally, optical delay lines have been realized to enable digital filtering, pulse shaping and data storage for all optical signal processing [99–101]. Si_3N_4 has also been attractive for frequency comb generation [97,99,102] that can be used as an optical source for high-capacity data transmission [99,103], spectroscopy and optical metrology [104]. Supercontinuum generation on Si_3N_4 has also been explored to obtain ultrabroadband spectra spanning from the visible to the mid-infrared [105,106]. As the transparency window of Si_3N_4 covers the spectrum between 730 and 920 nm, several research efforts have focused on creating highly sensitive biosensors [107–109]. Other biomedical applications have also benefited from Si_3N_4 circuits that can provide optical sources and (de)multiplexers in a compact size [110,111], including super-resolution microscopy [112], point-of-care diagnostics based on flow cytometry [110,113] and optical coherence tomography [114,115].

Many of the demonstrated devices use layers with a thickness of 300 nm and a stoichiometric composition ($n = 2.0$) due to the readily availability of both low pressure chemical vapor deposition (LPCVD) layers with considerably low losses and low-temperature ($<400 \text{ }^\circ\text{C}$) plasma enhanced chemical vapor deposition (PECVD) films more suitable for multilayer integration. This 300 nm thick stoichiometric silicon nitride will become the standard CORNERSTONE thickness for MPW calls,

with a 3 μm thick silicon dioxide under-cladding. Using 300 nm thick PECVD silicon nitride layers, we realized single-mode waveguides fabricated by e-beam lithography with propagation losses below 1 dB/cm in the O-band and close to 1.5 dB/cm in the C-band, as in Table 4 [116].

Table 4. Typical insertion loss of devices demonstrated using e-beam lithography on 300 nm stoichiometric SiN in the O and C telecom bands (TE mode). W = single mode waveguide width. R = bend radius.

Structure	O-band (1330 nm)	C-band (1550 nm)
Single mode strip waveguide	1.0 dB/cm ($W = 900$ nm)	1.5 dB/cm ($W = 1200$ nm)
Strip waveguide 90° bend	0.03 dB ($R = 60$ μm)	0.05 dB ($R = 80$ μm)
Directional coupler	<1.0 dB	<1.0 dB
1 \times 2 MMI	0.1 dB	0.3 dB
MZI	0.4 dB	0.7 dB
4-channel AMMI	<2.0 dB	<2.0 dB

A detailed comparison of silicon nitride technologies available at foundries and research groups around the world can be found in a publication by Muñoz et al. [90]. Moreover, we demonstrated a library of devices working in the O and C telecom bands that are crucial for the fabrication of more complex PICs, including directional couplers, multimode splitters and Mach–Zehnder interferometers (see Figure 14). In particular, we demonstrated 4-channel (de)multiplexers based on angled multimode interferometers with insertion losses <2.0 dB, crosstalk below 20 dB and a high tolerance to temperature variations with wavelength shifts below 10 pm/°C. Finally, we contributed to the realization of fiber-to-chip apodized grating couplers with a staircase teeth profile that exhibited a high directionality with coupling losses of only 1.5 dB and a 3 dB bandwidth of 60 nm in the C-band [117].

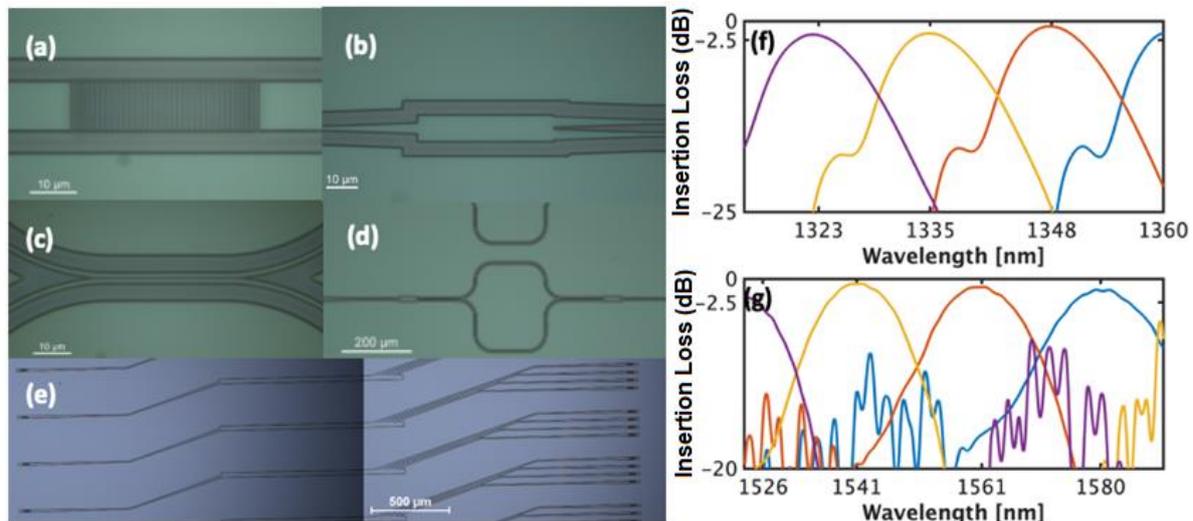


Figure 14. Si nitride device library: (a) grating coupler; (b) multimode interferometer; (c) directional coupler, (d) Mach–Zehnder interferometer; (e) angled-multimode interferometer (reprinted from [95], The Optical Society, 2017); (f) (de)multiplexer response in the O-band and (g) (de)multiplexer response in the C-band.

3.2. Germanium-On-Silicon

MIR group IV photonic devices and systems are well suited to a broad variety of applications including environmental, biological, chemical and pharmaceutical sensing, industrial process control, toxin and contaminant detection, point-of-care diagnostics, communications and astrophysics. The absorption spectra in the fingerprint region (wavelength range 6–25 μm) are comprised of clearly defined peaks for many molecules [118]. Therefore, this region is particularly appropriate for

sensing because it can be used to identify molecular composition and quantify concentration, which is possible because the wavelength of each absorption peak corresponds to the vibrational frequency of a molecular bond and the intensity corresponds to concentration. MIR photonic devices can be used for non-destructive characterization of solid, liquid and gas phase substances with minimal sample preparation. The integration of microfluidics and MEMS systems for repeatable and efficient sample handling is straightforward due to the planar geometry of group IV photonic devices. When combined with the economies of scale associated with the fabrication techniques originally developed by the microelectronics industry, there is clear potential for miniaturized and mass producible MIR photonic sensors for many applications.

SOI is the most mature group IV photonics material platform. However, SiO₂ is highly absorbing at wavelengths greater than 4 μm so the SOI platform is inappropriate for longer wavelength operation [119]. Several alternative material platforms have been investigated to extend the usable wavelength range to cover more of the fingerprint region and so enable a greater variety of applications. These include Si on sapphire (SOS) [120–122], Si on porous Si [123], Si on Si nitride [124], germanium-on-silicon (GOS) in this section [125–128] and suspended Si [129–131] (Section 3.3).

The chief advantages of germanium-based material platforms for MIR photonics are the wide transparency range (2–15 μm) and, in comparison with Si, its higher carrier mobility and larger non-linear effects. The first reported germanium-based MIR photonic devices were Ge-core fibers [132] and Ge slab waveguides on ZnS substrates [133]. Chang et al. have demonstrated GOS waveguides with 2.5–3.0 dB/cm loss at wavelength $\lambda = 5.8 \mu\text{m}$ [126], and GOS multiplexers, Mach–Zehnder interferometers and thermo-optic modulators at $\lambda = 5.3 \mu\text{m}$ [125].

We used two different thicknesses of germanium for device fabrication: 2 μm and 3 μm [134]. Initial investigations were performed using 2 μm Ge layers. The deposition of these layers required less time, which could result in lower cost devices. Latterly, a 3 μm Ge layer was adopted to allow larger waveguide structures; this platform will become the standard CORNERSTONE platform for Ge-on-Si MPW calls. The 3 μm thick Ge layer enabled single mode operation at longer wavelengths and allowed the mode to be more completely confined within the waveguide, thereby reducing its interaction with sidewall roughness and threading dislocations at the Ge-Si boundary, which occur due to the lattice mismatch between Si and Ge.

GOS devices that were 2 μm thick were based on rib waveguides using an etch depth of 1.2 μm and core width of 2.25 μm, which were optimized for single mode operation, with a measured loss of 3 dB/cm in the region $\lambda = 2\text{--}3.8 \mu\text{m}$. The non-linear response of germanium due to TPA was also investigated using GOS waveguides. The TPA non-linearity β_{TPA} was measured to be greater than $1 \times 10^3 \text{ cm/GW}$ in the wavelength range $\lambda = 1.9\text{--}2.3 \mu\text{m}$, which is approximately 1000 times greater than that of Si, and corresponds closely to β_{TPA} measured for bulk Ge [135,136]. The magnitude and ultrafast nature of the TPA nonlinearity mean this behavior can be used to implement a variety of all-optical functions including modulators, switches, logic gates and pulse shapers.

All-optical modulation was demonstrated using GOS waveguides at $\lambda = 2 \mu\text{m}$, where the high β_{TPA} value enabled high speed cross-absorption modulation (XAM). This experiment used a pump-probe setup where a high-power pump induced an absorption dip on a low-power probe that was too weak to induce TPA itself. Increasing pump power was shown to increase modulation depth, albeit with some roll-off due to pump saturation. A maximum extinction ratio (ER) of 8.1 dB was recorded for a coupled input peak power of 10 W, which is the highest published value for any group IV waveguide device [137,138]. Alternatively, due to the fact that free carrier effects are significantly stronger in Ge than Si [139], electrically induced modulation based on carrier injection into 1 mm long PIN devices has been demonstrated [140]. A modulation depth of >35 dB with a 7 V forward bias at $\lambda = 3.8 \mu\text{m}$ was demonstrated when operating as an electroabsorption device, and when operating as an electrorefraction device integrated into an MZI, a $V_{\pi} L$ of 0.47 V cm, driven by a 2.5 V_{pp} RF 60 MHz signal, was demonstrated.

3 μm thick GOS devices were based on rib waveguides using an etch depth of 1.7 μm and core width of 2.7 μm , which were optimized for single mode operation. A scanning electron microscope (SEM) image of a ductile machined end facet of a GOS waveguide is shown in Figure 15. Light was coupled into and out of the devices using surface grating couplers. The etch depth of the grating was kept the same as the waveguide etch depth of 1.7 μm to reduce the number of required fabrication steps. The period (2 μm) and duty cycle (0.5) were optimized for TE mode operation using Lumerical. Subsequently, coupling efficiency has been increased and reflections reduced by using inverse taper excitation. Propagation loss was measured as 0.58 ± 0.12 dB/cm at $\lambda = 3.8$ μm , which is significantly less than the data published for other GOS devices [125–127].

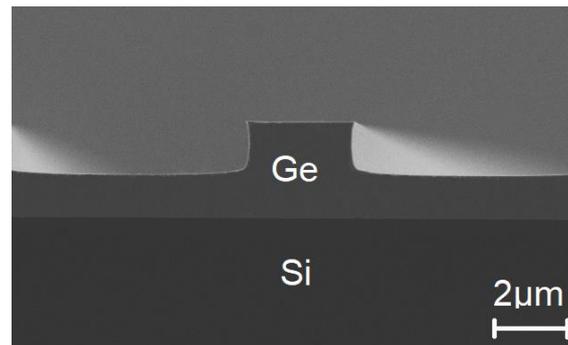


Figure 15. SEM image of a ductile machined end facet of a germanium-on-silicon waveguide.

A wide variety of devices for building PICs have been demonstrated using the 3 μm GOS platform (see Table 5), including MMI splitters [141], angled MMIs [142] and cascaded ring and racetrack resonators [143]. Low loss 1×2 and 2×2 MMIs are discussed here as an example.

Table 5. Experimental performance of 3 μm thick germanium-on-silicon (GOS) photonic components, which will be available in the CORNERSTONE Process Design Kit (PDK).

Device	Wavelength (μm)	Parameter	Value
straight waveguide	3.8	propagation loss	0.58 ± 0.12 dB/cm
1×2 MMI	3.8	insertion loss	0.21 ± 0.02 dB/MMI
2×2 MMI	3.8	insertion loss	0.37 ± 0.07 dB/MMI
straight waveguide	7.575	propagation loss	2.5 dB/cm
1×2 MMI	7.9	insertion loss	0.23 ± 0.04 dB/MMI
racetrack resonator, 2 μm GOS	3.8	insertion loss	1 dB
racetrack resonator, 2 μm GOS	3.8	extinction ratio	17.46 dB
angled MMI, 2 μm GOS	3.8	insertion loss	3 dB
angled MMI, 2 μm GOS	3.8	crosstalk	-10 dB

The optimized 1×2 MMI widths (W), lengths (L) and center-to-center output port separation (S) were $W_{\text{MMI}} = 10$ μm , $L_{\text{MMI}} = 58.2$ μm , $W_{\text{taper}} = 4.75$ μm , $L_{\text{taper}} = 30$ μm and $S = 4.75$ μm . The optimized 2×2 MMI dimensions were identical except for the length of the multimode region, which was $L_{\text{MMI}} = 114$ μm . MMI loss was calculated from the difference in transmission between different numbers of successively linked MMIs. Loss was measured as 0.21 ± 0.02 dB/MMI for 1×2 MMIs and 0.37 ± 0.07 dB/MMI for 2×2 MMIs [141].

GOS long wavelength operation was demonstrated in the wavelength range $\lambda = 7.5$ – 8.5 μm , with a minimum experimentally measured propagation loss of 2.5 dB/cm at $\lambda = 7.575$ μm [144]. An input facet for end-fire coupling was fabricated using ductile machining instead of cleaving, allowing optical-quality end facets with rapid wafer-scale fabrication.

A photonic method was used to measure loss instead of the cutback method. This used a splitting tree of 1×2 MMIs to divide power equally between eight waveguides, which terminated in output

grating couplers. This allowed power to be quantified using a long wavelength infrared camera above the device instead of a conventional detector, thereby avoiding large coupling losses associated with output end-fire coupling. This improved reproducibility by avoiding both the need for consistent end facet preparation for all eight waveguides and the need to align to each waveguide separately. This also improved the tolerance to fabrication errors due to the symmetry of the MMI devices, which in theory have perfectly even splitting ratios.

The future contains a large variety of potential applications that would benefit from the wide transparency and low loss operation of GOS devices. One obvious next step is to extend the wavelength range of the all-optical GOS modulator to demonstrate modulation at higher wavelengths, in order to take full advantage of the TPA window of Ge.

3.3. Suspended Silicon

In photonics Si is most commonly encountered in the SOI platform for optical communications at the telecoms wavelengths of 1.31 μm or 1.55 μm . Si is a viable mid-infrared material given that its usable transparency window extends up to wavelengths of 8 μm ; the factor limiting the wavelength range of SOI devices is the absorption of the buried silica layer above $\lambda = 4 \mu\text{m}$.

Air-clad Si structures offer an alternative to germanium-based material platforms (see Section 3.2) for extending the usable wavelength range beyond that of SOI by elevating a Si waveguide so the propagating mode does not interact with the substrate material. Such structures are implemented in one of two ways: pedestal-type structures [145], which are supported by a thin rib of Si, or suspended structures, where the region under the waveguide is completely removed and the waveguide is supported by lateral bars or membranes [146–148]. Such air-clad platforms avoid using a new material platform and thereby allow the full range of established SOI fabrication techniques to be used.

The major advantage of laterally suspended Si structures is that the suspending structure can be fabricated using lithographically patterned etching. Material underneath the waveguide must be removed using an isotropic etch, whether this is partial (as for pedestal structures) or complete (as for suspended Si devices). This limits the degree of longitudinal patterning that can be achieved underneath the waveguide, for example in the pedestal. Conversely, the lateral supports of a suspended Si can be periodically structured to form a grating [148]. This enables the mode confinement in the waveguide to be optimized so that the sample–light interaction and therefore sensitivity can be adjusted for a particular application.

Three techniques have been used to suspend Si waveguides. First, Si membrane waveguides have been fabricated using an array of holes far from a rib waveguide core to expose the buried oxide (BOX) to hydrofluoric (HF) acid and undercut the Si rib [146]. Second, suspended Si membrane rib waveguides were fusion-bonded to a Si substrate, which had prepatterned air trenches, to provide more support to the waveguide and improve stability [147]. Third, we have demonstrated a method where a subwavelength grating is used to suspend a waveguide core [148]. The grating is etched through the entire upper Si layer to expose the BOX for removal with HF acid. A schematic of this structure is shown in Figure 16.

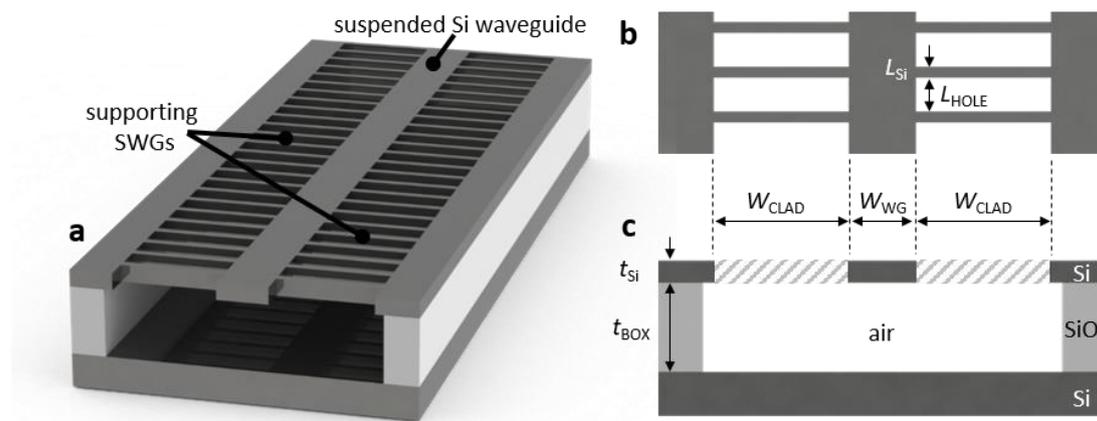


Figure 16. (a) 3D and (b) top view and (c) cross-sectional schematics of a suspended Si waveguide, which is supported by subwavelength gratings.

The subwavelength grating (SWG) supporting structure performs several functions, each with its own constraints. The SWG cladding must be strong and stiff enough to physically support the central waveguide structure without sagging or breaking. The periodicity must be such that it forms a subwavelength structure at mid-infrared wavelengths to suppress any propagation outside of the waveguide. The lateral refractive index can be controlled to optimize mode confinement, which is achieved by varying the longitudinal proportion of Si to air gap (i.e., $L_{Si}:L_{hole}$ in Figure 16b). A higher fraction of Si provides a lower index contrast with the waveguide. Finally, the gaps between the supporting bars allow the circulation of HF acid to selectively etch SiO_2 under the Si to form the undercut.

The suspended Si platform shares the potential for the same variety of mid-infrared applications as the GOS platform, discussed in detail in Section 3.2. The choice of which platform is more suitable is application specific. GOS provides a wider transparency region so is better suited to sensing applications that require access to the longer wavelength part of the fingerprint region. The two platforms have comparable loss although GOS is generally slightly lower. We demonstrated straight suspended Si waveguides with loss of 0.82 dB/cm at $\lambda = 3.8 \mu m$ and 3.1 dB/cm at $\lambda = 7.7 \mu m$ compared with GOS, which exhibited loss 0.58 ± 0.12 dB/cm at $\lambda = 3.8 \mu m$ and 2.5 dB/cm at $\lambda = 7.575 \mu m$.

For fluidic sensing, the sample will occupy the evanescent field both above and below a suspended Si waveguide compared with above but not below a GOS waveguide. This gives an increased light-sample interaction for the suspended Si platform so it could potentially achieve higher sensitivity and lower limits of detection.

Suspended Si is more suitable for microfluidic integration than GOS and can be implemented, for example, by bonding polydimethylsiloxane flow cells to SiO_2 via surface functionalization with oxygen plasma. The bond requires a surface monolayer of SiO_2 so can be formed using native oxide. Conversely GOS cannot be covalently bonded to common microfluidic materials so would require an additional cladding or a compression-sealed flow cell instead.

Suspended Si devices are inherently less robust than their fully supported SOI or GOS counterparts so have a lower limit for high pressure fluidic applications. However, if the SWG structure is not used to provide any flow functionality, careful design of the fluidic circuit should mitigate this disadvantage.

The SWG structure limits the size of suspended particles that could be safely transported within liquid samples. A nanoparticle suspension would likely not be influenced by the SWG, surface effects notwithstanding. However, the microparticulate content of biological samples such as cells, blebs and other microvesicles are of a comparable size to the holes in the SWG cladding and would be likely to become trapped, causing flow problems and interfering with the index contrast between the waveguide and the SWG.

Suspended Si has been used to implement components and devices for operation at both $\lambda = 3.8 \mu\text{m}$ and $7.7 \mu\text{m}$ including 90° bends, S-bends, MMI couplers and grating couplers. Typical device performance metrics are listed in Table 6 for TE polarization. Devices for $\lambda = 3.8 \mu\text{m}$ operation were fabricated using an SOI wafer, which is formed of a 500 nm layer of Si on 3 μm BOX on a Si substrate, which will become the standard CORNERSTONE platform for suspended Si MPW calls. Longer wavelength operation required a thicker 1.4 μm Si layer on top of the buried oxide, which was epitaxially grown on top of standard 500 nm SOI, but this modified thickness will not form part of the standard CORNERSTONE MPW calls.

Table 6. Experimental performance of suspended Si photonic components, which will be available in the CORNERSTONE PDK.

Device	Wavelength (μm)	Parameter	Value
straight waveguide	3.8	propagation loss	0.82 dB/cm
S-bend	3.8	propagation loss	0.01 dB/bend
90° bends	3.8	propagation loss	0.02 dB/bend
2×2 MMI	3.8	insertion loss	<0.3 dB
2×2 MMI	3.8	imbalance	<0.3 dB
straight waveguide *	7.7	propagation loss	3.1 dB/cm
S-bend *	7.7	propagation loss	0.06 dB/bend
90° bends*	7.7	propagation loss	0.08 dB/bend

* Devices operating at $\lambda = 7.7 \mu\text{m}$ using thick SOI will not be part of the standard CORNERSTONE MPW calls.

The future outlook for MIR sensing using the suspended Si platform is broadly similar to that of Ge-on-Si discussed above, albeit with the additional benefits of offering simpler integration with Si MEMS and polydimethylsiloxane (PDMS) microfluidics. One exemplar application would be exploiting the bioanalytical data we have obtained using Fourier-transform infrared spectroscopy (FTIR), including a detailed study of the MIR properties of blood [149]. When combined with comprehensive knowledge of the MIR performance of the GOS and suspended Si platforms, sensitivity can be maximized for blood-based medical diagnostics.

3.4. Electronic–Photonic Integration

Integration of photonics and electronics is one of the key subjects for the further adoption of Si photonics technologies in the marketplace. Traditionally, integration between photonics and electronics is often classified as the physical coupling approaches between the photonics and electronics devices, such as wire-bonding, flip-chip bonding or monolithic integration. However, we believe this subject should be expanded to a synergistic design concept, in which the photonics and electronics devices should be closely codesigned in every possible aspect, including the operation speed, power efficiency, footprint, signal integrity and physical connection approaches. Two of our recent design examples [150,151] demonstrate the advantages of this design philosophy.

3.4.1. Codesign of CMOS Driver and Si Modulator for Si Photonics Transmitters

In our previous work [150], we have presented an example where a carrier depletion based optical modulator is designed in a U-shape MZM configuration allowing access to both the input and termination pads of the MZM on one side of the chip. This allows both ends of the modulator to be electrically connected to the CMOS driver with short bonds. By terminating the travelling wave electrode on the CMOS chip (resistor R1 in Figure 17a), further control and dynamic tuning of the termination impedance is possible allowing fine tuning of the performance. The results shown in [150] were performance-limited by the parasitic effects of the bonding wires that coupled the CMOS driver and Si modulator.

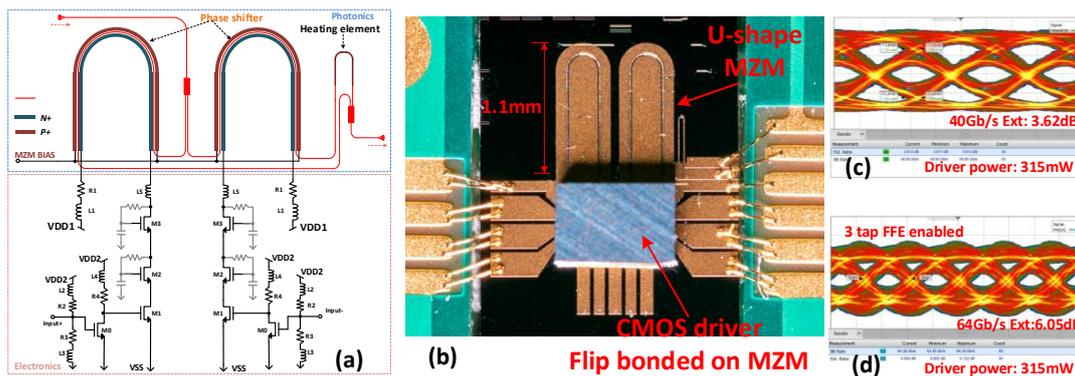


Figure 17. The integrated Si photonics transmitter. (a) Circuit diagram of the Si MZM integrated with the complementary metal oxide semiconductor (CMOS) driver, (b) microscope image of the integrated Si photonics transmitter, (c) measured optical results at 40 Gb/s and (d) measured optical results at 64 Gb/s with 3-tap feed forward equalization (FFE).

More recently, we developed a comprehensive flip-chip bonding process that is compatible with the SOI based CORNERSTONE platforms and will be offered as a standard CORNERSTONE process alongside the MPW calls. CORNERSTONE users will be responsible for the design and sourcing of the electronics chips, which can then be bonded to CORNERSTONE SOI photonics chips. Compatibility of the bonding processes with the new platforms described above (Sections 3.1–3.3) will be confirmed in due course. As shown in Figure 17b, the CMOS driver has been flip-chip bonded onto a 2.47 mm long U-shape carrier depletion modulator, using a modified CORNERSTONE PDK modulator. Measurement results show that the integrated transmitter can operate at 40 Gb/s with an extinction ratio of >3.6 dB (Figure 17c). Based on the 3-tap feed forward equalization (FFE), 64 Gb/s optical eye diagrams can be observed with extinction ratios of >6 dB (Figure 17d).

3.4.2. Codesign of Differential Transimpedance Amplifier and Balanced Photodetector for Si Photonics Receivers

In this work [151], we present the design and characterization of an optical receiver that is composed of a 28 nm CMOS transimpedance amplifier (TIA) and a balanced Si-Ge photodetector (PD). The electrical and optical units were codesigned and packaged, providing fully differential output signals (Figure 18a). The TIA circuit operates with the standard CMOS supply (1.0V). Without using any equalization or digital signal processing (DSP) techniques, the receiver can operate up to 54 Gb/s non-return-to-zero (NRZ) with a bit error rate (BER) of less than the KP4 limit (2.2×10^{-4}) with an optical modulation amplitude (OMA) of -8.6 dBm, whilst the power efficiency was 0.55 pJ/bit (or 0.98 pJ/bit including the output buffer), as shown in Figure 18c. Besides the carefully design and modeling of the optoelectronic circuit, the device packaging process plays a dominant role in enabling the receiver's performance.

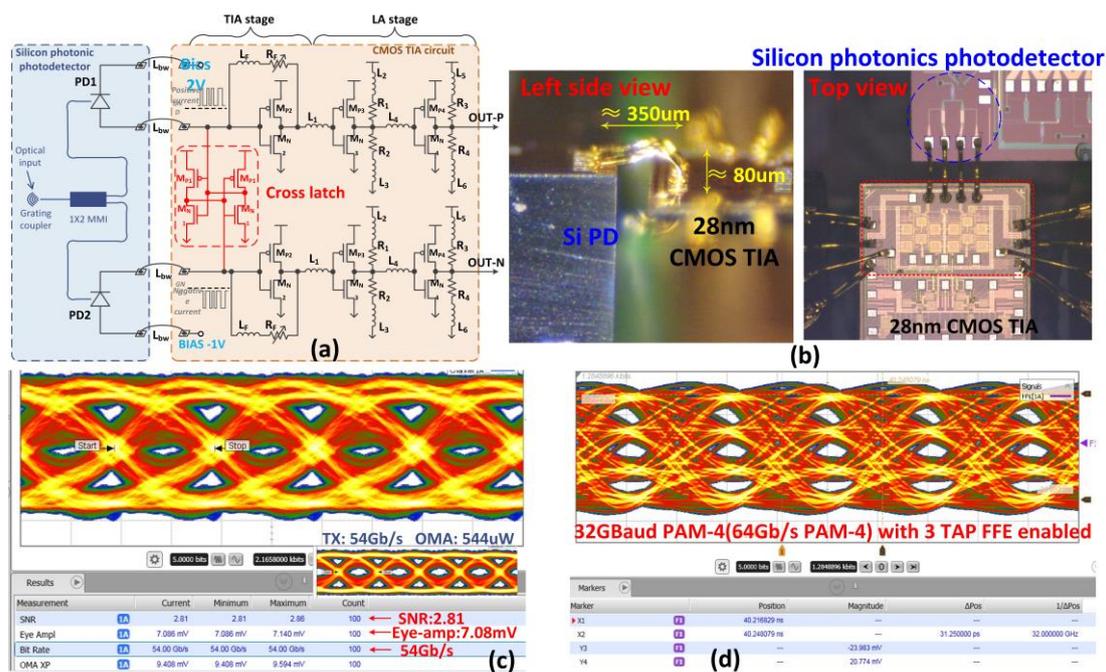


Figure 18. The integrated Si photonics receiver. (a) Circuit diagram of the balanced PD integrated with a CMOS transimpedance amplifier (TIA), (b) microscope image of the Si photonics receiver, (c) measured results at 40 Gb/s OOK and (d) measured results at 64 Gb/s PAM-4 (reprinted from [151], The Optical Society, 2020).

As highlighted in Figure 18, the PD chip and TIA chip were carefully placed within the cavity of a fully custom designed PCB. During the packaging process, the output pads of the PD and input pads of the TIA were precisely aligned using an industry-standard flip-chip bonding machine. Through the use of a programmable ball-bonding machine, the length and height of the bonding loops were established as 350 µm and 80 µm, respectively (Figure 18b). Furthermore, in order to minimize the current spike within the power supply rails, double-wire bonding was applied to the DC power pads within the TIA. Besides the on-off keying (OOK) performance, measurement results also prove that the integrated receiver can detect 64 Gb/s pulse amplitude modulation-4 (PAM-4) signals when the input OMA is -8.2 dBm (Figure 18d).

3.5. Pick-and-Place of Light Sources onto SOI

Although there are a variety of different technologies to integrate III-V active devices on SOI chips, these can be broadly classed into three main groups, namely heteroepitaxial growth, wafer or die bonding and flip-chip integration [152]. Heteroepitaxial growth of III-V semiconductor layers on a Si substrate would provide the ideal route for large scale industrial manufacturing of PICs; however, current technology in this area lacks the required reliability and performance. In fact the large lattice constant mismatch between silicon and III-V materials such as GaAs and InP, and the formation of antiphase domains at the III-V/silicon interface pose major technological challenges that affect the quality of the epitaxial layers [153].

In the wafer or die bonding approach, most commonly called heterogeneous integration, pieces of III-V material are bonded onto a patterned Si wafer followed by substrate removal and then processed using standard lithography tools [154,155]. The two most exploited bonding techniques are covalent molecular direct bonding and adhesive bonding using polymers, each with its own advantages and limitations [156]. Wafer bonding allows for very high accuracy lithographic alignment of the III-V devices as it employs the same registration markers used for the SOI chip fabrication; however, this requires running fully processed silicon PIC wafers through an III-V foundry. An alternative

approach that circumvents this limitation is transfer printing, in which fully fabricated III–V membrane devices are directly transferred and bonded onto the SOI chip [157]. Transfer printing retains the advantages of a full post-fabrication process at the expense, however, of a more complicated III–V fabrication processing that require the release of the III/V membranes from the native substrate, usually achieved through selective wet etching of a sacrificial layer [158]. Additionally, transfer printing does not provide a good heat flow when only Van der Waals forces are used for the bonding. In fact, efficient heat dissipation is a prime requirement of any heterogeneous integration technique as it directly impacts the reliability, lifetime and performance of the III–V active devices. This issue can be mitigated by using a metal, e.g., gold, as a bonding layer [159] or by bonding the membrane directly on the Si substrate after removal of the SiO₂ BOX layer [160,161]. The use of thin III–V membranes in the wafer bonding and transfer printing approaches is ideal to implement vertical mode coupling via efficient adiabatic mode coupling between III/V and SOI waveguides or to design hybrid coupled modes [162–165].

Although wafer bonding technology has substantially progressed in the last decade, hybrid integration by flip-chip bonding III–V active devices onto SOI chips is still the industry standard for the manufacturing of PICs in large markets such as telecoms and data centers [166–168]. In this approach, prefabricated III–V active devices are picked and placed onto silicon photonic chips usually with microgrippers [169,170] and attached to the host substrate via metal-to-metal flip-chip bonding. Crucially, because integration by flip-chip bonding is a post-fabrication technique it allows to independently optimize and prescreen devices fabricated in different foundries, which adds substantial design flexibility, reduces packaging cost and improves device yield. One major requirement of flip-chip integration is an accurate and robust alignment process to minimize the insertion losses that arise by any misalignment between the III/V active devices and the SOI waveguides. From a mechanical point of view, the accuracy of the flip-chip technique can be enhanced via the use of patterned registration markers [171], computer vision registration techniques and active alignment [172]. The design of both the III–V and SOI chips in the coupling region can also be optimized to improve the tolerance to misalignment and minimize the coupling losses [173–175]. Due to these approaches III/V devices flip-chip bonded to SOI have insertion loss as low as 1.1–1.5 dB [176–178].

As detailed in Section 3.1, CORNERSTONE will also offer PIC development on a silicon nitride platform because of the advantages offered by its wide transparency down to the visible spectral range and beyond. The SiN transparency range is well-covered by a variety of III–V compound semiconductors such as aluminium indium gallium nitride (AlInGaN) [179,180], gallium indium phosphide (GaInP), aluminium gallium indium phosphide (AlGaInP) and aluminium gallium arsenide (AlGaAs) [181]. The integration of these III–V active devices on a SiN material platform could be of great impact to several applications in healthcare, imaging and quantum technologies [182]. However, SiN presents additional integration challenges due to its lower refractive index, i.e., $n = 2.0$ for the stoichiometric composition, compared to the III/V materials, in the range of $n = 3–3.6$. This is often mitigated using a mode-matching waveguide between the III/V and the SiN waveguides made by a material with an intermediate refractive index waveguide, such as silicon or polymer. Examples of integration of III/V devices on a SiN platform are reported in the literature for both flip-chip bonding [183–185] and transfer printing [186–188] with an insertion loss as low as 2.1 dB.

CORNERSTONE will offer flip-chip bonding by metal-to-metal thermocompression with submicron alignment. Due to the large demand for telecoms applications, the initial focus will be on InP-based distributed feedback (DFB) lasers and InGaAs photodetectors integrated on an SOI platform operating at a wavelength of 1550 nm. This activity will be supported by the design of suitable waveguide geometries to mitigate the impact of misalignment tolerances and by the establishment of design rules that will ultimately be part of the CORNERSTONE PDK. A key feature of this model is that, provided compliance to design and fabrication rules is followed, users will be able to use the CORNERSTONE capability to integrate any III–V device, which adds a unique level of flexibility to support both established and emerging applications at non-telecom wavelengths.

4. Conclusions

As the adoption of silicon photonics technologies continues to rise, and the global ecosystem to support the expanding market grows in conjunction, there remains a challenge for researchers to fabricate their pioneering and potentially groundbreaking devices using a scalable technology process to accelerate the impact of their innovations and reduce the barriers to market adoption. CORNERSTONE seeks to support such researchers by offering unprecedented fabrication flexibility whilst using a scalable process technology based on DUV lithography.

In this review article, we gave an overview of the current SOI based technologies offered by CORNERSTONE via an MPW service, and presented a summary and motivation for new and emerging technology platforms, which will be made available via an MPW service in the summer of 2021.

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