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PMMA sacrificial layer based reliable debonding of ultra-thin chips after lapping

Yogeenth Kumaresan [1], Sihang Ma [1], Ravinder Dahiya [*]

Bendable Electronics and Sensing Technologies (BEST) Group, University of Glasgow, G12 8QQ Glasgow, UK

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ABSTRACT

Ultra-thin chips (UTCs) are needed to meet the performance and packaging related requirements of flexible electronics and 3D integrated circuits (ICs). However, handling of UTCs (<50 μm thick), particularly after thinning, is a challenging task as the excessive mechanical stresses could lead to cracking. Such damages could be prevented by restricting the stresses to acceptable levels. Herein, we present a new reliable and cost-effective method based on a polymethylmethacrylate (PMMA) sacrificial layer (20 μm-thick). The PMMA layer results in 4 order of magnitude lower stress on UTCs and, as a result, the reliable removal or debonding of UTCs (35 μm-thick) from the glass substrate has been achieved. The distinctive features of the presented method are high reliability and cost-effectiveness (an order of magnitude cheaper) with respect to conventional methods that use UV curable tapes. The UTCs with metal-oxide-semiconductor capacitors (MOSCAPs) devices were also obtained using this approach and were evaluated under different bending conditions. The stable and uniform performance (134 pF) observed under bending conditions demonstrates that the presented technique could be useful for integration of high-performance flexible UTCs on flexible printed circuit boards for various practical application.

1. Introduction

Silicon has been the workhorse material for electronics industry, owing to its excellent electrical and mechanical properties which has led to today's fast computation and communication through high-performance devices and integrated circuits (ICs) [1]. The value addition in silicon-based electronics over the past five decades has mainly come through following the path of Moore's law [2,3]. However, the International Technology Roadmap for Semiconductor suggests that Moore's law may be flattening soon, and a further value addition could come from a vertical growth i.e. 3-dimentional (3D) ICs through the stacking of chips via new form factors such as flexible electronics [4–7]. In this regard, ultra-thin chip (UTC) technology has emerged as a key solution, enabling high density packaging as well as high performance flexible electronic systems [7]. By enabling high-performance flexible electronics, the UTC research is also advancing the innovative solutions such as flexible electronic skin, wearable systems and flat panel displays etc. [8].

The UTCs are typically obtained by thinning the semiconductor wafers from approximately 700 μm to about 50 μm by using technologies such as back grinding, backside lapping, wet etching, dry etching, and chemical mechanical polishing (CMP) [3,9–14]. The back grinding and lapping are mechanical thinning processes, both of which provide high throughput and good flatness [15,16]. Amongst these, the back grinding is the most adopted process. However, compared with back grinding, back lapping employs loose abrasive slurry instead of fixed-abrasive wheels, which provides a gentler thinning process [17]. As a result, it is more effective than grinding for removing wafer waviness that offers a more uniform surface. A key issue that UTCs commonly face during these processes relates to their handling. They become fragile during thinning and it is challenging to remove them from the substrate that holds them during thinning. The thinner the chip or wafer, the more difficult it is to remove or pick from the chuck after thinning [18]. Vacuum tools are often employed to pick and transfer the thin chips to the target substrate, but there is always a risk of dropping and breakage [19,20]. Furthermore, vacuum-based pick and transfer is effective when the chips are not adhered to the substrate. As an example, during thinning by lapping the chips are placed firmly on a wax-based substrate and vacuum-based pick and transfer does not work because of higher fragility of the chip or wafer after thinning. Such issues are

* Corresponding author.
E-mail address: Ravinder.Dahiya@glasgow.ac.uk (R. Dahiya).
[1] authors equally contributed to this work.

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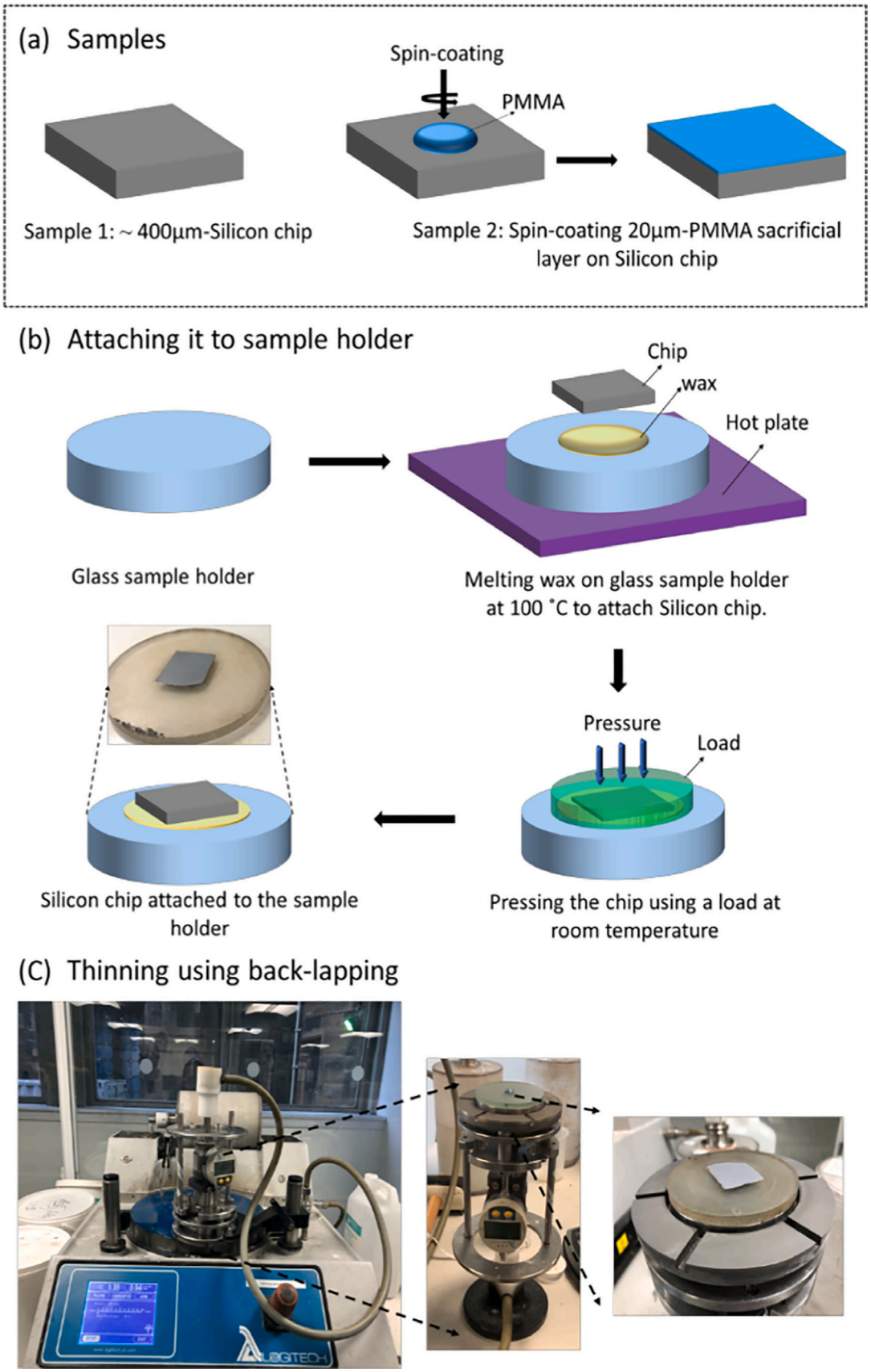

Fig. 1. Schematic flow of the wafer/chip thinning process; (a) Sample preparation namely sample1 is the silicon chip without any sacrificial layer and sample2 is the silicon chip with the PMMA sacrificial layer, (b) schematic flow of attaching the samples to the sample holder using wax and (c) the digital image of the backside thining using a lapping machine, in which the sample on the sample holder is mounted on the Jig (right corner).

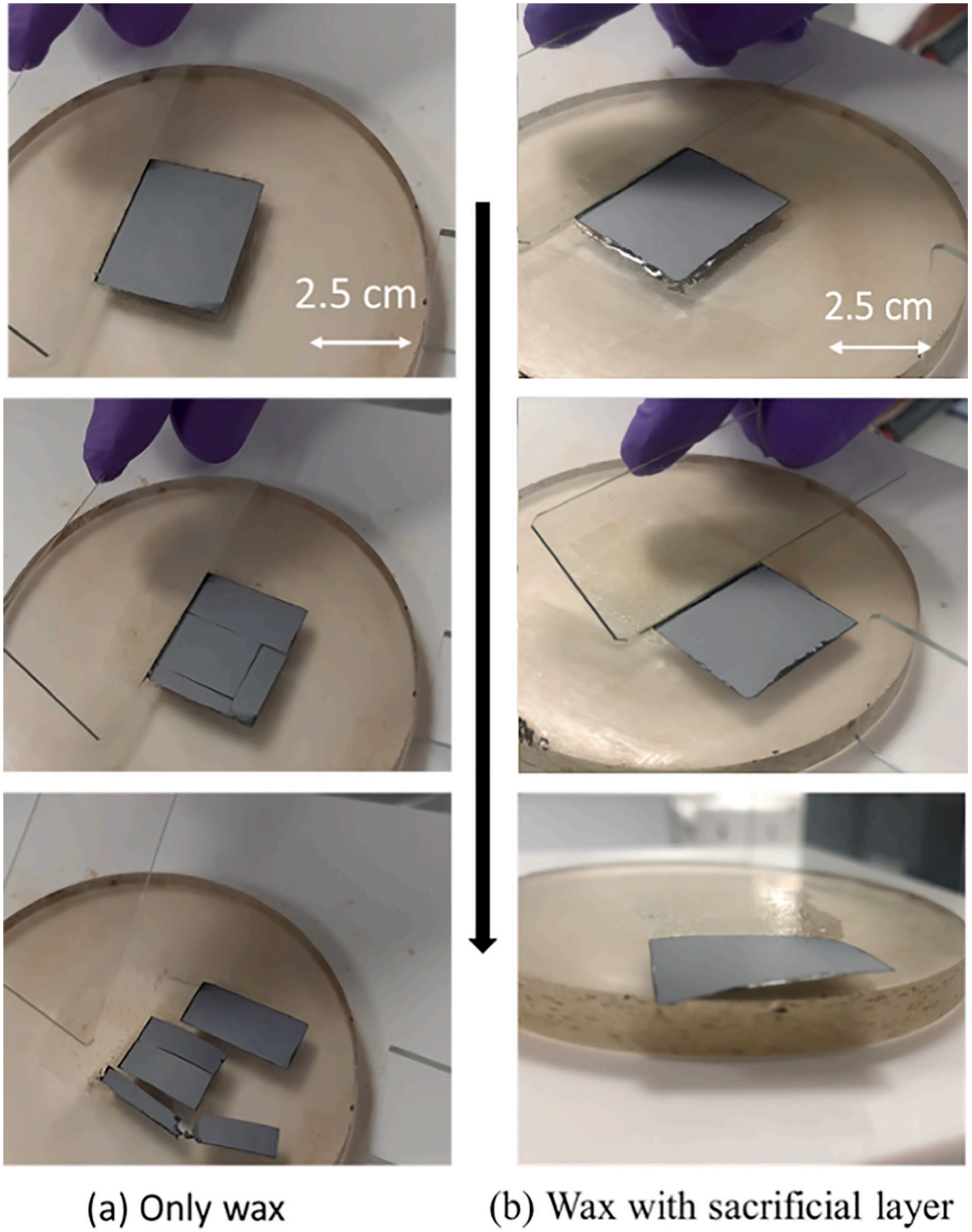

Fig. 2. Image of UTCs during separation from the glass sample holder after lapping process; (a) Sample 1, silicon without sacrificial layer, and (b) sample 2, silicon with PMMA as a sacrificial layer.

some of the long-standing challenges even for conventional electronics and indicate that handling difficulties for thinned chips and wafers are simply higher. Therefore, the UTC research, particularly when the thinning is done by lapping, will greatly benefit from an easy transfer method.

Herein, we present a new cost-effective method for a reliable removal or debonding of UTCs from wax substrates, after thinning has been carried out using backside lapping. The simple method presented here involves using a polymethylmethacrylate (PMMA) sacrificial layer between UTCs and the wax and the transfer or removal of UTCs is achieved without warpage. PMMA is suitable as the sacrificial layer owing to features such as great tensile strength, high rigidity, scratch resistance, low toxicity and cost [21]. As a thermoplastic material, PMMA can be easily removed with acetone [22,23]. Further, during the transfer or removal of UTCs from wax, the PMMA-based sacrificial layer also acts as a stress-relieving agent. Additionally, it can protect the active device region from impurities or damages during thinning and transferring processes. Taking advantage of these features of PMMA-based sacrificial layer, we demonstrate the removal or transfer of flexible UTCs that are 30-40 μm thick. Although different types of sacrificial

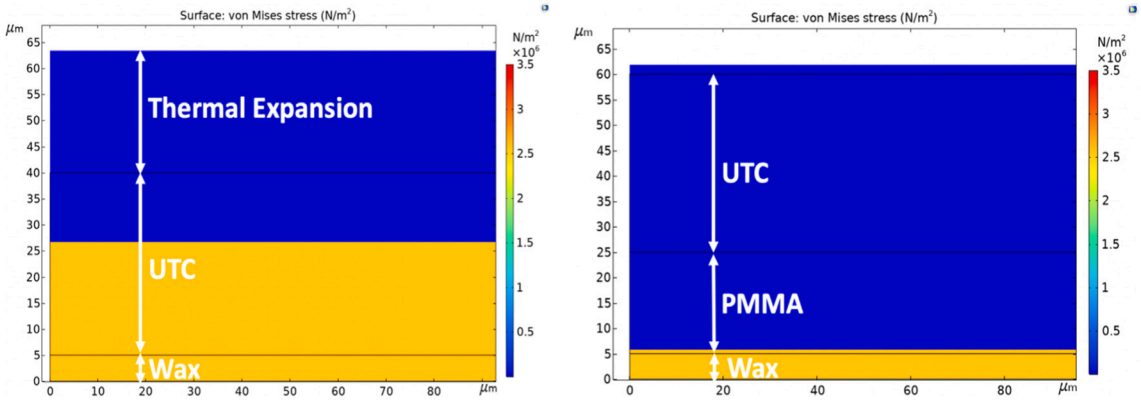

Fig. 3. Simulation results obtained from COMSOL comparing the stress distribution of UTCs without and with a sacrificial layer; (a) UTC without any sacrificial layers; (b) UTC with PMMA as the sacrificial material.

Table 1
Sacrificial materials comparison.

Materials	SiO_2	Photoresist	PI	PC	PMMA
Young's modulus	74GPa [31]	4.02GPa [32]	4.0GPa [33]	2.3GPa [34]	3.1GPa [35]
Removal Method	Wet Etching [38]	Dry Etching [39]	Dry Etching [40]	Dioxane [41]	Acetone [36]
Von Mises Stress (N/m^2)	2.85×10^6	4.08×10^4	1.45×10^4	2.77×10^4	7.86×10^2

materials (e.g. photoresist, polyimide (PI) and silicon dioxide (SiO_2) etc.) have been used in the fabrication of Micro-Electro-Mechanical-Systems (MEMS) devices [24–26], to the best of our knowledge, there are no studies involving the use of PMMA as a stress-relieving sacrificial layer.

This paper is organised as follows: Section II presents the thinning processes adopted in this paper for thinning of UTCs. The post-thinning experimental results such as removal of UTCs and demonstrating the importance of the sacrificial layer are discussed in Section III. The results related to the characterisation and analysis of the effect of bending on MOSCAP devices present on the UTCs are presented in Section IV. Finally, the key outcomes are summarised in Section V.

2. Materials and thinning methodology

The thinning process carried out in this work involves three steps: (1) Sample preparation; (2) Attachment of sample on holder with wax substrates; and (3) Backside lapping

2.1. Sample preparation

Two silicon chips, each with the thickness, length and width of ~400 µm, 2.5 cm and 2.5 cm respectively were utilised for the thinning process. As shown in Fig. 1a, the pristine silicon chip was considered as sample 1. The second sample (sample 2) was prepared by spin coating a ~20 µm-thick PMMA over a silicon chip on the polished side or on the device side (in processed chip). In the latter case, the PMMA acts as a sacrificial layer during the backside lapping. A 15 wt% PMMA in anisole was spin-coated at 1000 rpm to obtain ~20 µm thick PMMA sacrificial layer.

2.2. Attaching the chips to the sample holder

Prior to initiating the backside lapping process, the two silicon chips were attached to a sample holder by placing the polished side (sample 1) or the PMMA side (sample 2) on top of the glass sample holder via the wax (Fig. 1b). The holder was used as a chip carrier and the solid wax was placed at the centre of this holder. The sample holder (with the wax) was then placed on a hot plate set at 100 °C. When the wax started to melt, the silicon chip was placed on top of the wax, with the polished surface facing the wax (e.g. the polished side of the silicon chip directly touching the wax for sample 1 and the PMMA layer touching the wax for sample 2). Attaching the chip on the glass holder via wax is needed to firmly hold the chip during lapping. Subsequently, the whole setup was placed under a contact pressure equipment at room temperature for about 30 min to ensure a solid bonding between the chip and the sample holder. In the case of sample 2, the PMMA layer was removed on the

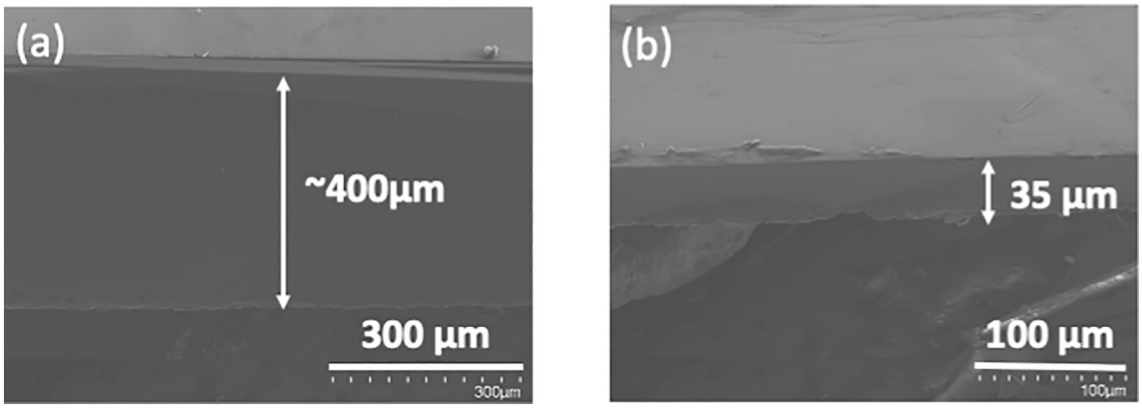

Fig. 4. SEM images of silicon chips; (a) Silicon chip with original thickness of 400 µm. (b) Thinned chip with a thickness of 35 µm.

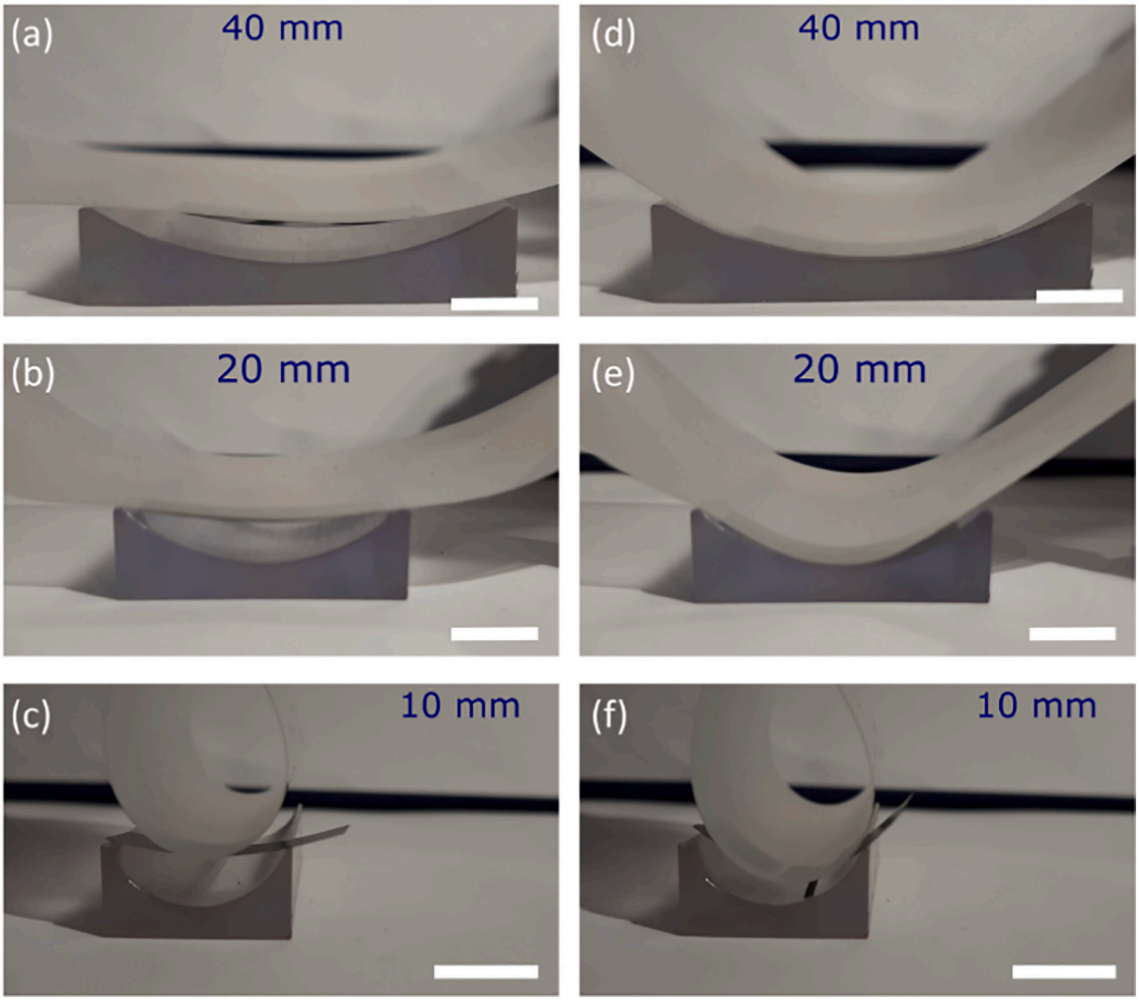

Fig. 5. The bending tests: UTC placed flat on top of 3D printed bending test rig with bending radius (a) 40 mm; (b) 20 mm; and (c) 10 mm; and UTC subjected to different bending radii (d) 40 mm; (e) 20 mm and (f) 10 mm. The scale bar is 10 mm.

periphery (<1 mm) of the chip before attaching to the glass sample holder to ensure good adhesion of the chip to the sample holder [27,28]. This also prevented the PMMA layer from peeling off during lapping.

2.3. Back lapping

The Logitech lapping machine was utilised for the back-lapping process, as shown in Fig. 1c. Firstly, the glass sample holder was attached tightly to the lapping jig using vacuum. While lapping, a mixture of water and aluminium oxide (Al_2O_3) powder with a particle diameter of ~15 μm was utilised as the slurry to back-thin the silicon substrate as shown in Fig. 1c. The speed of the lapping plate was set to around 25 rpm, and the thickness of the etched silicon was observed using the thickness monitor on the jig (Fig. 1c). After thinning, the sample was removed from the glass holder by placing the glass sample holder on a hot plate at 100 °C. Once the wax got melted, the UTC was carefully pushed from the glass sample holder (Fig. 2). After this, the residual wax and PMMA were removed using acetone.

3. Removal of UTCs

Fig. 2 demonstrates the separation of the UTC from the glass sample holder (Video S1, supporting information). After back-thinning, the critical challenge lies in the separation or removal of UTCs from the sample holder. Due to their fragile nature, the UTCs are prone to cracks and damages (Fig. 2a) and therefore the stresses on the UTCs during the separation process need to be carefully evaluated. In an industrial back-thinning process, the silicon samples are generally attached to sample holders using UV tapes. The adhesion of these tapes with UTCs on the sample holder can be controlled by irradiating UV light. The adhesion strength of these tape is reduced because of UV irradiation, and this facilitates an easy separation of the UTCs from the sample holder. These tapes are also utilised to encapsulate and protect the semiconductor devices from impurities and/or damages. However, these tapes are costly and lead to higher manufacturing cost of UTCs. For example, 2 ml of PMMA needed here would cost ~$0.1, which is much lower than the cost of UV tape for 6-in. wafer (~$1). Recent reports also highlight the issue related to the increase in overall UTC manufacturing cost due to UV tape [29]. An economic alternative way of thinning is to attach the bulk silicon chip to the glass sample holder using a wax layer, as shown in Fig. 1b. After thinning, the wax can be melted at 100 °C to separate the UTCs. But the melting of wax results in greater stresses which eventually damage the UTCs and cause a poor device performance. As a result, the use of wax for chips with thickness below 100 μm is quite challenging. This is also evident from the experiments related to sample 1, which was attached directly to the wax and then thinned down to about 50 μm thickness. Multiple cracks were developed in the sample when we attempted to remove it from the glass sample holder, as shown in Fig. 2a. In this case, to facilitate the separation or removal from wax, the UTC was gently pushed with a glass slide after the wax readily melted at 100 °C. During this process, the thermal stress that the UTC experienced induced warping and multiple crack formation in the UTCs.

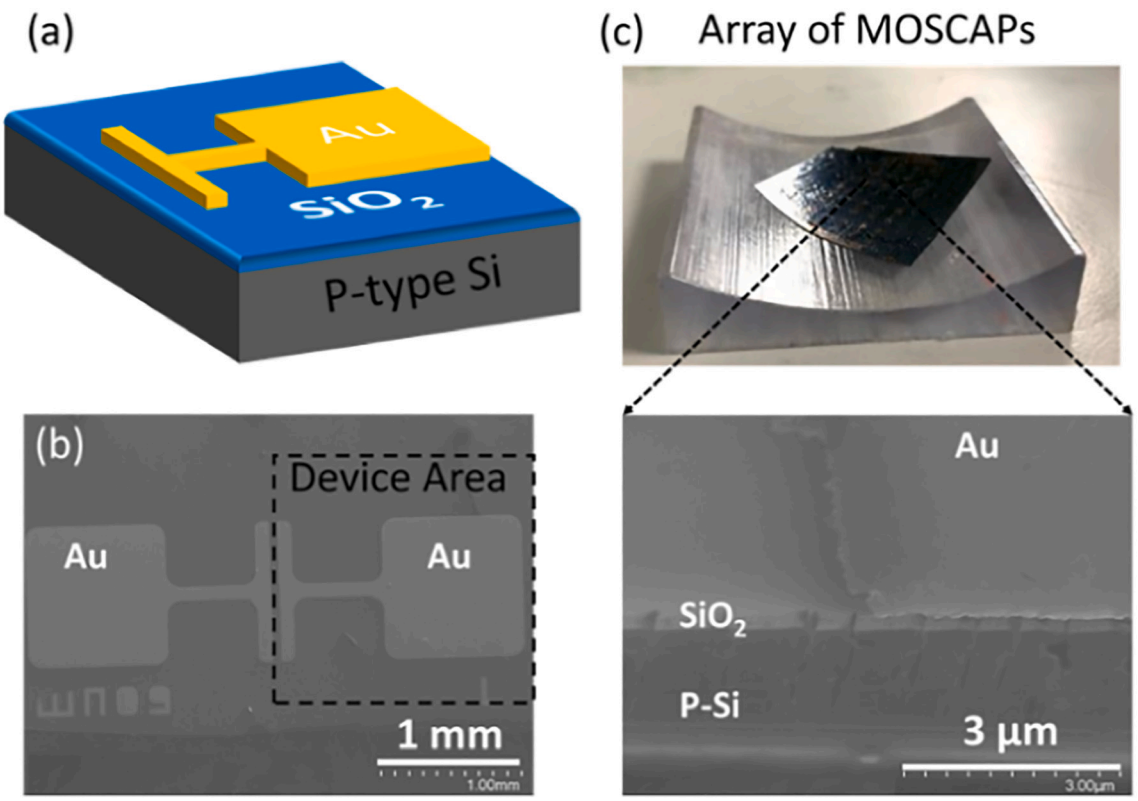

Fig. 6. MOSCAPs thinning: (a) the schematic of MOSCAPs devices; (b) SEM image of the MOSCAPs before thinning; (c) Array of MOSCAPs after thinning.

The stress distribution during the separation of UTCs from the wax on the sample holder was investigated using COMSOL Multiphysics®. Fig. 3 shows the thermal stress distribution inside the UTCs with- and without- a sacrificial layer. In the case of sample 1, the model is composed of UTC with dimensions of 2.5 cm × 2.5 cm × 35 µm (length, width and height) placed directly above the wax with dimensions of 2.5 cm × 2.5 cm × 5 µm (length, width and height). When the temperature of 100 °C is applied to the model, the Von Mises stress of 2.58×10^6 N/m^2 is noticed at the interface between the wax and the UTC (the side at which the potential devices would be resting). In addition, a thermal expansion of the chip is also observed as shown in Fig. 3a. Therefore, introducing an additional layer to relieve thermal stress at the interface between wax and the UTC has been explored.

The thermally insulating organic or inorganic layers could be used to reduce the temperature induced stress on UTCs during the separation process [30]. In this regard, sacrificial materials such as photoresist, polyimide (PI), silicon oxide (SiO_2), polycarbonate (PC) and PMMA were selected and simulated in COMSOL Multiphysics®. In the case of UTCs with a sacrificial layer, the model composed of an additional sacrificial layer with dimensions of 2.5 cm × 2.5 cm × 20 µm (length, width and height) which is placed in between the wax and the silicon chip, as shown in Fig. 3b. Accordingly, the Von Miss stress predicted at 100 °C for various sacrificial layer materials such as SiO_2, photoresist, PI, PC and PMMA are 2.85×10^6 N/m^2, 4.08×10^4 N/m^2, 1.45×10^4 N/m^2, 2.77×10^4 N/m^2, and 786 N/m^2, respectively, as shown in Table 1. Based on the simulation, the model with PMMA revealed the lowest stress amongst the selected sacrificial layer materials. The protective layer with lower stiffness and a relatively low Young's modulus (E) is preferred. This is because when the melted wax starts to drag the polymer layer, the polymer chain with low Young's modulus has multiple degrees of freedom which guides the polymer to deform at the wax interface without any significant changes at the UTC interface. In this regard, PC and PMMA have relatively lower Young's modulus (E of SiO_2 = 74GPa, E of photoresist = 4.02GPa, E of PI = 4.0GPa, E of PC = 2.3GPa, E of PMMA = 3.1GPa) [31–35]. However, PC tends to be 30% more expensive than PMMA, which would potentially increase the cost of the process [36]. Besides, PC forms Bisphenol A (BPA) during hydrolysis, which is hazardous to health and the environment [37]. Finally, the sacrificial layer needs to be removed after removal of UTCs and in this regard their removal method also needs to be taken into consideration. The chemical etching needed for removal of SiO_2, photoresist, and PI can significantly increase the cost and complexity of the process [38–40]. However, PC and PMMA can be simply dissolved in chemical solution, as presented in Table 1 [23,41]. In conclusion, considering low Von Mises Stress, low Young's Modulus, easy removal method and low cost, PMMA stands out as the preferred sacrificial material. Compared with the UTC without any sacrificial layer, the stress over the polished side of the chip is drastically reduced from 2.58×10^6 N/m^2 to only 786 N/m^2 with the use of PMMA as a sacrificial layer (Fig. 3a and b).

To prove our hypothesis, the sample 2 separation from the glass substrate with a sacrificial layer was also tested. We achieved ~35 µm-thick UTCs after thinning from about 400 µm by using the lapping machine. In this case, a 20 µm-thick PMMA layer was used as a thermal insulating sacrificial layer before bonding the bulk chip. As shown in Fig. 2b, the thinned silicon chip was successfully separated by using the glass slide, following similar steps as for sample 1 (Video S1, supporting information). A minor warping was also observed. It is worth mentioning that sample 1, i.e. without PMMA layer, was broken into pieces when it was being removed from the hot plate (Fig. 2a) using a similar removal process. Clearly, PMMA's rigidity, scratch resistance as well as tensile strength are protecting the UTC during the separation process. The thickness of the PMMA layer also plays a critical role in the successful separation of the UTCs. In our study, we used a 20 µm-thick PMMA layer, but by further increasing the thickness it may be possible to eliminate the warping of UTCs caused by thermal stress. For example, from Fig. 3 it is evident that the thermal expansion on UTC, responsible for warping, is much larger without any sacrificial layer. At the same

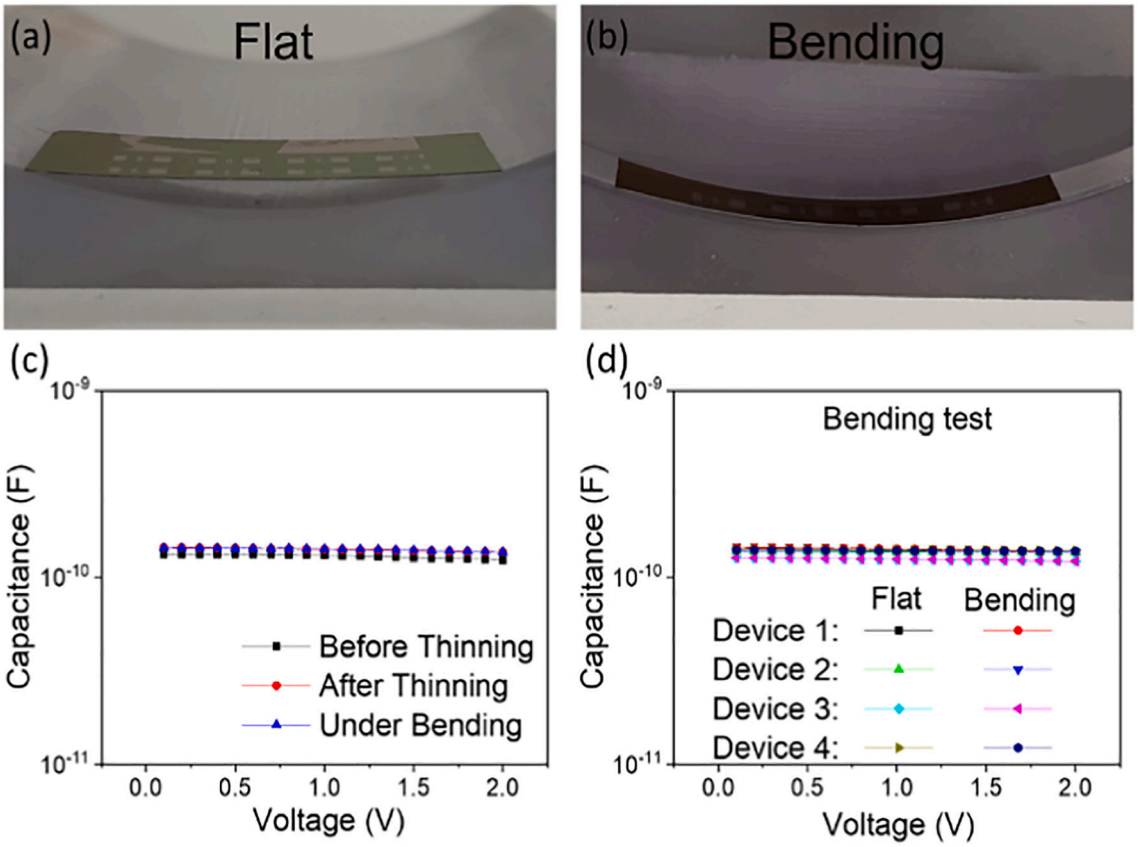

Fig. 7. Processed chip with array of MOSCAPs device. The image of 8 × 2 array of MOSCAPs mounted on 3D printed bending tool under (a) flat and (b) 40 mm bending state; (c) Comparison of C-V plot of MOSCAP device before and after thinning and under bending; (d) C-V measurement under flat and bending state for four devices.

time, smaller thermal expansion is observed on UTC from COMSOL simulations (Fig. 3b) even after introducing the 20 μm-thick PMMA which resulted in minor warpage of the UTCs (Video S1, supporting information). Based on the observation, we predict that increasing the thickness of the PMMA layer will minimise the thermal induced warping of UTCs. In order to achieve thicker PMMA, multiple spin coatings could be performed. The PMMA layer could be easily removed from the UTCs by placing it in the acetone bath, which is also compatible with the conventional electronics manufacturing process.

The thickness and surface morphology of UTCs were observed using the cross-sectional scanning electron microscope (SEM) of the bulk silicon chip and the UTC, as shown in Fig. 4. It can be clearly observed from SEM images (Fig. 4a) that the thickness of the bulk silicon sample was ~400 μm. After thinning, the thickness of the silicon chip was reduced to 35 μm as shown in Fig. 4b. The flexibility of the UTCs was also investigated using 3D printed concave shaped test rigs with radius of curvature of 40 mm, 20 mm, and 10 mm, as shown in Fig. 5a–c (Video S2 supporting information). In the case of 40 mm and 20 mm bending, the UTCs could conform to the concave shaped test rigs without any cracks (Fig. 5d and e). However, the UTC broke into multiple pieces when subjected to 10 mm bending radius as shown in Fig. 5f. This is because the mechanical strength of the UTCs should not crack at least up to the tensile stress of 300 MPa, which is determined using simple stress formula:

$$\sigma = E \cdot h / 2R$$

where E is the Young's modulus of Si (180 GPa), h is the thickness (35 μm) and R is the bending radius [42–44]. Based on this equation, the stress acting on the UTCs under 40 mm, 20 mm and 10 mm bending radius are calculated as 78.75 MPa, 157.5 MPa and 315 MPa, respectively. Therefore, the stress acting on UTCs exceeds the critical stress value of 300 MPa while subjected to the 10 mm bending radius, taking UTCs to the breaking point and eventually resulting in multiple broken pieces.

4. Characterisation and evaluation of devices

To study the effect of thinning on the processed chips, the metal-oxide-semiconductor capacitors (MOSCAPs) were fabricated on a P-type Si/SiO_2 (490 μm/300 nm) substrate. A shadow mask consisted of 8 × 5 arrays of openings, 10 nm-thick titanium and 80 nm-thick gold were deposited using electron-beam (e-beam) evaporator to obtain metal electrodes. This step defined the active MOSCAP device area with the length and width of 1 mm and 1 mm, respectively (Fig. 6a and b). The single chip (length = 2.5 cm, width = 2.5 cm, and thickness = ~490 μm) consists of 8 × 5 arrays of MOSCAP devices (Fig. 6c). Sequentially, the p-type substrate of the MOSCAP array was thinned down to ~35 μm through back lapping process (section II), with the MOSCAP array attached to the sample holder with the help of a PMMA sacrificial layer and wax. After thinning, the chip with MOSCAPs array was separated from the glass sample holder (Video S3, supporting information) and the PMMA sacrificial layer was removed by rinsing in acetone and DI water. Fig. 6c shows the array of MOSCAPs on a 40 mm bending test rig and the cross-sectional SEM image of single MOSCAP device displaying individual layers (metal, oxide, and semiconductor).

To evaluate the effect of thinning on the MOSCAP device performance, the MOSCAP device was characterised before and after the thinning process as shown in Fig. 7. In addition, the flexibility of the MOSCAP device was evaluated by measuring the capacitance while the device was placed on a 40 mm bending test rig (Fig. 7a and b). The

device demonstrated a stable capacitance value of 134 ± 10 pF (scan range of 0 to 2 V) under all three conditions, namely 1) before thinning, 2) after thinning and 3) under bending (Fig. 7c). From the capacitance-voltage characterisation (C-V plot), it is evident that the thinning process does not affect the device performance. Furthermore, thinning of MOSCAP chip introduced flexibility (Video S4, supporting information) without any degradation in the device performance. In addition, a minimum device to device variation (<±10 pF) was observed, as shown in Fig. 7d. Therefore, this approach has the potential to develop cost-effective high performance flexible electronic devices for 3D stacking and wearable applications.

5. Conclusions

This work shows a simple and economical method for the removal of thinned silicon chips without causing damages. The method uses PMMA as a sacrificial layer for a successful lapping process. The thinning and debonding processes of UTCs with and without the sacrificial layer were compared. The PMMA sacrificial layer reveals a stress-free method for the handling and transfer of UTCs without breakage. UTCs with approximately 35 μm thickness have been successfully obtained by using the presented method. This fabrication approach takes advantage of PMMA mechanical properties. Due to the simplicity of the method, there is a good potential for the presented approach to be employed in the large-scale manufacturing of UTCs. Furthermore, the processed UTCs demonstrated stable performances before and after thinning processes with an enhanced flexibility. This technique can possibly be implemented to directly transfer the UTCs to the targeted substrate. Further studies are being conducted to directly transfer/bond the UTCs with devices to polyimide substrates for practical applications.

Supplementary data to this article can be found online at https://doi.org/10.1016/j.mee.2021.111588.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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