$V_{\min}$ Prediction for Negative Capacitance MOSFET based SRAM

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***Abstract*—In this work we show that SRAM cells designed using negative capacitance (NC) based MOSFETs (NCFETs) can offer improved $V_{\min}$ (minimum supply voltage needed for reliable operation) compared to conventional MOSFET based SRAM. Increased noise margins and reduced variability in NCFETs lead to this lowering of $V_{\min}$. For this work we use a modified version of the standard BSIM4 compact model for bulk MOSFETs by coupling it with the Landau-Khalatnikov model of ferroelectrics in a self-consistent manner, while the statistical variability information of the reference device is extracted from 3D statistical TCAD simulations.**

***Keywords*—Negative Capacitance, MOSFET, SRAM, n-curve, $V_{\min}$, variability**

I. Introduction

Different approaches have been in vogue for countering the slow scaling of SRAMs in the sub-100 nm regime. SRAM designs based on new transistor architectures have been researched extensively during the last decade with a number of optimizations proposed taking a device-circuit co-design approach [1], [2]. In the mean time, in recent years negative capacitance effect of ferroelectrics has been utilized to enhance the performance of CMOS devices, enabling more aggressive supply voltage ($V_{\rm DD}$) scaling due to the possibility of achieving sub-60mV subthreshold swings [3]–[5].

Accordingly, various modeling approaches and the impact of improved transistor characteristics on circuits have been reported [6]. In particular, performance of 7nm node NC-FinFET based SRAM was reported in [7]. Further, NC transistors have been shown to offer variability suppression [8]–[10] which is expected to improve the minimum supply voltage for SRAM operation. In this work we examine the SRAM stability through circuit simulations using a compact model of NCFETs.

II. Methodolgy and Modeling Approach

Fig. 1 shows the cross-sectional schematic of the NCFET. The ferroelectric layer is deposited between the internal gate of the baseline MOSFET and an external metal gate. Table I lists some of the structural details of the device. Fig. 2 describes the overall methodology of this work. We start with the extraction of the compact model from the TCAD simulation of the variability-free device. We then perform 3D statistical TCAD simulations of the reference MOSFET

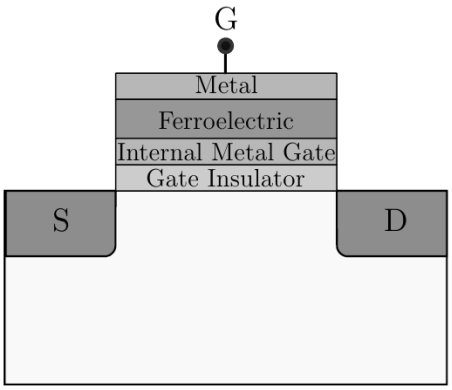


Fig. 1. Cross-sectional schematic of the NCFET. The bulk MOSFET is "well" designed with a gate length of 25nm.

using GARAND [11] considering the three major sources of statistical variability: RDD (random discrete dopants), LER (line edge roughness), and MGG (metal gate granularity). The key parameters used in the statistical simulation are included in Table I. From the statistical ensemble, we obtain the variability in the threshold voltage, σVt, which together with the nominal model parameters leads to variability aware compact model card. Next, these parameters are fed to the NCFET model. The compact modeling approach using a self-consistent coupling of the BSIM4 model [12] with the ferroelectric model [13] has been illustrated in Fig. 3. A ferroelectric thickness (t_{fe}) of zero corresponds to the reference bulk MOSFET.

A. Nominal Device Characteristics

Fig. 4 shows the transfer characteristics of the reference MOSFET and NCFETs (with different t_{fe}). The NCFET devices show superior characteristics with steeper subthreshold swing and higher drive current compared to the reference MOSFET for the same OFF-state leakage. Note that for the ferroelectric parameters and the thickness of the ferroelectric layer used in this work, the nominal devices are hysteresis-free.

B. Variability Suppression

The improved electrostatics in NCFETs leads to a suppression of statistical variability. This has been shown using TCAD simulations as well as compact modeling approaches. In this work, for simplicity we have focused on the variation

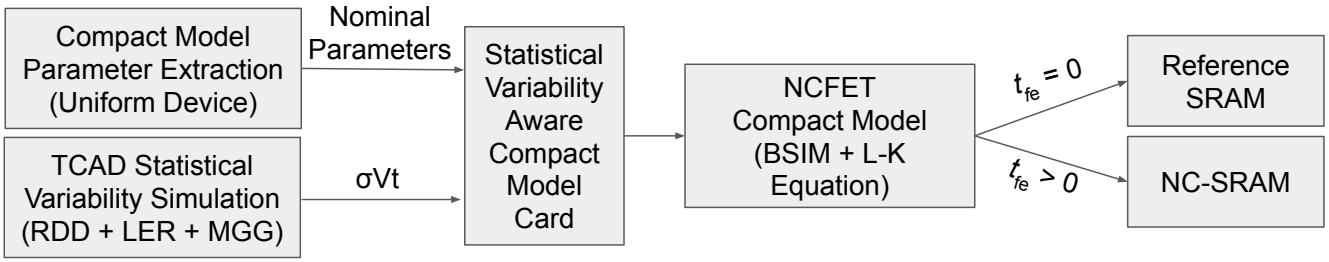


Fig. 2. Flow of the overall methodology used in this work. A ferroelectric thickness, t_{fe} of zero corresponds to the reference bulk MOSFET.

TABLE I. DEVICE DETAILS

Parameter	Value
(a) Reference MOSFET	
L_{gate}	25 nm
W_{gate}	25 nm
EOT	1 nm
N_A	5×10^{17} cm^{-3}
$N_{S/D}$	1×10^{20} cm^{-3}
(b) Ferroelectric Layer	
t_{fe}	1-3 nm
P_r	5 μC/cm^2 [14]
E_c	1 MV/cm [14].
(c) Statistical Variability	
LER correlation length	25 nm
LER RMS amplitude	0.66
MGG	TiN gate (Two W.F. distributions with 40% and 60% probability)

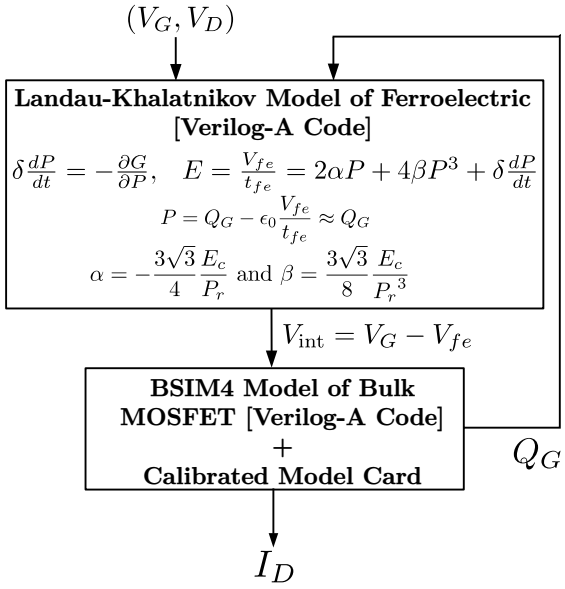


Fig. 3. Compact Modeling Approach. P = polarization, G = total free energy, E = electric field, V_{fe} = voltage drop across the ferroelectric, t_{fe} = ferroelectric thickness, δ = ferroelectric damping factor, Q_G = gate charge, α and β: Landau parameters, E_c = coercive field, P_r = remnant polarization.

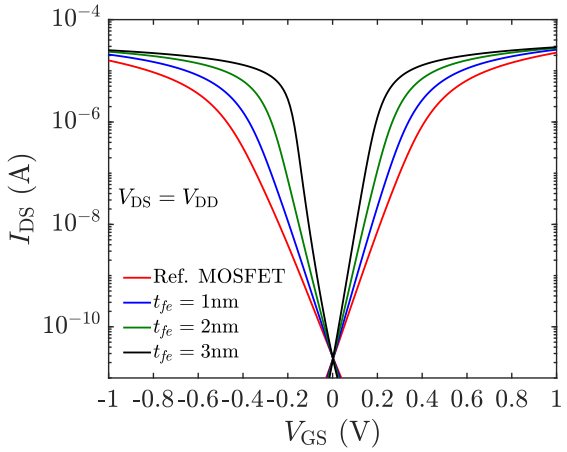


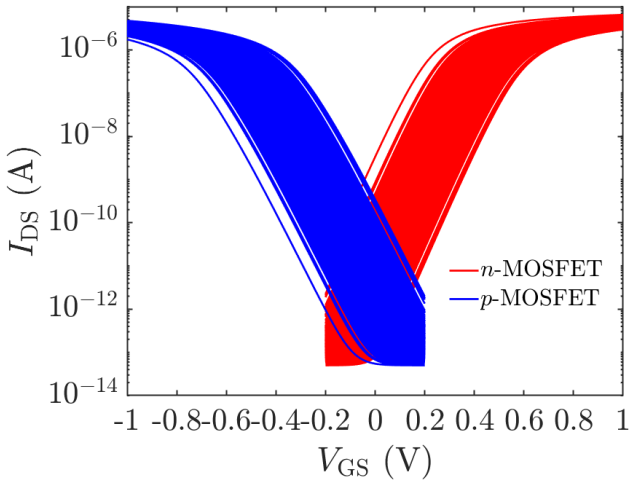
Fig. 4. $I_{\text{DS}} - V_{\text{GS}}$ characteristics of n and p type Ref. MOSFETs and NCFETs with different t_{fe} at V_{DS}=V_{DD}=1V at iso-I_{OFF}.

of threshold voltage and the corresponding BSIM4 compact model parameter. We have applied a Gaussian distribution of the threshold voltage parameter with standard deviation obtained from the statistical simulations of the reference MOSFET. We ran Monte Carlo simulations with a statistical ensemble of 1000 devices in the circuit simulator. Fig. 5 shows the ensemble of the transfer characteristics of the two devices with the NCFET clearly displaying lesser variability than the reference bulk device. Note that in this preliminary study, the variability contribution of the ferroelectric layer has not been considered.

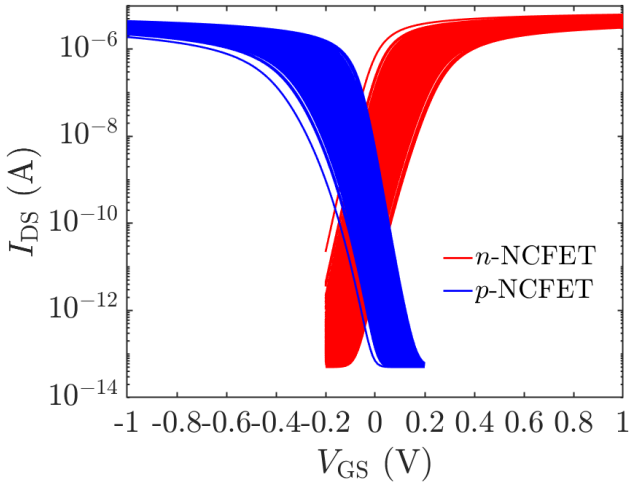
III. STATISTICAL SRAM SIMULATIONS

A. Setup Details

In this section we compare the V_{min} of the 6-T SRAM cells designed using NCFETs and the conventional reference bulk MOSFETs. In the SRAM cell, the Pull-Up, Pass-Gate and Pull-Down transistor widths are in a ratio of 1:2:3. We have considered the evaluation of the read stability and write ability in terms of the critical currents under read and write conditions (I_{crit} and I_{critw} respectively) obtained from the analysis of the respective n-curves [15]. The schematic of the 6T-SRAM cell along with the arrangement for the n-curve measurements is shown in Fig. 6. A DC voltage V_{in} is applied to the storage node and the current entering the node is recorded, The $I_{\text{in}} - V_{\text{in}}$ plots under the READ and WRITE conditions are the n-curves.



(a)



(b)

Fig. 5. Statistical ensemble of 1000 $I_{\rm DS} - V_{\rm GS}$ characteristics of n and p type (a) Ref. MOSFETs, and (b) NCFETs with $t_{fe} = 2$nm obtained from Monte-Carlo SPICE simulations. $V_{\rm DS}$=0.05V.

It has been previously shown that for the nominal case, the NC-SRAM offers higher $I_{\rm crit}$ under READ condition as well as higher $I_{\rm critw}$ under WRITE condition [7]. To examine the impact of variability, we perform 5000 statistical Monte Carlo simulations for the 6T SRAM cells, with the threshold voltage parameter for each nominal transistor having a Gaussian distribution as described in section II-B. The NC-SRAM displays lower relative standard deviation (σ/μ) for the critical currents.

B. $V_{\rm min}$ Analysis

$V_{\rm min}$ is the minimum supply voltage needed for reliable operation of the SRAM cell. The methodology for $V_{\rm min}$ calculation is as follows: i) We calculate $N_{\sigma,Fail} = \mu/\sigma$ as $V_{\rm DD}$ is varied. Here μ and σ are the mean value and standard deviation of the critical currents obtained from 5000 Monte-Carlo runs in the circuit simulator. ii) A target $N_{\sigma,Fail}$ is set. iii) The $V_{\rm DD}$ corresponding to the target $N_{\sigma,Fail}$ is the

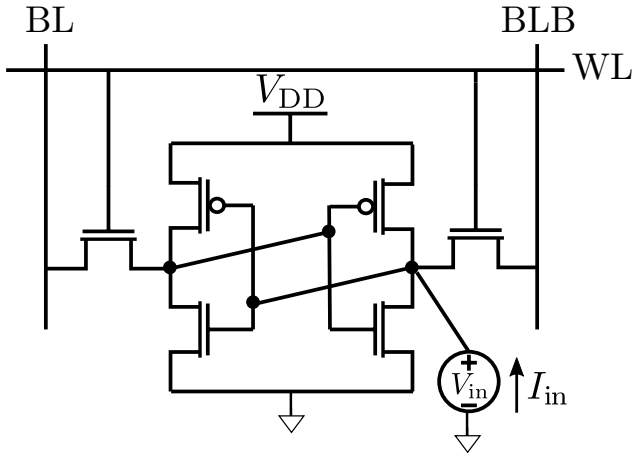


Fig. 6. Schematic of the 6-T SRAM cell including the arrangement for the n-curve measurements.

$V_{\rm min}$. In this work, target $N_{\sigma,Fail}$ has been set to 5.4. $V_{\rm min}$ is known to be limited by variability, and hence NC-SRAMs due to the suppressed variability are expected to achieve lower $V_{\rm min}$ relative to the regular SRAMs. Indeed, we find that the NC-SRAMs offer better $V_{\rm min}$ than their regular counterparts. Fig. 7 shows the percentage improvement in $V_{\rm min}$ when considering the critical current variability obtained from the READ n-curve ($I_{\rm crit}$). It can be seen that for the $V_{\rm min}$ derived from $I_{\rm crit}$, the advantage of NCFETs initially increases with t_{fe} till an optimum value (t_{fe}= 2 nm corresponds to a 34% reduction in $V_{\rm min}$) and then starts to decrease at higher t_{fe}.

However, for the $V_{\rm min}$ derived from $I_{\rm critw}$, the gains are much lower, with t_{fe}= 2 nm showing lesser improvement than t_{fe}= 1 nm, while t_{fe}= 3 nm cannot fulfill the set criterion. Thus the overall $V_{\rm min}$ cannot be lowered as much as the $I_{\rm crit}$ analysis suggests, and the limit to maximum t_{fe} is set by the WRITE operation. These trends are similar to the reduction of critical current improvement in the nominal SRAMs on increasing the ferroelectric thickness beyond a certain value [7]. It should be noted that for a more comprehensive study, the variability in the ferroelectric layer thickness and properties (the Landau parameters in our modeling approach) should also be taken into account. It is expected that considering this will further diminish the $V_{\rm min}$ improvement.

IV. Conclusion

Statistical device simulations considering the effects of random discrete dopants, line edge roughness, and metal gate granularity are performed for reference bulk devices. A self-consistent coupling of the standard BSIM4 compact model with the Landau-Khalatnikov equations has been used for compact modeling of the ferroelectric NCFETs. Using statistical circuit simulations utilizing the threshold voltage variability data of reference MOSFETs, we have shown that the better characteristics and immunity of the NCFETs against the baseline MOSFET's conventional statistical variability translates into lower $V_{\rm min}$ for NCFET based SRAMs, especially under READ condition. This shows that more aggressive $V_{\rm DD}$ scaling relative to existing CMOS technologies is possible

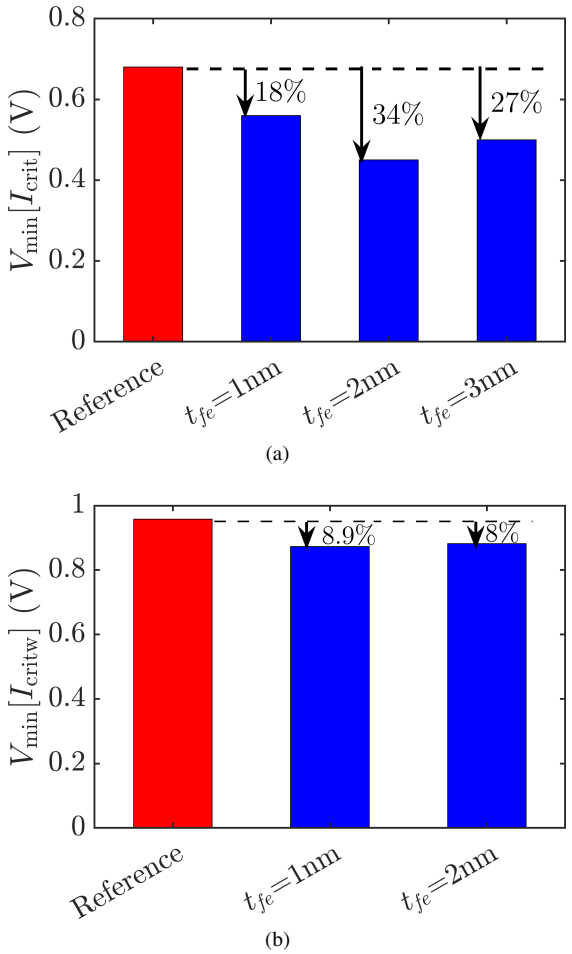


Fig. 7. Comparison of $V_{\min}$ for reference SRAM and NC-SRAM with varying t_{fe} derived from (a) read n-curve (I_{crit}) and (b) write n-curve (I_{critw}).

using NCFETs. As a further work, the impact of the ferroeletric layer itself should also be included in the analysis in order to determine more realistic performance.

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