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Improved quality of InSb-on-insulator microstructures by flash annealing into melt

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Abstract

Monolithic integration of III–V semiconductors with Silicon technology has instigated a wide range of new possibilities in the semiconductor industry, such as combination of digital circuits with optical sensing and high-frequency communication. A promising CMOS compatible integration process is rapid melt growth (RMG) that can yield high quality single crystalline material at low cost. This paper represents the study on ultra-thin InSb-on-insulator microstructures integrated on a Si platform by a RMG-like process. We utilize flash lamp annealing (FLA) to melt and recrystallize the InSb material for an ultra-short duration (milliseconds), to reduce the thermal budget necessary for integration with Si technology. We compare the result from FLA to regular rapid thermal annealing (seconds). Recrystallized InSb was characterized using electron back scatter diffraction which indicate a transition from nanocrystalline structure to a crystal structure with grain sizes exceeding 1 μm after the process. We further see a 100× improvement in electrical resistivity by FLA annealed sample when compared to the as-deposited InSb with an average Hall mobility of 3100 $cm^2 V^{-1} s^{-1}$ making this a promising step towards realizing monolithic mid-infrared detectors and quantum devices based on InSb.

Supplementary material for this article is available online

Keywords: Insb, rapid melt growth, flash lamp anneal, Hall mobility, heterointegration

(Some figures may appear in colour only in the online journal)

1. Introduction

Si complementary metal oxide semiconductor devices (CMOS) is the foundation for the semiconductor industry we have today. However, further scaling of Si CMOS is becoming increasingly challenging due to increase in the leakage currents, difficulties in controlling the device electrostatics and short channel effects [1]. This as well as the emergence of the Internet-of-Things has pushed research to find ways to enhance the functionality of the electronic chips, such as adding optical sensors, quantum devices, wireless communication and integrated memories [2, 3] on top of the digital circuits. Many of these devices can be better realized in other materials than Si, in particular III–V semiconductors with direct bandgap, high electron mobility and strong spin–orbit coupling are excellent candidates for heterointegration [4, 5]. It is however critical that these materials can be integrated with high-quality, low thermal budget and in a compatible process, to be viable for large scale use. Several techniques for integrating III–V on Si have been reported, such as direct epitaxial growth using thick buffer layer [6],

wafer bonding [7, 8] aspect ratio trapping (ART) [9], nanowire epitaxy and template assisted selective epitaxy (TASE) [10, 11]. While especially ART and TASE are CMOS-compatible processes that give high quality material, the lateral size of the integrated structures is limited to a few microns at most.

Rapid melt growth (RMG) is a technique to integrate III–Vs on Si to obtain high quality single crystalline structures, tens to hundreds of micrometers in lateral dimension while down to tens of nanometer in thickness [12–14]. In RMG a low-quality film is deposited on an insulator and with only a small contact area to the crystalline substrate. The film is structured and contained within a dielectric capping layer (crucible), after which it is annealed until melting. Upon cooling the melt crystallizes rapidly starting from the contact point of the crystalline substrate, leading to a single crystalline film of high quality. RMG of Ge [15] material has become a well-established process with successful device implementations such as finFETs [16, 17] and photodetectors [18]. There are also some reports of RMG of common III–V semiconductors like InAs [19], GaSb [20], and GaAs [21], with very promising material characteristics.

InSb has the smallest direct bandgap (0.17 eV) and highest electron mobility (77 000 $cm^2\,V^{-1}\,s^{-1}$) among the III–V semiconductors. InSb has attracted growing attention in the field of integrated mid-infrared optoelectronics [22] and for topological quantum devices [23]. However, hetero-integration of InSb [24–26] with any common semiconductor substrate is challenging due to its relatively large lattice parameter, a lattice mismatch of 19% to Si, resulting in a higher density of defects when integrated by common epitaxial techniques. InSb high electron mobility transistors [27] and monolithic InSb photodetectors [28] integrated on Si were realized through the use of thick buffer layers. Our aim in this work is to explore the possibility of integrating InSb microstructures on Si, through the RMG technique, despite the huge 19% lattice mismatch. We expect a high crystal quality if the nucleation of InSb is limited to a single nucleation event in a patterned Si seed area that confines the defects generated due to the lattice-mismatch [29]. Liquid phase epitaxy of InSb quantum dots on GaAs results in roughly one nucleation event per 100 × 100 nm^2 area, indicating that it is feasible to achieve the same here [30]. Thus in this paper we present a study on the integration of ultra-thin InSb-on-insulator microstructures on Si substrates using RMG and specifically compare the effect of flash lamp annealing (FLA) versus regular rapid thermal annealing (RTA). Although epitaxial growth of InSb was interfered by the presence of an interfacial layer our results indicate the transformation of amorphous nanocrystalline material to polycrystalline InSb with a few large grains upon annealing, with 10 to 100× improvement in the device resistivity for varying annealing conditions. The process was designed to have a low thermal budget and to be compatible with InSb integration on top of already processed CMOS circuits.

2. Experimental procedure

Sample fabrication started with 3 inch Si (100) wafers, onto which a 40 nm silicon nitride (Si_3N_4) layer was deposited by inductively coupled plasma plasma-enhanced chemical vapor deposition (ICP PECVD) (MicroSystems MS200) at 300 °C using SiH_4 and N_2 precursors. Openings in the Si_3N_4 layer 50 μm long and 70 nm wide were formed using electron beam lithography (EBL) (Raith Voyager) and inductively-coupled reactive ion etching (ICP-RIE) (PlasmaTherm Apex SLR) using CHF_3:N_2 15:85 sccm at 10 mTorr. These openings were intended to enable contact points between the Si and InSb, which we denote as seed areas. A V-groove were formed in the Si in the seed areas by first removing the native oxide layer with a quick buffered oxide etch (BOE) followed by etch in TMAH (25%) at 60 °C. Amorphous InSb (1:1), 30 nm thick, was then deposited using molecular beam epitaxy (MBE) with the substrate held at a temperature of 300 °C at an estimated growth rate of 0.1 ML/s (0.324 Å s^{-1}), based on single crystal growth rates obtained from RHEED oscillations of InAs on InAs substrates. Just prior to deposition the substrate was held at 850 °C for 1 h in the MBE chamber with the aim to evaporate any native oxide in the Si seed area. As InSb is sensitive to the hydroxide-based chemicals used in common lithography processes, the InSb film was covered with a 3 nm Al_2O_3 layer by atomic layer deposition (Cambridge Nanotech) at 200 °C to protect it from the subsequent processing. The InSb layer was patterned into structures 10 μm long with different widths (400 nm, 600 nm, 800 nm, 1000 nm and 1200 nm) using EBL and ICP-RIE (PlasmaTherm Apex SLR) using $CH_4/H_2/Ar$ (6.5:6.5:1) chemistry. The structures were defined so as to overlap the seed area in their central part, resulting in a seed area defined by the intersecting area between the trench and the InSb structure, as is illustrated in figures 1(a) and (b). Structures wider than 400 nm were designed with a narrower region around the trench to limit the seed area width to 400 nm. After resist removal and thorough cleaning the structures were capped by 10 nm additional Al_2O_3 followed by a 950 nm Si_3N_4 layer deposited using PECVD. A schematic of the final sample structure is presented in figure 1(c).

To melt and recrystallize the InSb, the samples were annealed above the melting temperature of InSb (527 °C) using two techniques: RTA (UniTemp RTP) and FLA (Rovak FLA 50/100 AS). The RTA treated sample was annealed to a peak temperature of 530 °C for 1 s, whereas the FLA-treated samples was preheated to a temperature in the range 236 °C–413 °C after which it was exposed to a broad spectrum light flash with a duration of nominally 1.5 ms, and pulse energy of 19.5 J cm^{-2}. The temperature of the RTA system was calibrated by use of the well-defined eutectic temperature of the Si/Au and Si/Al system and any offsets in the measured temperature were taken into account [31]. Temperature measurements in FLA is non-trivial as the flash only heats up the front side of the sample [32–34]. Instead the temperature profile across the sample depth was modeled by a

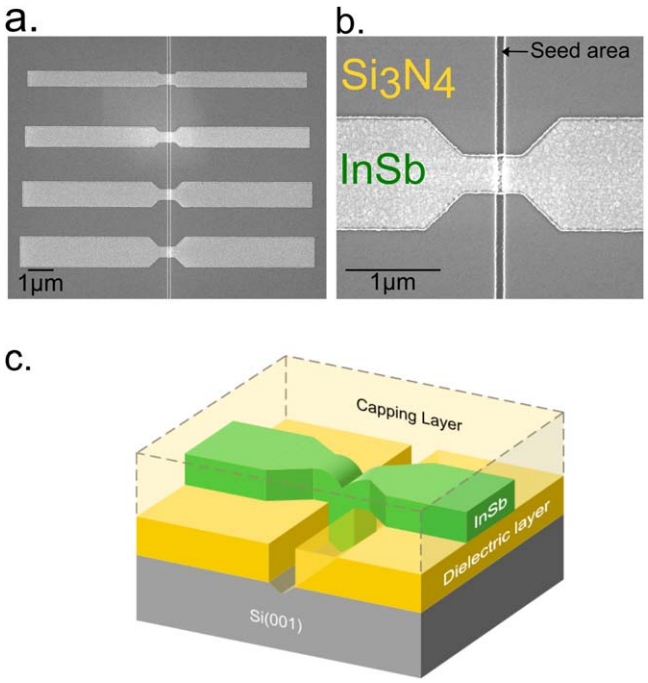

Figure 1. SEM images of MBE deposited amorphous InSb layer after patterning and before melting of (a) InSb double wing structures with varying widths (b) InSb double structure with narrow region near the seed area (c) schematic of the sample structure indicating the narrow Si seed (70 nm), patterned InSb and capping layer. The cavity between the bottom dielectric layer and the capping layer which hold the melt is referred to as the crucible.

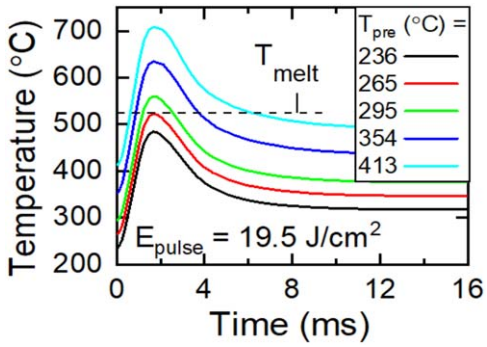

Figure 2. Finite element simulation of the surface temperature variation in samples exposed to 1.5 ms flash duration at 19.5 J cm^{-2} flash energy, with varying preheating temperatures.

finite-element simulation estimating the peak temperature in this process as reaching 492 °C–700 °C, depending on the chosen preheating temperature (figure 2). The assumptions of the model were verified by pyrometer measurements of the backside temperature (see supporting information (available online at stacks.iop.org/NANO/32/165602/mmedia)).

After annealing, the Si_3N_4 capping layer was removed using RIE (Trion Sirus T2 Plus) with SF_6 and O_2 chemistry and the crystallinity and crystal orientation were characterized using scanning electron microscopy (SEM) (Zeiss Gemini SEM 500) equipped with an electron backscattering diffraction (EBSD) detector (Oxford Symmetry).

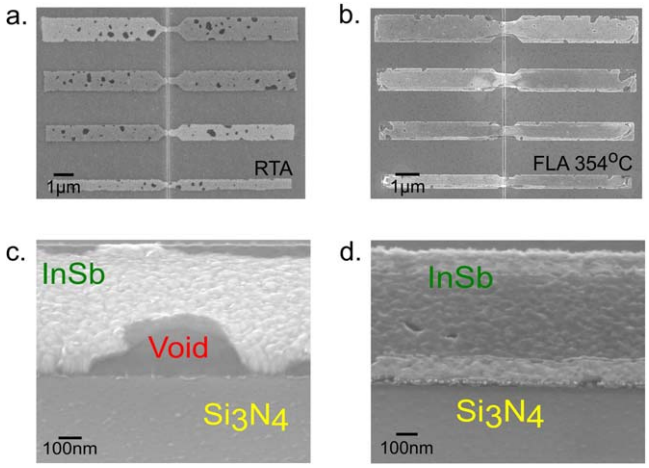

Figure 3. SEM images of InSb structures with varying widths after melting by (a) RTA (b) 354 °C preheated FLA (c) a 52° tilted SEM image depicting the large voids in the RTA annealed sample (d) a 52° tilted SEM image of 354 °C FLA sample showing the smaller voids at the edges of the structure.

For electrical characterization, contacts to InSb structures were fabricated by a lift-off process using EBL of the contact patterns followed by passivation in $(NH_4)_2S$ (20%) and H_2O 1:40 for 90 s at 40 °C. Contact metal with of 20 nm Ni and 120 nm Au was evaporated followed by a lift-off of the resist.

3. Results and discussions

Figure 3 illustrates the first pronounced difference between the RTA and the FLA annealed samples. When heating above the melting temperature using RTA it was observed that large voids are formed in the InSb structures (figure 3(c)), which could indicate loss of material from the crucible during the melting process. Contrary, the samples annealed using FLA had intact InSb structures with no voids visible in the bulk of the structures. On the edges, there are still some loss of material. We attribute the formation of voids to loss of In and Sb by diffusion through the dielectric crucible during the time that the InSb is held in a liquid state above the melting temperature. The markedly smaller degree of material loss for the samples processed by FLA can be explained by the nearly 1000 times shorter time that the sample is held above the melting temperature. Despite that In and Sb diffusion through stoichiometric Si-based dielectrics such as SiO_2 and Si_3N_4 should be negligible at these temperatures there is evidence of enhanced In diffusion if the films contain hydrogen or have low density [35]. Indeed, our Si_3N_4 films are deposited by ICP-CVD at 300 °C, and despite efforts to optimize its stoichiometry they likely contain >10% hydrogen, based on their relatively high etch rate in BOE 1:10 of 2.8 nm min^{-1} and density of 2.6 g cm^{-3} [36]. It is thus plausible that given sufficient time In and Sb could penetrate the crucible in their liquid state. The loss of material at the edges is attributed to a worse quality of the dielectric capping layer at the step edge, as indicated by an enhanced BOE etch rate in these regions. Thus, having excellent dielectric layer quality is essential and

non-trivial given the limited thermal budget in III–V integration. Importantly, FLA mitigates the issue to a large extent and provides a way forward.

3.1. Structural characterization

To study the crystallinity and the crystal orientation of the annealed InSb structures, EBSD measurements were performed. The EBSD reconstructed maps of the FLA processed samples with different preheating temperatures are shown in figure 4. Figure 4(a) presents the SEM image of the 354 °C preheated sample. The colors in the EBSD maps of figures 4(b)–(f) and (i) represent a specific InSb zinc-blende crystal orientation, given by the legend in figure 4(g). From the data in these maps one can thus extract the InSb grain orientation, shape, and size. The EBSD measurement does not discriminate between InSb and the Si seed area which has [001] orientation, visible as a red vertical line on the left side of the maps. Figure 4(b) displays the sample annealed with a preheating temperature of 236 °C (T_{peak} = 492 °C). The EBSD map exhibits single pixel grains (<50 nm), indicating no observable crystallinity at the current measurement resolution. This sample thus appears to have the same amorphous nature as the InSb film after MBE deposition.

In contrast, the samples annealed with the preheating temperature ranging from 265 °C to 413 °C (T_{peak} = 527 °C–709 °C) (figures 4(c)–(f)) consist of only a few large grains with grain size mostly exceeding 1 μm. It is thus evident that heating above the melting temperature results in recrystallization. Figure 4(h) displays the EBSD orientation map (z direction) of an InSb structure on a sample annealed to 530 °C using RTA. Similar to the FLA process, the RTA samples also resulted in grains exceeding 1 μm in size.

Although we expected crystallization to originate from the Si seed area and result in a single epitaxial structure [13, 14], this is not what we observe. The Si seed is visible as a red line at the left edge of the EBSD maps corresponding to Si (100) orientation. We do not see any relation between this and the rest of the InSb material in any of the measured structures, indicating that crystallization has not been preferential at this interface. Indeed, we observe by high-resolution TEM the presence of an unintentional interfacial layer that isolates the InSb from the Si substrate (see supplementary information). Having had no preferential nucleation site, the InSb melt has instead nucleated at random (unseeded) elsewhere in the crucible. Future experiments will have to ensure to avoid the interfacial layer to realize epitaxial InSb. Here we use this opportunity to explore the nucleation properties on the inside of the crucible that must be controlled to enable epitaxy later on.

In order to analyze the EBSD measurement more thoroughly the measurement area was reconstructed using a spline filter and the grain size, defined as the longest diameter of a grain, and the number of grains in each sample area was calculated. Figure 5 shows the grain density for varying FLA

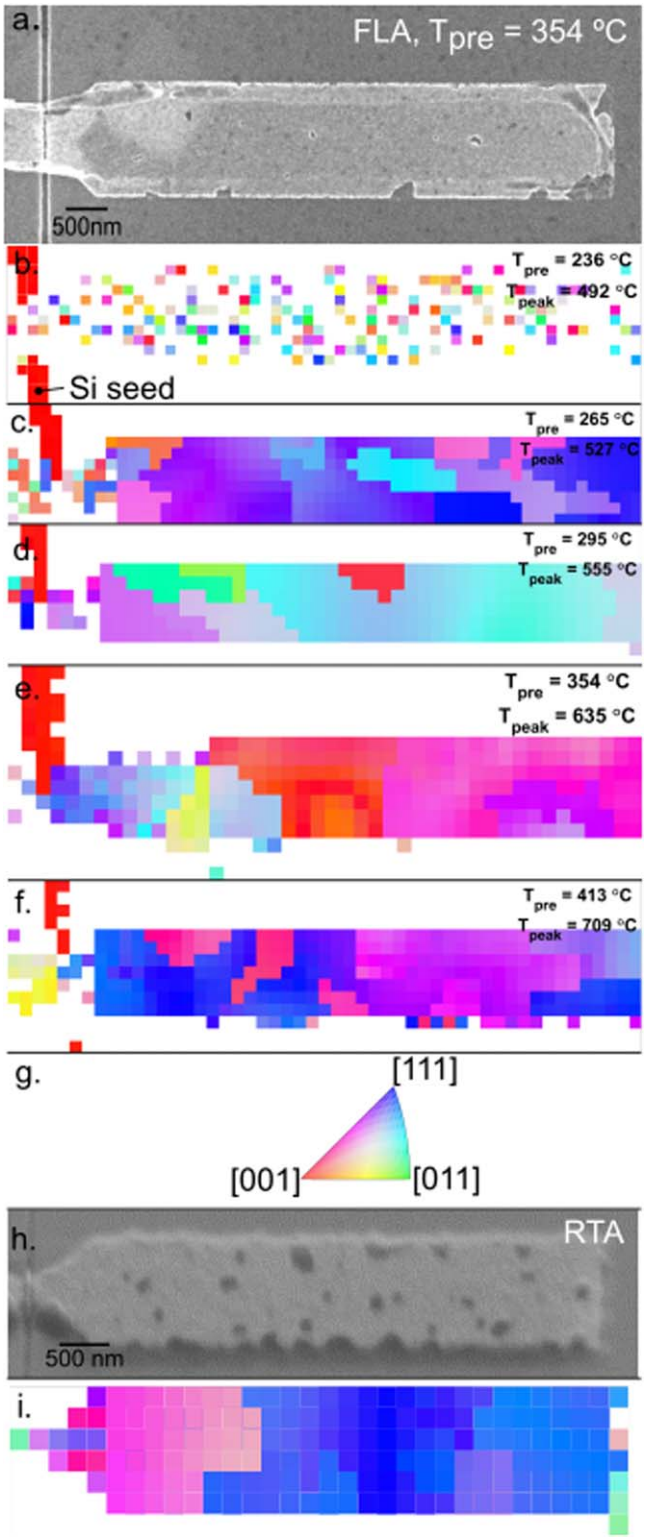

Figure 4. (a) SEM image of the FLA annealed sample corresponding to EBSD Z map(e). (b)–(f) EBSD Z orientation map of 1.5 ms 19.5 J cm^{-2} FLA annealed samples with preheating temperatures (b) 236 °C (c) 265 °C (d) 295 °C (e) 354 °C (f) 413 °C (g) color code representation of orientation of crystal in EBSD map (h) SEM image of 530 °C RTA annealed sample (i) EBSD Z orientation map of RTA annealed structure.

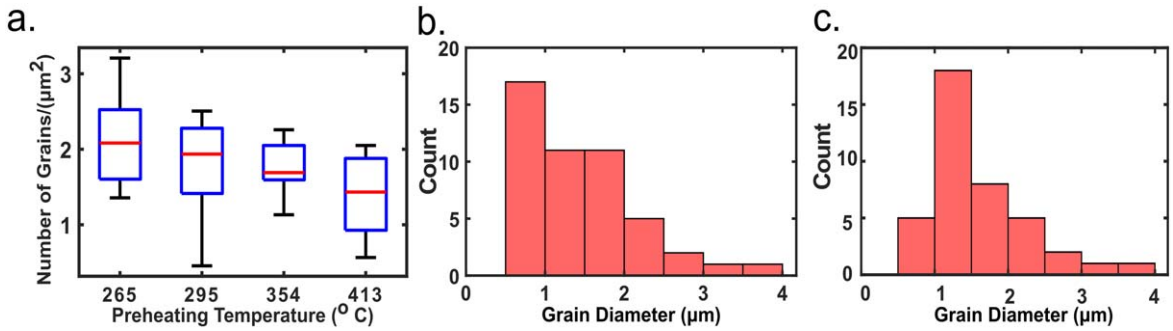

Figure 5. (a) Boxplot showing the variation of number of grains per area for different FLA preheating temperatures where red line corresponds to the median (b) grain size distribution of FLA annealed samples with 413 °C as the preheating temperature (c) grain size distribution of RTA annealed sample (530 °C).

preheating temperatures. Overall, we can see a decline in the number of grains per area (figure 5(a)) with rise in preheating temperature. As the preheating temperature increases, the peak temperature achieved by the flash also increases. The overall declining trend of grain density may be due to fewer nuclei and an increase in growth time with increase in preheating temperature as shown in figure 2.

Figures 5(b) and (c) displays the distribution of grain diameters of FLA annealed samples with $T_{\text{peak}} = 709$ °C and RTA annealed samples, respectively. This particular FLA sample was chosen because it had the lowest grain density among the FLA samples. It was observed that grain size ranging from 1 to 4 μm was obtained through both the processes. The average grain diameter for FLA and RTA annealed samples were 1.5 μm and 1.6 μm, respectively. The similar grain sizes indicate the possibility to achieve the same conditions for unseeded nucleation both in FLA and RTA. With the FLA, the temperature spike leading to melting and return to a much lower equilibrium temperature occurs in the millisecond time frame, after which, a much slower gradual reduction in temperature occurs similar to regular RTA. We hypothesize that unseeded nucleation on the inside of the crucible occurs in this slower cooling phase, which can explain the observed grain size similarity between FLA samples with highest T_{pre} and the RTA sample.

3.2. Growth modeling

To verify the hypothesis given above, and to aid the understanding of the unseeded nucleation and growth process we model the homogeneous nucleation rate, heterogeneous nucleation rate on the crucible wall and the expected melt growth rate of InSb using the thermodynamic model introduced by Liu *et al* [37]. After annealing, when the liquid InSb is cooled, InSb transforms into its solid phase by one of the following process: by heterogeneous nucleation on the inner walls of the crucible (Al_2O_3 or Si_3N_4) or by homogeneous nucleation within the InSb liquid itself. Epitaxial nucleation on the crystalline seed (Si surface) is not considered here because of the interfacial layer in the seed area.

The homogeneous nucleation rate [37] is given by:

$$I_{\text{hom}} = \frac{1}{V_A^{\frac{2}{3}}} v_0 4\pi (r^*)^2 \frac{N}{n^*} \exp\left(-\frac{\Delta G'_M}{kT}\right)\left(-\frac{\Delta G^*}{3\pi kT}\right)^{\frac{1}{2}} \times \exp\left(-\frac{\Delta G^*}{kT}\right), \tag{1}$$

where r^* is the critical radius of the nucleus, N is the total number of atoms in the liquid, n^* is the number of critical sized nucleus for homogeneous nucleation, $\Delta G'_M$ is the activation free energy of an atom jumping across liquid nucleus interface, ΔG^* is the critical free energy change for homogeneous nucleation.

Similarly, the heterogeneous nucleation rate is given by:

$$I_{\text{het}} = \frac{1}{V_A^{\frac{2}{3}}} v_0 2\pi (r^*)^2 \frac{V_A^{-\frac{2}{3}}}{n^*_{\text{het}}} \left(\frac{\Delta G^*_{\text{het}}}{3\pi kT}\right)^{\frac{1}{2}} (1 - \cos\theta) \times \exp\left(-\frac{\Delta G^*_{\text{het}}}{kT}\right)\exp\left(-\frac{\Delta G'_M}{kT}\right) \tag{2}$$

here, n^*_{het} and ΔG^*_{het} are the number of atoms in a critical sized nucleus and the free energy change for the heterogeneous nucleation which is given by the equation:

$$\Delta G^*_{\text{het}} = \Delta G^* S(\theta), \tag{3}$$

$$n^*_{\text{het}} = n^* S(\theta) \tag{4}$$

where $S(\theta) = \frac{1}{4}(2 + \cos\theta)(1 - \cos\theta)^2$ and θ is the contact angle between a spherical cap-shaped nuclei and the crucible wall [37].

After nucleation of an initial crystallite template, atoms can either get attached to the template from the liquid phase or the atoms in solid phase may dissolve in the liquid. The difference of this forward and backward rate gives the growth rate [37]:

$$U = a_0 v_0 \exp\left(-\frac{\Delta G''_M}{kT}\right)\left[1 - \exp\left(-\frac{\Delta g_a}{kT}\right)\right], \tag{5}$$

where a_0 is the interatomic spacing, v_0 is the vibrational frequency of an atom $\Delta G''_M$ is the kinetic barrier of an atom to jump across the liquid crystal interface, Δg_a is the energy

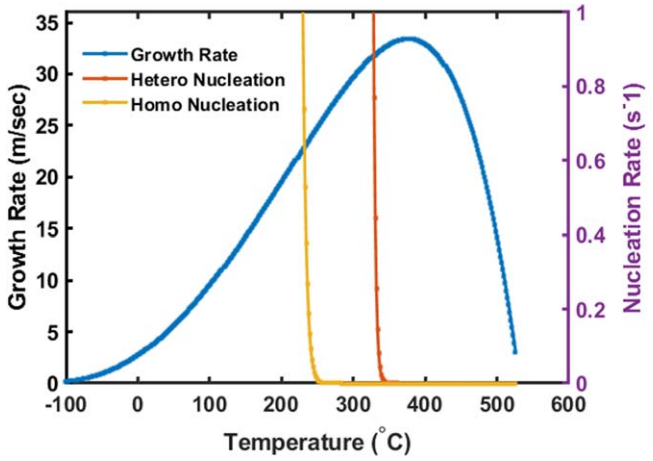

Figure 6. Calculated growth rate, heterogeneous and homogeneous nucleation rate for a liquid InSb microstructure 30 nm thick, 5 μm long and 1 μm wide.

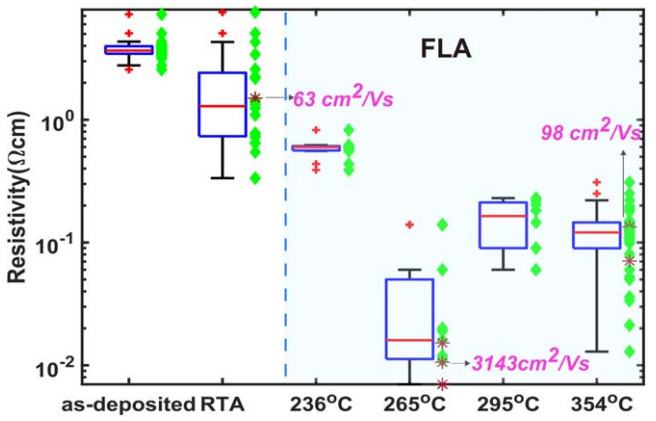

Figure 7. Boxplot comparison of resistivity of the samples before annealing, after RTA anneal and FLA anneal (towards the right of the blue dashed line) with preheating temperatures of 236 °C, 265 °C, 295 °C and 354 °C. The distance between top and bottom of the blue box represents the interquartile range of the sample. The red line represents the median of each dataset and the red cross mark represents the outliers in these datasets. The green diamond markers represent the resistivity data points measured for each annealing technique. The star marker with different shade of red represents the resistivity of the mobility measured sample.

change per atom. All input values are available in the supplementary information table 2.

Simulation results of growth velocity and the nucleation rates are given in figure 6 for an InSb structure 30 nm thick, 1 μm wide and 5 μm long, corresponding to one side of the fabricated InSb structures in this work. It is evident that as the temperature decreases below the melting point, homogeneous nucleation does not become important until around 255 °C, while heterogeneous nucleation becomes important around 343 °C. The rate of InSb crystal growth from the super-cooled melt increases below the melting temperature at 527 °C and reaches a peak of near 30 m s^{-1} at 375 °C. Because the unseeded nucleation rates do not become appreciable until below 343 °C, in the current case in which epitaxial nucleation at the Si seed area is not possible, it is likely that neither nucleation or growth occur until the temperature of the super-cooled melt drops below roughly 340 °C and a first nucleation event on the inner walls becomes probable. This can explain the similar grain sizes observed in both RTA and FLA; although the temperature in FLA cools much faster above and close to the InSb melting temperature, the temperature quickly equilibrates as seen in figure 2. For the samples with the highest T_{pre} the cooling rates are thus similar to RTA around 343 °C leading to similar nucleation and growth rates. To obtain an epitaxial single crystal, it is important that the continued growth after epitaxial nucleation should not be interrupted by unseeded nucleation. We thus observe that there is a process window between approximately 343 °C and 527 °C where both homogeneous and heterogeneous nucleation are insignificant allowing for epitaxial growth to dominate. If the goal is to achieve a single crystal, it is thus vital that the time within this temperature window is sufficient to grow the crystal throughout the whole structure. As the growth rate is very high (m s^{-1}) in this window we estimate that both RTA with seconds of cooling time and FLA with millisecond cooling time should be sufficient to at least grow InSb crystals hundreds of micron in size, as was previously demonstrated for Ge [15, 38]. The modeling presented here thus gives confidence that it will be possible to realize epitaxial single crystalline InSb structures sufficiently large to realize large quantum wire networks (100 × 100 μm^2) and large area InSb photodetectors (10 × 10 μm^2).

3.3. Electrical characterization

Characterization of the electrical resistivity of the InSb structures was carried out by three different techniques: transition line measurements, four probe measurements and Van der Pauw measurements. Importantly, the resistivity values extracted from all three measurement techniques correlate well with each other. It was also observed that the resistivity values were the same regardless of the width of the structure ($p = 0.001$).

Figure 7 shows the comparison of resistivity of as-deposited and annealed InSb structures. The as-deposited InSb exhibits high resistivity with an average of 3.2 Ω cm with small device to device variation. The RTA processed InSb exhibit a much larger variation between devices, with mean resistivity of 1.2 Ω cm. However, the devices which were FLA processed exhibit a reduced resistance when compared to the RTA processed devices. There is a radical shift in the average resistivity between samples with $T_{pre} = 236$ °C and 265 °C which is yet another indication of the effect of achieving full melting and recrystallization of the InSb material. It is also observed that the resistivity of the sample annealed closest above the melting point ($T_{pre} = 265$ °C) has the lowest resistivity with an average of 40 mΩcm when compared to the $T_{pre} = 295$ °C and $T_{pre} = 354$ °C samples with average resistivity of 0.15 Ω cm and 0.12 Ω cm, respectively. Remarkably, despite being polycrystalline material the average resistivity of the $T_{pre} = 265$ °C sample is similar to the resistivity of single-crystalline InSb nanowires grown by vapor–liquid–solid growth with resistivity ranging 45–93 mΩ cm [39]. Although

the observed grain sizes are similar regardless of using RTA or FLA for annealing, the much higher resistivity and larger device-to-device variation resulting from RTA could be due to the high density of voids appearing after the RTA process. Other contributing factors could be surface non-stoichiometry and surface roughness, which is expected to impact the electron transport in these thin InSb layers.

The carrier Hall mobility was measured on Hall cross devices from the FLA samples with $T_{pre} = 265$ °C and 354 °C, and the RTA annealed sample using a Hall measurement set up with variable magnetic field (max 1 T) at room temperature. Three devices from the $T_{pre} = 265$ °C FLA sample were measured giving an average electron mobility $\mu_e = 3143$ $cm^2\,V^{-1}\,s^{-1}$ with an average carrier concentration of 1.89×10^{17} cm^{-3}, whereas two devices in the $T_{pre} = 354$ °C FLA sample gave $\mu_e = 57$ and 139 $cm^2\,V^{-1}\,s^{-1}$ with an average carrier concentration of 7.01×10^{17} cm^{-3}. The mobility of a device on the RTA annealed sample was similar, 63 $cm^2\,V^{-1}\,s^{-1}$ with a lower carrier concentration of 6.5×10^{16} cm^{-3}. The reason for the much higher mobility for the sample with $T_{pre} = 265$ °C (and T_{peak} just above melting) is yet unclear, but we speculate that the much shorter time in the melted state ($T < 343$ °C after ~5 ms, see figure 2) for this sample maintains a better InSb surface that otherwise could limit the electron mobility in these thin devices for which significant electron confinement is expected in InSb [40]. See supplementary information for raw data of Hall measurement on $T_{pre} = 265$ °C FLA sample and a SEM image of a Hall cross device.

4. Conclusion

In this paper we present the integration of ultra-thin InSb on insulator microstructures on to Si by a RMG process using FLA and RTA techniques. EBSD and electrical measurements indicate the transition from amorphous InSb to crystalline structure upon annealing above the melting temperature, with average grain size above 1 μm. We find that FLA provides significantly less loss of material during the RMG process, and markedly lower resistivity and higher electron mobility compared to RTA. The FLA sample annealed closest above the InSb melting point has an average resistivity of 40 mΩcm and an average electron mobility of 3143 $cm^2\,V^{-1}\,s^{-1}$. The results of this study are thus promising for realizing high-quality InSb-on-insulator devices on Si for optoelectronic and quantum applications using RMG.

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