A Fast Transient Response and High PSR Low Drop-Out Voltage Regulator

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***Abstract*—In this paper, a low drop-out (LDO) linear regulator with high power supply rejection ratio(PSR) and fast transient response is proposed for various applications. To achieve fast transient response, this work employs variable bias and transient-boost capacitance. The variable bias structure enhance the slew rate and PSR of LDO. The transient-boost capacitance (TBC) is set in a proper location, using its voltage characteristic to enhance transient response without consuming quiescent current, and it also improves circuit's stability. This circuit is designed based on TSMC 65nm CMOS Technology and verified by Cadence simulation environment. According to the simulation results, the LDO achieves a PSR of 68.3dB and 51.4dB at 10kHz and 1MHz. Undershoot and overshoot of Vout are 190mV and 143mV under a varying load current from 20mA to 80mA with edge time of 1ns.**

***Index Terms*—Variable bias, transient-boost capacitance, LDO, fast transient response, high PSR**

I. Introduction

In CMOS circuit systems, with improvement of the system-on-chip integration and combination of analog and digital circuits in a single chip, ripple from power supply has a great influence on signal propagation. [1] In this case, low dropout linear regulators are always employed as power management to solve this problem. In many portable device applications, it is common for the digital circuit to have many different operation modes. When the digital circuit switches from one operation mode to another, load and output voltage of the LDO can change quickly. [2] Because most digital circuits do not react favorably to large voltage transients, it is necessary to improve the LDO's transient response. In addition, due to large noise generated by RF blocks and DC-DC converter, it is also important for the LDO to have high power supply rejection ratio(PSR) to prevent these noise from being coulped to transmission track. [3] Therefore, designing a stable low dropout linear regulator (LDO) with high PSR, low quiescent current and fast transient response is very important for various applications. However, many previous techniques achieve only one of these advantages or use relatively complicated structure.

In [4], a cross-coupled common gate input stage and adaptive bias circuit is employed to get fast transient response. However, it has a relatively large undershoot/overshoot of Vout, and the transient response can be more fast. Structure and technology also limit its bandwidth and power consumption. Paper [5] presents a LDO with a high pass filter, dual-input transconductance error amplifier, and a mirror NMOS. It achieves good transient response in a wide range of load current change and high PSR over a wide temperature range, and its output current maximum can reach 3 A. Circuit in [6] uses dynamically-biased gain stage and overshoot reduction structure to improve transient response. Its feedback network help lower the quiescent current of LDO and the chip's area. Nevertheless, setting time is relatively long and PSR is relatively low.

This paper presents a LDO circuit that achieves high PSR and fast transient response with variable bias, transient-boost capacitance and NMOS regulation FET. When Vout changes in a short time, the difference from Vref will be amplified and reversed by the folded cascode EA, then goes through unity-gain buffer and NMOS regulation FET to restore the output voltage to the former value. The rest of this paper is divided into three sections. The proposed LDO is discussed in Section 2. The simulation results of the LDO is shown in section 3, and Section 4 is the conclusion of this paper.

II. Design of the Proposed LDO

Fig.1 shows the schematic of the proposed LDO. This LDO consists of a buffer, an error amplifier (EA) with variable bias and transient-boost capacitance (TBC), and an NMOS regulation FET (M_N). The EA in this circuit uses a folded cascode structure to amplify small signal, which provides high voltage gain and high PSR. M_{17}, M_{18} is the input stage of EA, and $M_{15}, M_{16}, M_7, M_8, M_9, M_{10}$ generate bias current for EA. Variable bias structure, which consist of $M_9, M_{10}, M_{11}, M_{12}, M_{13}, M_{14}, M_{15}$, is used to change the bias current of EA when transient load change, thus provides higher slew rate (SR) of EA to enhance transient response. C2 is used to lower undershoot and overshoot of Vout when transient load change. C1 is the transient-boost capacitance (TBC), and its voltage coupling characteristic help to improve transient response. Because this circuit use NMOS as regulation FET, an extra supply power voltage (VDD) is used to power EA, variable bias and buffer to ensure low dropout voltage.

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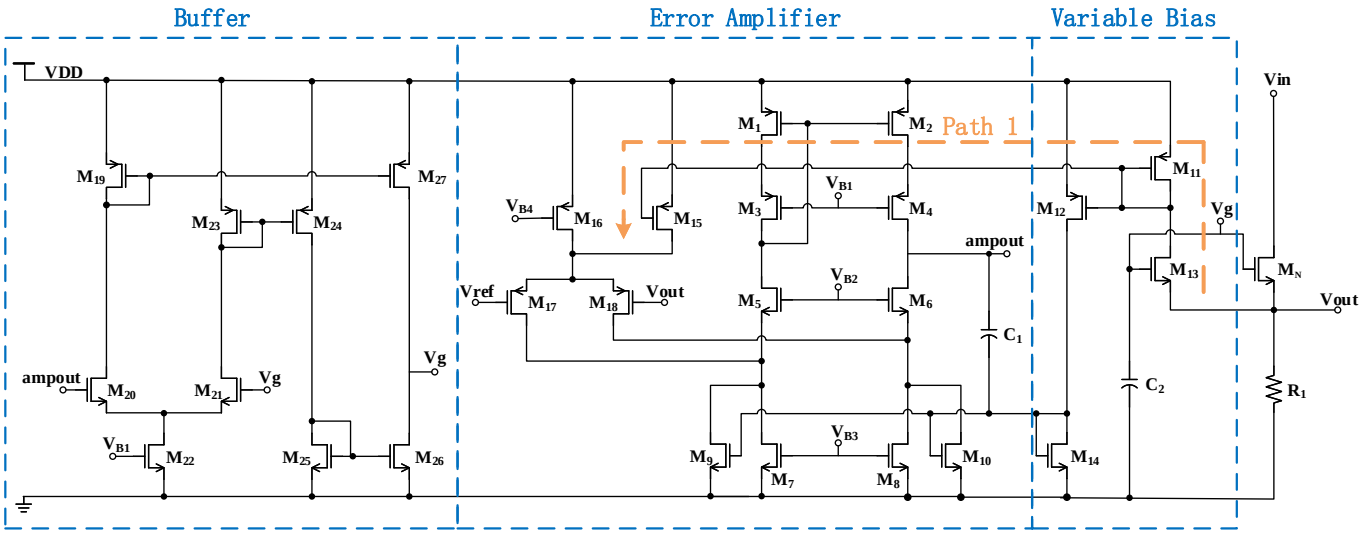

Fig. 1. The Proposed LDO

The dominant pole of this circuit is set at the output node of EA (ampout) due to high output resistance of EA and TBC. And because of lower R_o in TSMC 65nm CMOS Technology, this pole ω_{ampout} is at relatively high frequency, hence obtain bigger GBW(gain-bandwidth product), faster transient response and better PSR. NMOS Regulation FET and cascode structure of EA ensure big resistance seen from VDD to Vout, thus improve the PSR.

A. Variable Bias

In Fig.1, variable bias structure consists of sensing stage (M_{11}, M_{12}, M_{13} , M_{14}), PMOS bias stage (M_{15}) and NMOS bias stage (M_9, M_{10}). M_{13} sense a fraction (1/K1) of I_L flowing through M_N, and M_{12}, M_{14} copy and amplify this current by K2 times. M_9, M_{10} are placed in parallel with M_7, M_8 to copy a fraction (1/K3) of the current flowing through M_{14}. M_{15} is placed in parallel with M_{16} to copy a fraction (1/K4) of the current flowing through M_{11}, M_{13}. During transient load change when Vout sees an undershoot (ΔV_{out}), M_{13} will detects ΔV_{out} and currents flowing through M_9, M_{10},M_{12}, M_{14}, M_{15} will increase, hence the bias current of EA will increase. Assume the increased current of M_{15} all flow though M_{18}, slew rate(SR) of EA can be expressed as:

$$SR = \frac{I_{M8} + (\frac{K_2}{K_1 \times K_3} - \frac{1}{K_1 \times K_4}) \times (I_L + \Delta I_L)}{C_1}$$

I_{M8}, I_L is the current flowing through M_8, M_N in quiescent mode (I_L hasn't changed). Because $\frac{K_2}{K_1 \times K_3} \gg \frac{1}{K_1 \times K_4}$, so the SR of EA is improved when Vout undershoots (ΔI_L>0).

As shown in Fig.1, PMOS bias stage (M_{15}) forms another negative feedback loop (Path 1) for the ripple of input voltage (Vin), hence enhance the PSR of LDO. When voltage ripple of Vin couple to Vout, the conventional negative feedback loop is through M_6, M_{18}, M_N and buffer to dampen the ripple coupled to Vout, which is a main function of a traditional LDO. In this work, with PMOS bias stage of variable bias structure, another negative feedback loop consist of M_6, M_{11}, M_{13},M_{15}, M_{18},buffer is employed to enhance the dampening effect, thus significantly improve the PSR of the circuit.

B. Transient-boost Capacitance (TBC)

The TBC (C1) is employed between the gate of NMOS bias stage (M_9, M_{10}) in variable bias and output node of EA (ampout). During transient load change, Vout will increase/decrease, and V_{ampout} will decrease/increase due to the negative feedback loop. Using the characteristic of a capacitance that transient voltage change of one end of C1 will be coupled into the other end, increase/decrease of ampout will help the gate voltage(V_G) of M_14, M_{10}, M_9 to increase/decrease and vice versa. And because V_G of M_14, M_{10}, M_9 have the same trend of V_{ampout} during transient load change, a capacitance between these two nodes will improve transient response.

In small signal analysis, because ω_{ampout} is the dominant pole, TBC will push this pole to a lower frequency, hence improve LDO's phase margin and stability. Moreover, employing TBC brings an zero as shown in Fig.2, which improve gain bandwidth (GBW) and phase margin. While achieving all these advantages mentioned above, employing TBC doesn't bring any more quiescent current.

C. Buffer Stage

In a LDO, output resistance of EA is usually big due to its high gain, and gate parasitic capacitance of regulation FET is also big because of its large width-length ratio. So, if EA directly connect to regulation FET, there will be a pole at very low frequency, which could cause small GBW and slow transient response. To avoid this situation, a buffer is always employed in LDO circuits to separate the big resistance and capacitance. In this paper, an unity-gain buffer

with operational transconductance amplifier and current mirror serves that function.

M_{20} and M_{21} form the input stage of this unity-gain buffer, and M_{22} generates the bias current for the amplifier inside. M_{19}, M_{23}, M_{24},M_{25}, M_{26}, M_{27} copy and amplify the current flowing through M_{20}, M_{21} to the output side, putting big current in just one road, thus consume less quiescent current compared to conventional unity-gain buffer and improve SR at the same time. Because higher SR brings faster speed when voltage changing, this buffer helps to improve LDO's transient response.

D. NMOS Regulation FET

Because gate parasitic capacitance(C_G) of NMOS regulation FET is much smaller than PMOS FET, the second dominant pole ω_{vg}(this pole is at the gate of M_N) is at higher frequency, so it can achieve a wider gain bandwidth and a fast slew rate. It also improves the load transient response including settling time and undershoot/ overshoot of output voltage, and the PSR of the LDO in high frequency. Besides, NMOS regulation FET forms a source follower structure which has relatively low output resistance. It ensures the output pole at high frequency in a wide range of load change, thus maintains a good loop stability even in light current load.

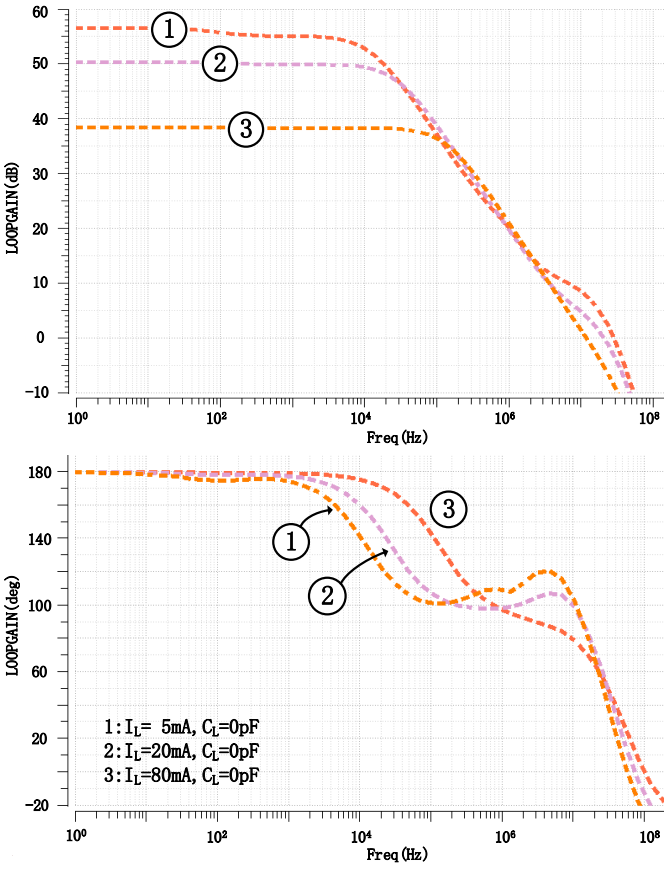

Fig. 2. Simulated loop-gain and phase

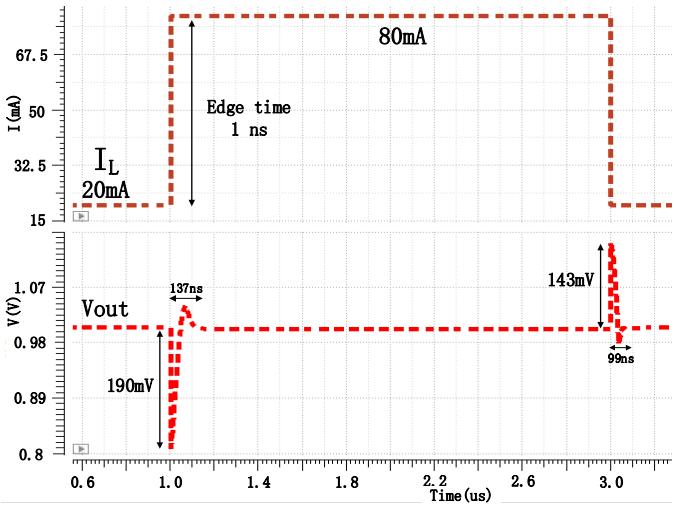

Fig. 3. Simulated load transient response

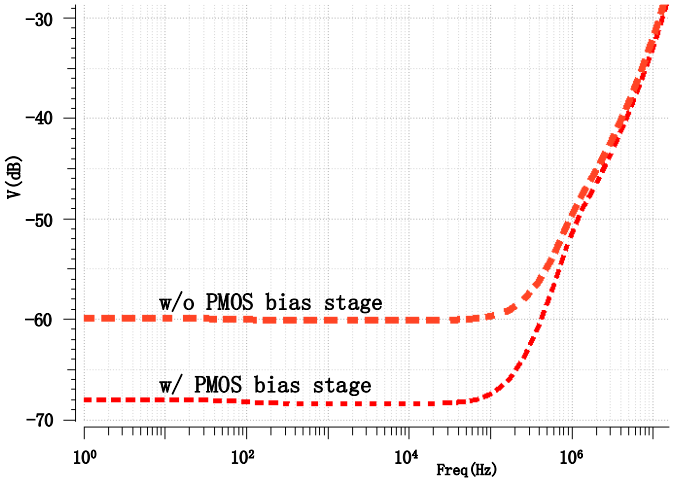

Fig. 4. Simulated PSR w/ and w/o PMOS bias stage at I_L = 5 mA

III. SIMULATION RESULTS

The proposed LDO regulator is designed in TSMC 65nm CMOS Technology and simulated by Cadence simulation environment. Vout of this LDO is 1V and Vin is 1.2V, thus the dropout voltage is 200mV. The simulated I_Q of the whole circuit is 58.2 μA. The loop-gain and phase of this LDO is shown in Fig.2 at $I_L = 5, 20, 80mA$, $C_L = 0pF$.

In Fig.3, transient load response is simulated at $C_L = 0pF$. Setting time of Vout from undershoot/overshoot is 137ns/99ns when load current varies from 20mA to 80mA with a rise/fall time of 1ns. The undershoot/overshoot voltage of Vout is 190mV/143mV.

Fig.4 shows the simulated PSR of 68.3dB and 48dB at 10kHz and 1MHz. The figure also shows the simulated PSR of 60dB at 10kHz when PMOS bias stage (M_{15}) of variable bias is disabled. By comparison, PMOS bias stage help increase PSR at low frequency by 14%.

Table.I summarizes different performance parameters of the presented LDO and compares them with prior arts designed

TABLE I
COMPARISON WITH PRIOR ARTS

Parameter	**This work**	2014 [3]	2013 [6]	2012 [7]	2014 [8]	2018 [9]	2016 [10]	2019 [11]
Max I_L (mA)	**80**	10	100	200	50	100	30	10
Vin/Vout (V)	**1.2/1**	1.15/1	1.2/1	2.07-5.5/1.03	0.75-1.2/0.55	1.2/1	2.4-2.6/1	1.2/0.9-1.1
I_Q (μA)	**58.2**	50	0.9-82.4	176	200	102	161	28/3
ΔV_{out} (mV)	**190**	43	68.8	104	24	37	195	40
sim/measured	**simulated**	measured	measured	measured	measured	simulated	measured	simulated
$T_{setting}$ (ns)	**137**	0.65	6000	$\sim$60	250	$\sim$340	$\sim$500	$<$1000
Edge time (ns)	**1**	0.2	300	16	100	80	0.2	100
ΔI_L (mA)	**60**	10	100	149	49	98	30	9
PSR(dB)@Hz	**68.3@10k 51.4@1M**	15.5@1G	58@10k	50@1k	51@1k	-	40@10k	26@1M
FOM(mV) [6]	**0.92**	0.22	0.93	9.8	48.98	15.4	1.05	6.67

with the same 65nm technology. To compare the load-transient response performance of different LDO, the edge-time of load step, undershoot of Vout voltage and I_Q are all key factors. In [6], the figure-of-merit (FOM) is presented to compare transient response performance:

$$FOM = K(\frac{\Delta V_{out} \times I_Q}{\Delta I_{LOAD}})$$

K is a ratio:

$$K = \frac{\Delta t \ used \ in \ the \ measurement}{the \ smallest \ \Delta t \ among \ designs \ for \ comparison}$$

A small FOM means the LDO achieves good transient response. FOM of this LDO is calculated as 0.92mV, and is relatively small due to low I_Q and small edge time. PSR is relatively high as shown in Table.I, and maintains a high value over 1 MHz.

IV. CONCLUSION

In this paper, an NMOS low dropout regulator using variable bias and transient-boost capacitance is presented. With zero load capacitance, the proposed LDO has 190/143 mV undershoot/overshoot of output voltage and 135 ns settling time when load current changing from 20 to 80 mA in 1 ns edge-time. And it achieves a PSR of 68.3dB and 51.4dB at 10kHz and 1MHz.

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