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Nanoribbon-Based Flexible High-Performance Transistors Fabricated at Room Temperature

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Si-nanoribbon-based high-performance field-effect transistors (FETs) with room temperature (RT)-deposited dielectric are presented. The distinct feature of these devices is that the high-quality SiN_x dielectric deposition at RT, directly on the transfer-printed nanoribbons, is compatible with most flexible substrates. The performance of these FETs (mobility ≈656 $cm^2 V^{-1} s^{-1}$ and on/off ratio >10^6) is on par with the highest performance of similar devices reported with high-temperature processes, and significantly higher than devices reported with low-temperature processes. The transfer and output characteristics of nanoribbon-based field-effect transistors under planar, tensile, and compressive bending and multiple bending cycles (100) show excellent mechanical stability of the devices as they retain performance. The device characteristics are also compared with the equivalent simulation data. The excellent response of nanoribbon-based FETs and the fabrication compatibility with diverse flexible substrates makes the presented approach attractive for flexible electronics applications such as conformal tactile active matrix sensors for e-skin, where high performance is needed.

1. Introduction

Recent progress in flexible electronics[1] has enabled advances in several emerging applications such as wearable electronics,[2] electronic skin,[3] epidermal electronics,[4] flexible display,[5] etc. Many of these applications require fast computation and communication, which require performance at par with Si-based technology. The thin films of organic semiconductors,[6] 2D layered materials,[7] inorganic amorphous oxides,[8] etc., which have been widely explored in recent years lead to devices with modest performance as a result of their low mobility (1–10 $cm^2 V^{-1} s^{-1}$ against ≈1000 $cm^2 V^{-1} s^{-1}$ by Si devices) and large device channel lengths (>20 µm), etc.[9] In this regards, the ultrathin chips[10,11] have partly helped to meet the performance requirements, even if their application is limited to small and compact areas as for economic reasons and integration related difficulties it is not practical to have them over the large areas. As a result, the printed devices and circuits based on nanostructures (NSs) of high-mobility materials such as Si nanowires (NWs), Si nanoribbons (NRs), carbon nanotubes (CNTs), GaAs NWs, etc. have been explored.[12–14] The excellent performance (e.g., high mobility and On/Off ratio) offered by some of the NS-based devices is summarized in **Table 1**. A major challenge with NSs based devices is that some of the critical fabrication steps (e.g., NSs fabrication/growth, doping, high-k dielectric deposition) require high-temperatures that are incompatible with the flexible substrates such as plastics.

Currently, the popular method to address this issue is to transfer print NSs from the native or growth substrates to the receiving flexible substrate using a stamp or career substrate.[12,15,16] Since the high temperature fabrication steps are carried out before transfer (i.e., when NSs are still on the native or growth substrates), this method decouples the high temperature process steps from the low-temperature steps (e.g., metallization) that are carried out after transfer to realize devices on flexible substrates, as shown in **Figure 1**. Previous works have carried out most of the steps, including high temperature dielectric deposition which yielded good device characteristics,[17,18] before transfer printing. Transfer printing of such fully formed field effect transistors (FETs) increases the process complexities which also raises the technology cost. An alternative method is to use substrates such as metal foils, which can withstand higher processing temperatures. However, additional fabrication steps such as insulation on foils increase the cost of fabrication and for this reason manufacturing through low-temperature processing steps is preferred. The low-temperature processing keeps the transfer printing process highly robust and could aid fabrication of FETs over large area flexible substrates as it is compatible with methods such as roll-to-roll technology. Thus, key challenge is to develop high-performance NRFET by dielectric deposition preferably at room temperature (RT). Many experimental techniques, such as atomic layer deposition (ALD), low-pressure chemical vapor deposition (LPCVD), plasma-enhanced (PE)-CVD, inductively coupled plasma (ICP)-CVD, e-beam evaporation, etc., have been successfully used to develop high quality dielectric films in the past.[19] ALD and LPCVD techniques typically use growth temperatures in

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Table 1. Si membranes or NR-based FETs with various reported gate dielectrics.

S. no.	Dielectric	Dielectric deposition temperature [°C]	Si Micro/nanostructure morphology	Source	Channel dimensions			Mobility [$cm^2 V^{-1} s^{-1}$]	On/off ratio	Ref.
					L [µm]	W [µm]	T_{Si} [nm]			
1	≈2 µm SU-8	RT	Sub-µm ⟨111⟩ ribbons	Bulk ⟨111⟩ Si	100	10	115–130	360 (Lin.) 100 (Sat.)	≈10^3	15b
2	≈15 nm SAND[a)]	RT	µs-Si	SOI	250	100	300	680	>10^7	30
3	≈90 nm Tg-SiO_2	1100	Fully formed n-type MOSFETs	Custom SOI with ⟨111⟩ base	20	150	≈2000	≈710 (Lin.) ≈600 (Sat.)	>10^6	17
4	200 nm a-SiO	RT	Sub-µm membranes	SOI	1	2 × 20	200–300	423		31b
5	100 nm PECVD SiO_2	250	Fully formed n-type NR MOSFETs	Custom SOI with ⟨111⟩ base	10	40	≈100	650 (Lin.) 530 (Sat.)	>10^5	18
6	100 nm RT ICP CVD SiN	RT	Nanoribbons–ribbon length (55 µm)	SOI	5	50 (5 × 10)	70	656 (Lin.)	>10^6	This work

[a)]Self-assembled nanodielectrics.

excess of 250 °C, which are not suitable for direct deposition of dielectrics over flexible materials. Similar issue arises using PECVD along with additional problems such as plasma-induced damage, active layer degradation, high charge trapping, increased concentration of defects (dangling Si bonds), Ohmic contact degradation, etc.[20] In this regard, the ICP-CVD offers unique advantage as it allows high quality dielectrics (SiO_x, SiN_x etc.) at room temperature without any harmful effects.[21,22] SiN_x is a widely explored gate dielectric material for III–V devices and oxide thin film transistors exhibiting good performance.[20]

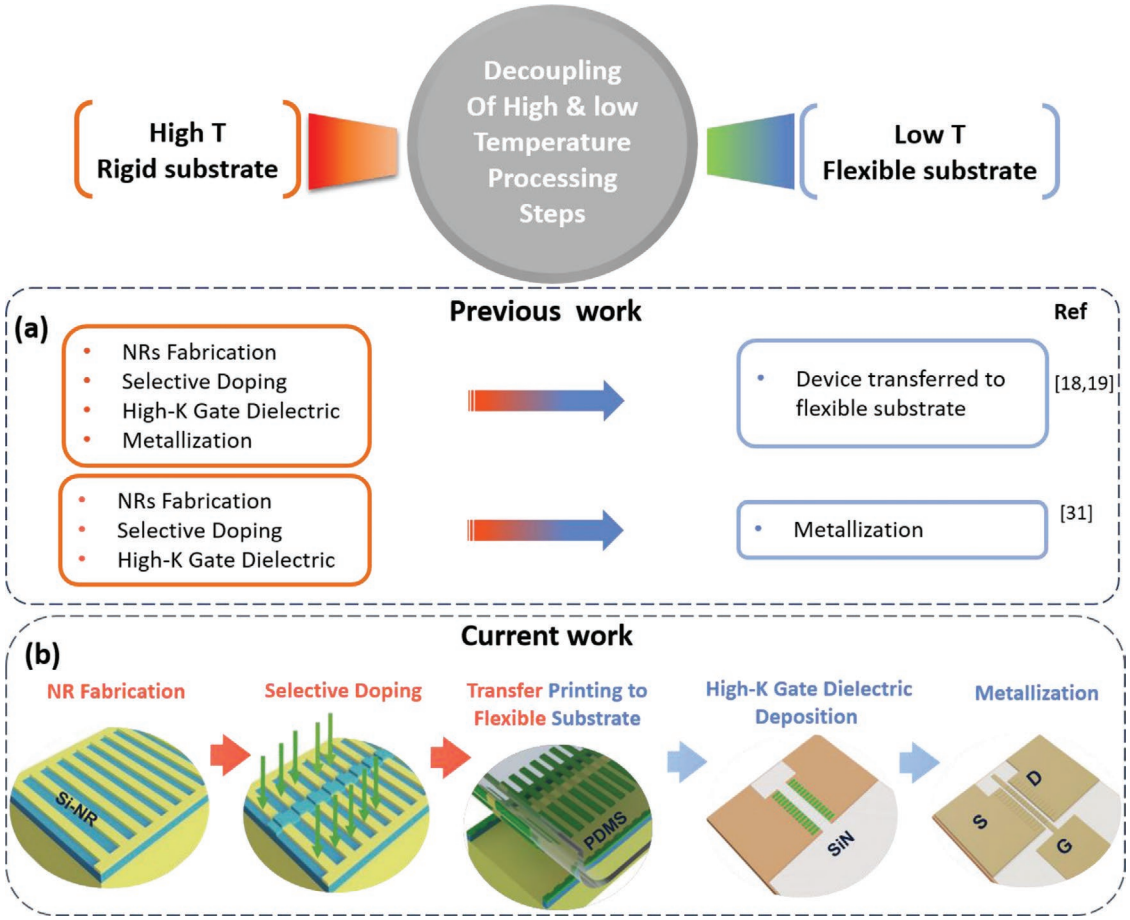

Figure 1. Overview of the NRFET fabrication by transfer printing process with transition from high to room temperature steps. a) The previously reported works have majority of the fabrication steps requiring high temperature. b) The critical fabrication steps in this work are carried out at low temperature regime suitable for flexible electronics.

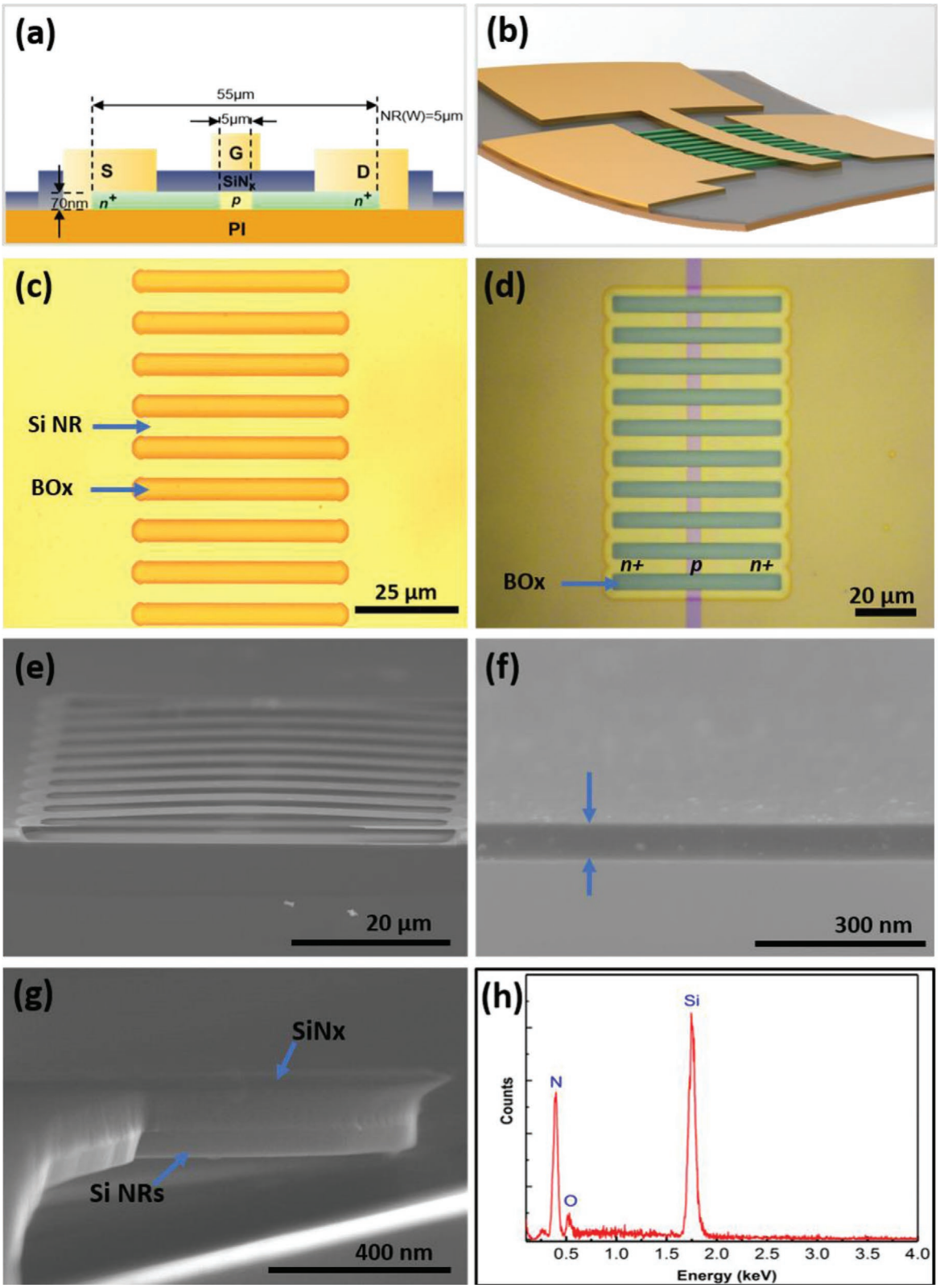

Figure 2. a) Schematic 2D cross-sectional structure of the single NRFET. b) Schematic 3D illustration of the array of NRFETs on flexible substrate. Structural characterization of Si NRFETs at various fabrication stages. c) Si NRs definition and d) selective doping at source and drain regions. (e) Cross-section SEM image of suspended NRs array. f) Cross-section of single Si NR structure. g) Cross-section of Si NRs with SiNx dielectric. h) EDX spectrum of the SiNx dielectric film.

Herein, we demonstrate the flexible Si NRs (5 μm (L) × 50 μm (W) × 70 nm (T)) based FET (**Figure 2**a,b) developed over flexible PI substrates using a room temperature ICP-CVD deposited SiN_x (100 nm thickness) as the gate dielectric. The SiN_x dielectric film was observed to be very smooth (≈0.4 nm roughness), crack-free, and deposited with high stoichiometry (Si:N ratio). The low deposition temperature, appreciable dielectric constant (≈9), low interface traps, CMOS compatibility, combined with ICP-CVD process is highly beneficial for Si NRFETs, which operate with high ON/OFF ratio (>10^6), low leakage current, and high mobility (≈656 cm^2 V^{-1} s^{-1}) under multiple mechanical bending cycles. The NRFET device characteristics show that the low temperature SiN_x dielectric film holds advantage compared to the SiO_x and a-SiO deposited using other techniques. The RT ICP-CVD dielectric deposition process is compatible with flexible polymeric substrate could be key step forward for the development of high-performance large area flexible Si NRFETs.

2. Results and Discussion

Si NRFETs fabrication process involves four major steps: 1) chemical etching, 2) n+ doping of source and drain regions, 3) transfer printing, and 4) FETs fabrication. The detailed fabrication processes are illustrated in Figure S1 of the Supporting Information. The schematic diagram of the obtained devices and the microscopy images of various stages of the development of flexible Si NRFET are shown in Figure 2, respectively. The selective wet etching of top Si layer results in well-defined Si NRs with uniform interspacing (Figure 2c). The channel region was protected from source and drain n+ spin-on-doping process by the SiO_x mask (Figure 2d). The devices have a channel length of 5 μm, gate overlap length of 5 μm, and the effective channel width of 50 μm (10 ribbons × 5 μm each). The BO_x layer etching process led to the suspended Si NRs strongly anchored at both NR ends with the Si layer (Figure 2e). As observed in the cross-sectional image of Si NRs (Figure 2f), the etching process produced smooth sidewalls without any undercut. The process steps depicted through microscopy images in Figure 2c–e were carried out using a commercial SOI wafer resulted in suspended Si NRs array. The transfer printing is introduced at this stage and the remaining steps in the device fabrication are carried out at low temperature (Figure 1). The microstructure of RT ICP-CVD deposited SiN_x dielectric thin film (thickness 100 nm) over Si NR is shown in Figure 2g. The key factors that govern the effectiveness of any dielectric materials are internal stress, chemical composition, surface roughness, interfacial defects, etc. These factors are mostly influenced by their deposition technique. Here, the dense dielectric film was found to be uniform across the NR thickness with good surface adhesion. Typically, the tensile stress in dielectric films promotes cracking and compressive stress enhances its peeling. The microscopic observations (Figure 2g) show that these were found to be absent in the SiN_x film. The stoichiometry of the SiN_x analyzed using EDX measurement (Hitachi SU8240-EDX) (Figure 2h), shows strong peaks of Si and N with an estimated Si/N ratio ≈0.7, which is close to the stoichiometry of Si_3N_4. The weak oxygen signal could have raised from the ambient or surface adsorbed atoms. The good stoichiometry ratio of Si/N confirms the high quality of film deposited at the room temperature. This eliminates the issues with other deposition processes such as LPCVD and PECVD, which deteriorate the flexible substrates and the channel. For example, high energy plasma could affect both the PI substrate and the NRs surface, which eventually affects the device performance. Various stages of Si NRFETs fabrication are presented in Figures S2–S5 of the Supporting Information. **Figure 3**a shows the SEM image of an NRFET, comprising of ten nanoribbons as active channel, with the source (S), drain (D), and gate (G). Figure 3c shows the photograph of fabricated Si-NRFET array with RT deposited ICP-CVD SiN wrapped around a vial with radius of curvature 7.5 mm. The devices were tested using Cascade Micro-tech Auto-guard probe station interfaced to an Agilent B1500A semiconductor device parameter analyzer. The fabricated device was tested for their flexibility and mechanical stability as illustrated in Figure 3d to observe the effect of bending stress. For this purpose, the device arrays were placed on to 3D printed convex and concave structures both with radius of curvature of 40 mm. In convex bending, the device comes under tensile stress whereas its experience compressive stress comes in the case of concave bending. The transfer and the output characteristics of the transistor are shown in **Figure 4**a,b, respectively. The mechanical bending and the resulting strain are known to affect the band structure of the material, which affects the effective mass and hence the mobility of the charge carriers.[10,23] Analytical equations relating the stress with the mobility and drain current can be used to model these variations[10,24]

$$\mu_{(\text{stress})} = \mu_{\text{o}} \left(1 \pm \Pi_{\mu} \sigma \right) \tag{1}$$

where μ_0, μ_{stress}, Π_{μ}, and σ are the mobility under normal condition and stressed condition, piezoresistive coefficient, and the stress, respectively. Since the NRFET are fabricated as n-channel device, the resistance decreases with tensile bending as it leads to overall increase in the current. Conversely, the compressive strain leads to decrease in the drain current. This is reflected both in the transfer characteristics and the output characteristics. **Table 2** indicates a summary of the main parameters calculated using the electrical characterization of the fabricated NRFET under planar and bent conditions. The effective surface mobility μ_{eff} was calculated by using following equation

$$\mu_{\text{eff}} = \frac{L}{W} \frac{g_{\text{d}}}{C_{\text{ox}} \left(V_{\text{GS}} - V_{\text{th}}\right)} \tag{2}$$

where L and W refer to the channel length and the effective width of the NRFET, g_{d} is the drain conductance, C_{ox} is the oxide capacitance, V_{GS} is the gate source voltage, and V_{th} is the threshold voltage. Since the NR is 70 nm thick, the thickness was considered negligible and the effective width was considered as 50 μm (10 ribbons × 5 μm each). The threshold voltage (extracted from linear extrapolation method[25]) is –0.87 V, which may not be suitable for CMOS digital application because of the high current at V_{GS} of 0 V. However, this could

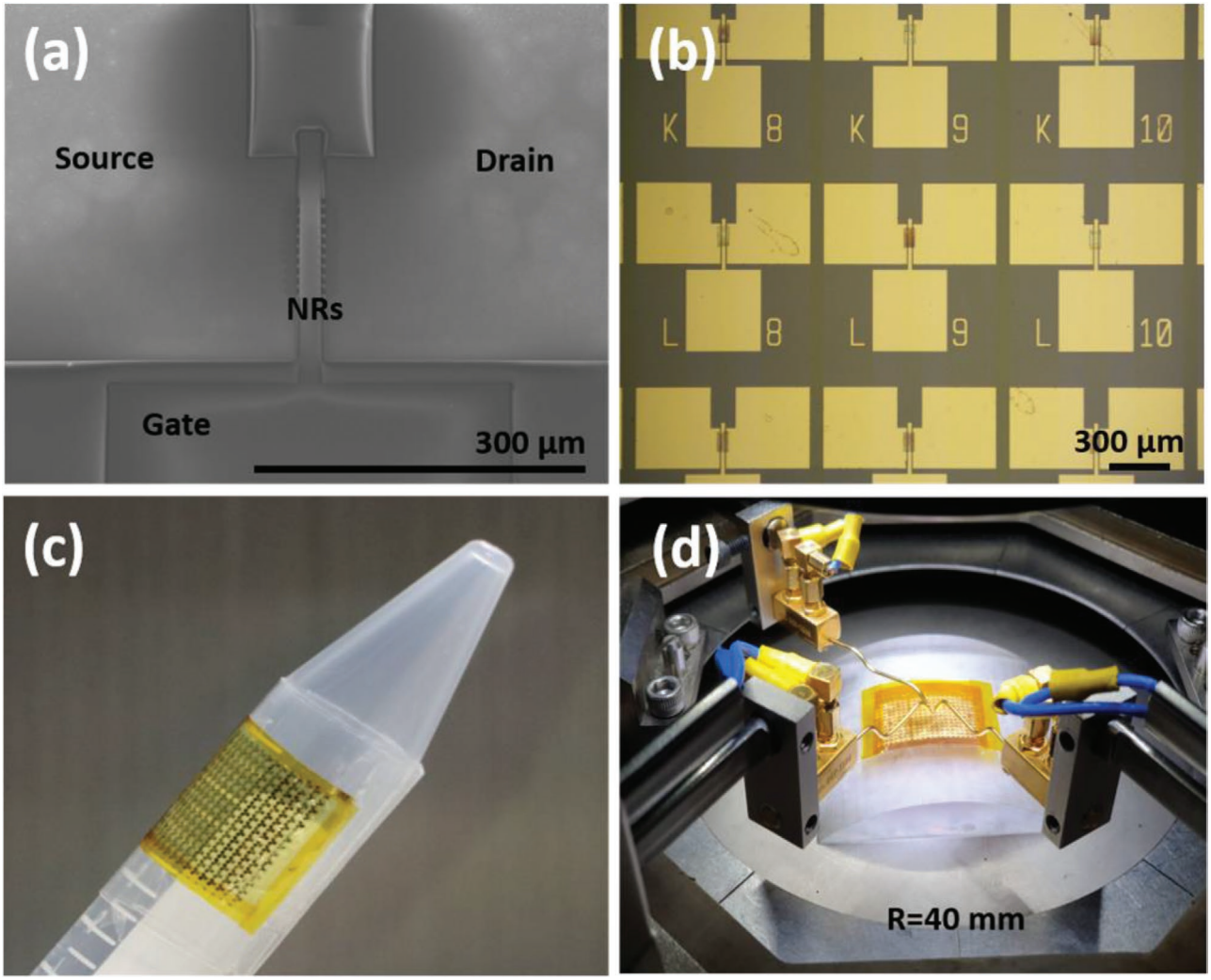

Figure 3. a) SEM image of a representative NRFET with the source (S), drain (D), and gate (G) electrodes labeled in it comprising of ten nanoribbons as active layer. b) Optical microscopy image of NRFETs array transferred on PI substrate. c) Photograph of flexible NRFETs on PI substrate wrapped on a curved surface. d) Illustration of electromechanical characterization of the fabricated NRFET with bending.

be tuned by channel ion implantation or by optimizing the work function of the gate metal to push the threshold voltage toward enhancement mode operation. The drain conductance is given by the equation

$$g_{\mathrm{d}} = \frac{\partial I_{\mathrm{D}}}{\partial V_{\mathrm{DS}}} \Big| V_{\mathrm{GS}} = \text{constant} \tag{3}$$

Based on the obtained output characteristics, the drain conductance at tensile, planar, and compressive conditions were estimated by numerically differentiating the drain current with reference to the drain-source voltage and their values were 42.72, 41.28, and 40.08 µS µm^{-1}, respectively. Peak transconductance (g_{m}) of the NRFET was calculated under planar and bending conditions, by numerically differentiating the values extracted from I_{D}–V_{GS} data, using a Matlab according to the following equation

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{D}}}{\partial V_{\mathrm{GS}}} \Big| V_{\mathrm{DS}} = \text{constant} \tag{4}$$

The estimated effective surface mobility for the three conditions, tensor, planar, and compressive were 679, 656, and 637 cm^2 V^{-1} s^{-1}, respectively.

The performance of NRFETs is compared in Table 1 with previous works based on Si-membrane/ribbon-based devices with best reported performances for various dielectric materials. In this regard, NRFETs with ultraviolet (UV) curing and spin-coating of SU8-5 have been explored in past as the gate dielectric.[15,26] Spin-coating leads to nonuniform films compared to other conventional processes such as CVD, thermal oxidation or ALD.[27] The devices using SU-8 based dielectric showed ≈360 cm^2 V^{-1} s^{-1} maximum linear-regime electron mobilities ($\mu_{\text{e-lin}}$) and the on-to-off ($I_{\text{on}}/I_{\text{off}}$) ratio in the order of 10^4.[15,26] Other low-temperature gate dielectric deposition is the PECVD-based silicon oxide (PEO), which resulted in $\mu_{\text{e-lin}} \approx 650$ cm^2 V^{-1} s^{-1} and $I_{\text{on}}/I_{\text{off}}$ of 10^6.[18,28] However, 250 °C, at which the PEO was deposited, is suitable only for high heat-resistant polymers such as polyimide (PI).[29] The highest mobility (≈710 cm^2 V^{-1} s^{-1}) with Si NSs has been achieved with

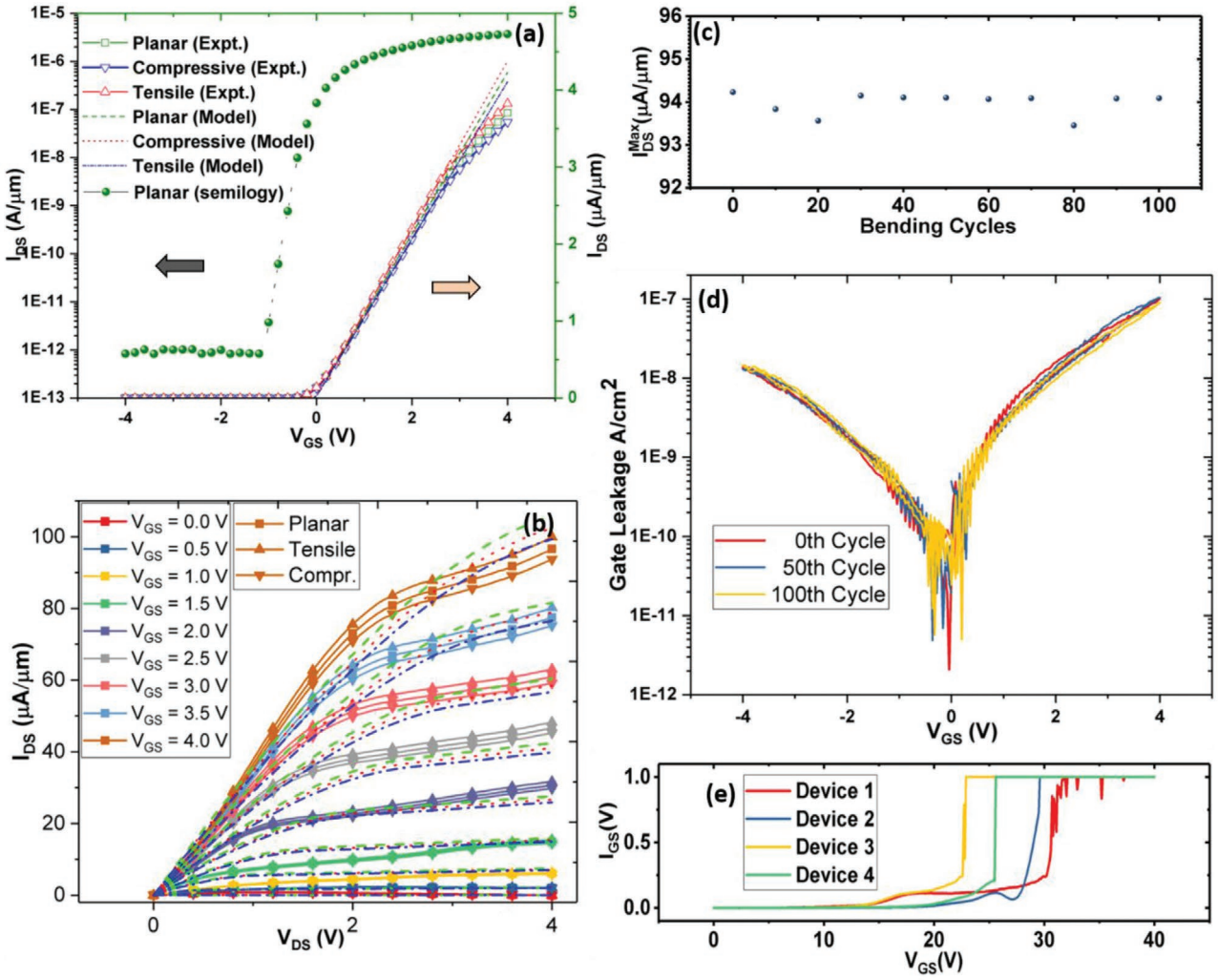

Figure 4. a) Transfer characteristics (experimental (line) versus model (dashed) simulations) and b) output characteristics of the NRFET at planar, tensile, and compressive bending conditions (R_c = 40 mm). c) Variation of the drain current at planar condition after cycles of compressive and tensile bending at $V_{DS} = V_{GS} = 4$ V. d) Gate dielectric leakage current V_s gate voltage after subjecting it to cyclic bending. e) Breakdown voltage characteristics of four randomly chosen devices after subjecting to cyclic bending of 100 cycles.

thermally grown SiO_2 as dielectric, where instead of membranes or ribbons, the process has been modified to transfer print fully fabricated FETs to destination substrate.[17,18] The comparison with previous reports (Table 1) shows that the characteristics of the device with room-temperature processed dielectrics are not at par with the high temperature deposited dielectrics.

The saturation mobility (μ_{sat}) of the presented device obtained from its output characteristics under planar condition is 612 cm^2 V^{-1} s^{-1} while it was 632 and 594 cm^2 V^{-1} s^{-1} with convex

Table 2. Various parameters related to NRFET characteristics.

Parameters	Tensile strain	Planar	Compressive strain
Bending radius of curvature R_C	40 mm (convex)	–	40 mm (concave)
Effective mobility (experimental) μ_{eff}	679 cm^2 V^{-1} s^{-1}	656 cm^2 V^{-1} s^{-1}	637 cm^2 V^{-1} s^{-1}
Saturation mobility (experimental) μ_{sat}	632 cm^2 V^{-1} s^{-1}	612 cm^2 V^{-1} s^{-1}	594 cm^2 V^{-1} s^{-1}
Saturation current ($I_{D\text{-}sat}$) at $V_{DS} = V_{GS} = 4$ V	96.24 μA μm^{-1}	93.67 μA μm^{-1}	90.86 μA μm^{-1}
Drain conductance (g_d)	42.72 μS μm^{-1}	41.28 μS μm^{-1}	40.08 μS μm^{-1}
Transconductance (g_m)	1.129 μS μm^{-1}	1.093 μS μm^{-1}	1.058 μS μm^{-1}
Gate delay	1.49 ns	1.54 ns	1.59 ns

(tensile) and concave (compressive) strain tests, respectively. The saturation currents (at $V_{DS} = V_{GS} = 4$ V) were 96.24, 93.67, and 90.86 μA μm^{-1} for tensile, planar, and compressive conditions, respectively. The on-to-off current ratio for the device was 4.4×10^6 or 6.644 decades. This is slightly lower than the previously reported value employing SAND dielectric (15 nm).[30] Further improvement could be achieved by using a thinner SiN_x dielectric. At the subthreshold regime, the subthreshold swing (SS) was extracted from the logarithmic transfer characteristics by numerical differentiation based on the equation

$$SS = \frac{1}{\partial \log(I_D)/\partial V_{GS}} \tag{5}$$

The subthreshold slope was found to be 182 mV per decade. This value is significantly higher than previously reported a-SiO while the SAND dielectric has better subthreshold performance.[30,31] This could be further enhanced by reducing the thickness of the gate dielectric, thereby the gate can have a better control on the channel. The approximate gate delay for a typical CMOS application assuming a fanout (fn) of 2 and symmetric balanced CMOS (i.e., μ_{eff}, L, and W of n-MOS and p-MOSFET) was indirectly calculated from the below equation[32]

$$\tau_{GD} = \frac{12\,\mathrm{fn}}{\mu_{eff}} L_{Min}^2 \frac{V_{DD}}{(V_{DD} - V_{th})^2} \tag{6}$$

The calculated gate delays were 1.49, 1.54, and 1.59 ns for tensile, planar, and compressive conditions, which imply ≈650 MHz operation assuming V_{DD} of 4 V. This can be further improved by reducing the gate length and improving the operating voltage (engineering the capacitance and the threshold voltage). The cyclic bending impact on the performance of the device was also evaluated.

The peak values of the drain current (at $V_{DS} = V_{GS} = 4$ V) were obtained under planar condition after every 10 cycles of compressive and tensile bending ($R_c = 40$ mm). A total of 100 bending cycles were performed and the result is shown in Figure 4c. It can be observed that the device performance in terms of the drain current remains unchanged even after 100 bending cycles with negligible variation in the gate leakage current (less than 1%). The maximum gate leakage current density was ≈10^{-7} A cm^{-2} at 4 V. In order to evaluate the gate breakdown voltage after applying cyclic bending test of 100 cycles, four randomly chosen NRFET devices were characterized and the results are shown in Figure 4e. The breakdown field strength of the dielectric was >2.2 MV cm^{-1}, which is excellent for a room temperature deposited gate dielectric.

3. Conclusions

This paper presented the silicon nanoribbon-based FETs with room temperature deposited SiN_x gate dielectric on flexible substrate and exhibiting excellent performance (mobility ≈656 cm^2 V^{-1} s^{-1} and On/Off ratio >10^6), which is at par with highest performing devices reported thus far. The mechanical flexibility, robustness, and stability were investigated by performing tensile and compressive cyclic bending measurements. The room temperature ICP process adopted here for the deposition of high-quality dielectric (SiN_x) of thickness 100 nm leads to enhanced device performance. This is evident from the distinctive enhanced performance of developed device in comparison with other devices based on RT deposited dielectric materials. The RT process used in this paper is combatable with low temperature polymer materials, which means the NRFETs on various flexible substrates can be used as building blocks for applications requiring high-performance flexible electronics such as conformal tactile active matrix sensors for e-skin.

4. Experimental Section

Si NRFETs have been realized using commercial SOI wafers, which consist of 70 nm top Si (100) layer over 2 μm of buried oxide, supported by 600 μm bulk Si (Figure S1, Supporting Information). The diced wafer samples were cleaned using acetone, iso-propyl alcohol (IPA) and deionized (DI) water to remove the surface contaminants. Si NRs (5 μm (*W*) x 60 μm (*L*)) were defined by employing spin-coated S1805 photoresist (4000 rpm for 30 s), followed by soft baking at 115 °C for 60 s (Figure S1a–d, Supporting Information). The samples were exposed to UV source (Suss MicroTec-MA6) for 4 s and subsequently the NRs patterns were developed by using MF 319. The etching of UV exposed Si regions, using solution of nitric acid, ammonium fluoride, and DI water for an optimized 120 s, resulted in the array of NRs attached with Box (Figure S1d, Supporting Information). The unexposed photoresist was removed using acetone and IPA. The selective source–drain doping (Figure S1e–h, Supporting Information) of NRs was carried out using 150 nm thick SiO_x mask layer deposited using PECVD (Figure S1e, Supporting Information). The source and drain regions of NRFET were defined over SiO_x mask layer by spin-coating photoresist (S1805, 4000 rpm) followed by UV exposure (3 s) (Figure S1f, Supporting Information). The exposed SiO_x mask areas were etched by reactive ion etching using a combination of CH_3/Ar gas sources (Figure S1g, Supporting Information). The high temperature selective doping of source/drain regions was carried out in a resistive heating tubular furnace system under inert N_2 gas ambience. The spin-on doping of phosphorus (P509, Filmtronics, USA) was carried out at 950 °C selectively on source/drain areas. This step could be avoided by using a doped wafer and this could lead to NEFRTs will all RT fabrication steps. Further, the SiO_x dopant diffusion barrier layer was removed using buffered oxide etchant (BOE-5:1). At this stage, the Si NRs with defined source/drain regions were firmly attached with the bottom BO_x layer (Figure S1h, Supporting Information). A wet etching step using HF acid leads to the releasing of NRs from the bulk wafer with anchoring points at both ends (Figure S1i, Supporting Information). The doped NR arrays were then transferred to polyimide foils using an intermediate PDMS stamp (Figure S1j, Supporting Information). A thin PDMS stamp (Sylgard 184 with 10:1 ratio of base and curing agent) of ≈2 mm thickness was prepared by casting and curing on a bare Si wafer. The PDMS stamp with a gentle pressure (≈50 kPa) over the suspended NR array aided the transfer printing over designated polyimide foils. The transfer of NRs over PI substrates was enhanced by adhesion promoter, VM652, followed by wet etching of the PDMS stamp (1 wt% of tetrabutylammonium fluoride in propylene glycolmethyl ether acetate)[33] (Figure S1l, Supporting Information). The process ensured that the integrity of as fabricated NRs was preserved during transfer printing over PI foils. Further, the gate dielectric film, SiN_x (100 nm), was deposited over NRs using RT ICP-CVD system[22] (Figure S1m, Supporting Information). The optimized SiN_x recipe consisted of SiH_4/N_2 flow rate 7/6 sccm, ICP source RF power of 100 W; chamber pressure of 7 mTorr. The source and drain regions were selectively patterned by dry etching of SiN_x. The metal contacts (Ti (10 nm)/Au (90 nm)) for gate, source, and drain were deposited using e-beam evaporation tool (Figure S1p, Supporting Information).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

flexible electronics, flexible FETs, field-effect transistors, transfer printing

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