Demonstration of Genuine Surface Inversion for the p/n-$In_{0.3}Ga_{0.7}Sb$-Al_2O_3 MOS System with in-situ H_2 Plasma Cleaning

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Results of an investigation into the impact of in-situ H_2 plasma exposure on the electrical properties of the p/n-$In_{0.3}Ga_{0.7}Sb$-Al_2O_3 interface are presented. Samples were processed using a clustered inductively coupled plasma reactive ion etching (ICP-RIE) and atomic layer deposition (ALD) tool. Metal oxide semiconductor capacitors (MOSCAPs) were fabricated subsequent to H_2 plasma processing and Al_2O_3 deposition and the corresponding capacitance-voltage (CV) and conductance-voltage (GV) measurements were analyzed quantitatively via the simulation of an equivalent circuit model. Interface state (D_{it}) and border trap (N_{bt}) densities were extracted for samples subjected to the optimal process, with a minimum D_{it} of 1.73×10^{12} eV^{-1} cm^{-2} located at ~110 meV below the conduction band edge and peak N_{bt} approximately aligned with the valence and conduction band edges of 3×10^{19} cm^{-3} and 6.5×10^{19} cm^{-3} respectively. Analysis of the inversion response in terms of the extraction of the activation energy of minority carriers in inversion (p-type) and the observation of characteristics which pertain to minority carriers being supplied from an external inversion region (n-type) unequivocally demonstrate that the Fermi level is unpinned and that genuine surface inversion is observed for both doping polarities.

Antimony-based compound semiconductors are promising candidates for future complementary metal oxide semiconductor (CMOS) devices,[1] tunnel field effect transistors (TFETs),[2] and mid infrared optoelectronics.[3] Unlike other III-V compounds, antimonides exhibit excellent transport properties[4] for both electrons and holes and therefore could circumvent the bottleneck in III-V p-type metal oxide semiconductor field effect transistor (MOSFET) performance. Accordingly, both p and n-type antimonide based MOSFETs have the potential to produce significantly higher on-currents than their Si counterparts at a given supply voltage, V_{DD}.[5] Thus, in comparison to Si CMOS, an antimonide based CMOS technology could enable either: clock frequencies to be increased without increasing power consumption (due to a reduced CV/I gate delay)[6]; or power consumption to be decreased without degrading on-state performance.[6] Furthermore, an all III-V antimonide based CMOS technology would offer substantially reduced fabrication complexity in comparison to hybrid CMOS, where p and n-type devices of different (largely lattice mismatched) materials require co-integration on a common substrate, and each device polarity has a significantly different thermal budget.[7] $In_xGa_{1-x}Sb$ ternary compounds offer the combined optimal performance for electrons and holes in the same material[8]: the incorporation of In maintains excellent electron transport,[8] while room temperature (RT) hole mobilities as high as 1,500 $cm^2V^{-1}s^{-1}$ have been demonstrated in strained p-$In_{0.4}Ga_{0.6}Sb$ quantum wells.[9] As such, complementary devices which have a common channel material of $In_xGa_{1-x}Sb$ have the potential to offer the simplest manifestation of III-V CMOS, where p and n-type devices can be fabricated with a unified process. Forming an unpinned dielectric interface to InGaSb with a low interface trap density (D_{it}) is critical in order to fully exploit its advantageous material properties. To date, while InGaSb devices have been demonstrated,[8,10–17] systematic studies on improving the electrical properties of the dielectric interface to antimonides have been limited to GaSb[13,14,16,18–26] and InSb[27–33] only. For the former, ex-situ HCl[13,14,17,20] and $(NH_4)_2S$[18,21,22] surface treatments, and in-situ H_2 plasma exposure[23–26] have yielded promising results. In this paper we report on the impact of in-situ H_2 plasma exposure on the electrical properties of the $In_{0.3}Ga_{0.7}Sb$-Al_2O_3 interface.

$In_{0.3}Ga_{0.7}Sb$ epitaxial layers were grown by molecular beam epitaxy (MBE) on heavily doped GaAs (100) substrates. An InSb mole fraction of 30 % was chosen as simulations have shown mole fractions between 20-40 % to offer the maximum drive current for n-type devices[8]: increasing the In concentration increases the injection velocity, V_{inj}, and decreases the density of states (DOS), and mole fractions between 20-40 % yield the optimal trade-off between these two parameters.[8]

The complete layer structure comprised, from the substrate-up: 250 nm GaAs regrowth; a 200 nm GaSb relaxed buffer; a 3 μm $In_{0.3}Ga_{0.7}Sb$ buffer; and a 500 nm $In_{0.3}Ga_{0.7}Sb$ capacitor layer. The regrowth and buffer layers were doped to a nominal value of 1×10^{18} cm^{-3}, while the $In_{0.3}Ga_{0.7}Sb$ capacitor layer was uniformly doped at a nominal value of 2×10^{17} cm^{-3}. Both p (Zn doped substrate, Be doped epitaxial layers) and n-type (Si doped substrate, Te doped epitaxial layers) variants were grown.

Prior to H_2 plasma exposure, all samples were subjected to an ex-situ HCl surface clean (HCl:H_2O, 1:2, for 3 minutes, followed by rinsing in isopropyl alcohol) and subsequently

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loaded into a central vacuum load lock, which is part of a clustered inductively coupled plasma reactive ion etching (ICP-RIE) and atomic layer deposition (ALD) tool. Samples were exposed to the H_2 plasma in the ICP-RIE chamber with varying exposure times. The following ICP-RIE parameters were common to all samples: H_2:Ar (1:7) plasma chemistry, 150 W ICP power, 2 W platen power, 90 mT chamber pressure and 150°C platen temperature. Following H_2 plasma treatment, samples were transferred under vacuum to the ALD chamber where Al_2O_3 was deposited via 80 cycles (8 nm nominal thickness) of a thermal ALD process at 200°C using trimethyl-aluminium (TMA) and H_2O as precursors. Immediately prior to Al_2O_3 deposition, the samples were exposed to in-situ TMA pulses (30 cycles, 20 ms TMA exposure, 3 s Ar purge), which has demonstrated a self-cleaning effect for other III-Vs.[34–36]

Metal oxide semiconductor capacitors (MOSCAPs) were fabricated with circular gate diameters ranging from 50 to 250 μm in size. The gate metal (20 nm Pt/200 nm Au) was deposited by ebeam evaporation through a shadow mask. Subsequently, the samples were annealed in forming gas (H_2:N_2, 5%:95%) at 350°C for 15 minutes. Ti/Pt/Au (30/50/100 nm) ohmic contacts were formed to the substrate via blanket metal deposition using ebeam evaporation to the back of the sample.

The impact of H_2 plasma cleaning on the electrical properties of the interface was assessed using variable temperature (RT to $-50°C$), multifrequency (1 kHz to 1 MHz) capacitance-voltage (CV) and conductance-voltage (GV) measurements, which were acquired using a Keysight B1500A semiconductor parameter analyser in conjunction with a microchamber probe station (Cascade Summit 12971B). Measurements were recorded in a dark, dry air (dew point < $-65°C$) environment.

Fig. 1 shows RT CV measurements for p-type MOSCAPs processed with H_2 plasma cleaning times of 1, 10 and 30 minutes, in addition to a control sample which had no plasma exposure. The gate leakage current for all samples was <1× 10^{-7} A/cm^2 at an applied gate voltage, V_g, of ± 2 V (not shown). The capacitance modulation, C_{mod} (where C_{mod} = (C_{max}-C_{min})/C_{max} at 1 MHz), of all samples which included H_2 plasma cleaning was significantly greater than the control; indicating an increased freedom of Fermi level movement.[37] The 1 minute sample exhibited the largest C_{mod}, with a value of 73.78 %. This degraded with increasing plasma exposure time and decreased to 61.36 % for the 10 minute sample and to 41.06 % for the 30 minute sample. Interestingly, the maximum capacitance in accumulation, C_{max}, increased with increasing plasma exposure time: with reference to the control, C_{max} increased by 8.11 %, 14.64 % and 16.48 % for 1, 10 and 30 minute samples respectively. Further research is required to determine the impact of H_2 plasma cleaning on the chemical composition of the InGaSb-Al_2O_3 interface and how this relates to the effective oxide permittivity and magnitude of D_{it}. This, however, is beyond the scope of this paper. The frequency dispersion in accumulation was extremely low for all samples, with a value of 1.1 %/Dec. for the 1 minute sample. A correlation has been shown to exist between frequency dispersion in accumulation and MOS device reliability,[38] and this therefore may have important ramifications for III-V p-type devices. The minimum measured capacitance of the 1 minute sample closely approaches its theoretical minimum value based on the nominal doping density ($C_{\text{min,theory}}$ = 187 nF/cm^2, shown in Fig. 1 by the black dashed line). This is not the case for any of the other samples which clearly have limited Fermi level movement away from the valence band edge.

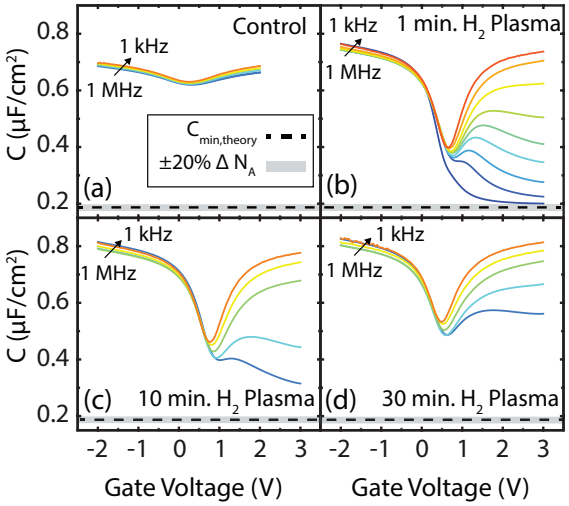

FIG. 1. RT CV measurements over a frequency range of 1 kHz to 1 MHz for p-type Au/Pt/Al_2O_3/$In_{0.3}Ga_{0.7}Sb$ MOSCAPs, processed with H_2 plasma cleaning times of (a) 0, (b) 1, (c) 10 and (d) 30 minutes.

It should be noted that the inclusion of the above-discussed forming gas anneal (FGA) appears to be critical in order to fully obtain the benefits of H_2 plasma cleaning on the electrical properties of the $In_{0.3}Ga_{0.7}Sb$-Al_2O_3 interface, since the optimal electrical characteristics cannot be achieved with H_2 plasma cleaning in isolation, without FGA treatment, or vice versa (the Reader is referred to the supplementary material). Further investigation may be required to optimise this annealing process, however, this is beyond the scope of this paper.

Fig. 2 shows RT and low temperature (-50°C) CV measurements for both p and n-type MOSCAPs processed with a 1 minute H_2 plasma clean. Unlike the p-type sample, the n-type sample does not reach its theoretical minimum value. This may lead one to infer that Fermi level is pinned towards the conduction band edge, assuming that the doping density of the n-type sample is not significantly higher than the nominal value. For the same gate stack process to be applicable to both p and n-type InGaSb MOSFETs, it is critical that the Fermi level at the InGaSb-dielectric interface is unpinned so that both device polarities can turn on. Accordingly, in order to discern if the Fermi level is indeed pinned, or if it is unpinned and genuine minority carrier responses are observed, the following presents a comprehensive analysis of the inversion response of both p and n-type MOSCAPs processed with a 1 minute H_2 plasma clean.

For the n-type sample, it was observed that at fixed measurement frequency, the capacitance in inversion increased

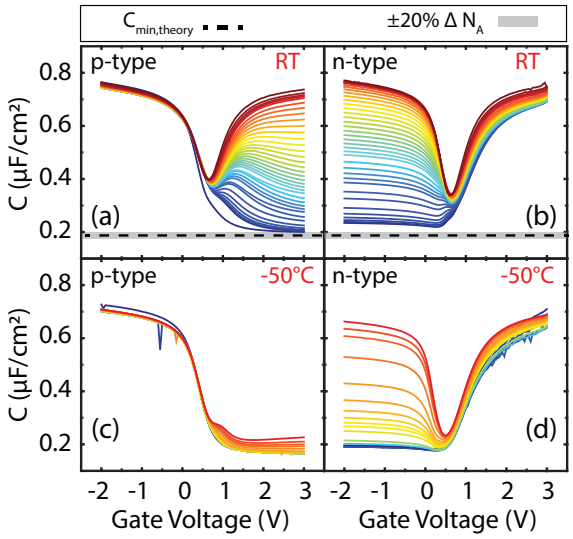

FIG. 2. RT and low temperature (-50°C) CV measurements over a frequency range of 1 kHz to 1 MHz for p and n-type Au/Pt/Al_2O_3/$In_{0.3}Ga_{0.7}Sb$ MOSCAPs, processed with a H_2 plasma cleaning time of 1 minute.

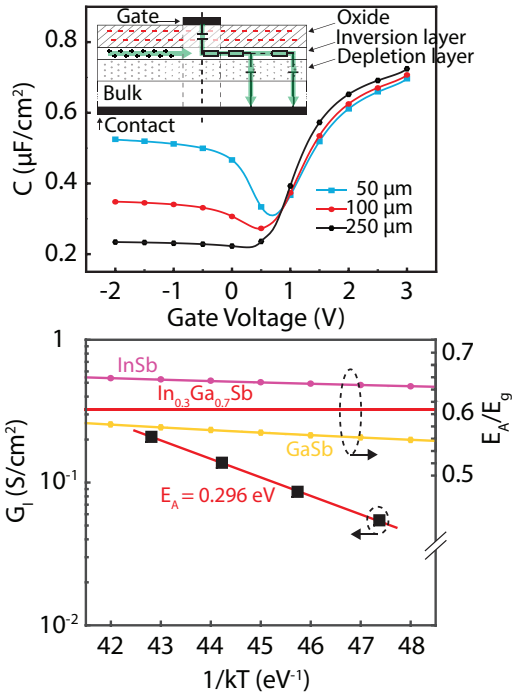

FIG. 3. (a) RT CV measurements at 1 MHz for the n-type Au/Pt/Al_2O_3/$In_{0.3}Ga_{0.7}Sb$ MOSCAP processed with a H_2 plasma cleaning time of 1 minute, for gate diameters of 50, 100 and 250 μm. Inset: schematic of an n-type MOSCAP with negative charge in the oxide causing a peripheral inversion layer. (b) Left-hand y-axis: Arrhenius plot of the equivalent parallel conductance in inversion ($V_g = 3\ V$), G_I, against 1/kT for the p-type Au/Pt/Al_2O_3/$In_{0.3}Ga_{0.7}Sb$ MOSCAP processed with a H_2 plasma cleaning time of 1 minute. Right-hand y-axis: the calculated activation energy associated with n_i for InSb and GaSb, normalised to their respective bandgap energies. This was calculated by taking $\frac{d}{d(1/kT)} ln(n_i)$, where the empirical relation of $n_i(T)$ was known for InSb and GaSb from Refs. 41 and 42 respectively.

with decreasing gate area. This is shown in Fig. 3(a) at a frequency of 1 MHz for gate diameters of 50, 100 and 250 μm. Such a dependancy is a signature of genuine surface inversion with minority carriers supplied from an external inversion layer situated beyond the periphery of the gate (resulting from charge in the oxide). In such a case, the dominant mechanism over all temperatures by which minority carriers are supplied to the inversion layer beneath the gate is diffusion from the externally inverted surface (depicted in the left hand side of the MOS schematic inset to Fig. 3(a)).[39] The gate area dependance of the measured capacitance arises due to the increasing diffusion distance with increasing gate size from the externally inverted surface to the centre of the gate. The existence of this mechanism is further validated by the fact that the inversion response is not suppressed at low temperature (Fig. 2(d)) as minority carriers supplied in this manner are not thermally generated. These characteristics cannot be explained by D_{it} and unequivocally demonstrate a genuine minority carrier response. With regards to the theoretical minimum capacitance, it can be seen in Fig. 2(b) and (d) that the true high frequency CV response of the n-type sample is not observed for any measured frequency or temperature: each dataset features a distinct minimum in measured capacitance at $V_g \sim 0.4\ V$. This is a further consequence of an external inversion layer: at high frequency, the minority carriers cannot follow the applied AC signal and thus the surface beneath the gate remains inverted and acts as a conductor through which AC current can flow laterally beyond the gate edge into the external inversion layer. The semiconductor beyond the gate edge behaves as a distributed R-C network[40] (depicted in the right hand side of the schematic inset to Fig. 3(a)). As the gate bias is pushed further into inversion, the coupling between the inversion layer beneath the gate and the external R-C network increases, and thus the measured capacitance increases.[40] Consequently, this mechanism masks the true high frequency response and it is suggested that this results in the discrepancy between the measured and nominal theoretical minimum capacitance of the n-type sample, for which there is explicitly a genuine minority carrier response.

It should be noted that there are no ramifications due to the presence of the above-discussed external inversion layer on the performance of a corresponding inversion mode p-type MOSFET, where minority carriers would be injected into the channel from the highly-doped source of the MOSFET, and not supplied from the external inversion layer. The characteristics observed in the n-type CV measurements due to the external inversion layer are merely an artefact of the MOSCAP test set up used, which, advantageously, we have been able to exploit in order to discern genuine surface inversion.

The above characteristics were not present for the p-type MOSCAP, which is to be expected as the same oxide charge which peripherally inverts the n-type surface, will accumulate, not invert, the p-type surface.[39] In order to discern a genuine inversion response for the p-type sample, the activation energy, E_A, of minority carriers was extracted from an

Arrhenius plot of the equivalent parallel conductance in inversion, G_I, versus 1/kT, as shown in Fig. 3(b) (left hand y-axis). Here, k is Boltzmann's constant and T temperature. G_I was calculated from the measured capacitance and conductance at $V_g = 3\ V$ as per Ref. 43. The extracted E_A of 0.296 eV is in close agreement with half of the band gap energy ($E_G/2 \sim 0.245$ eV, measured by photoluminescence spectroscopy) indicating genuine surface inversion with minority carriers supplied via generation-recombination (G-R) in the bulk.[39] The magnitude of the discrepancy between the extracted E_A and $E_G/2$ is within the margin of error reported for both InGaAs[43] and Si.[39] Furthermore, it should be noted that the assignment of $E_G/2$ for the activation energy of the G-R dominated regime is derived from the dependency of G_I on intrinsic carrier concentration, n_i, which, when Boltzmann statistics are assumed, yields the expression in Eqn. 1.[39]

$$n_i = \sqrt{N_c N_v} exp(\frac{E_G}{2kT}) \tag{1}$$

Taking the derivative of the natural logarithm of Eqn. 1 with respect to (1/kT) yields $E_A = E_G/2$:

$$E_A = \frac{d}{d(1/kT)} ln(n_i) = \frac{E_G}{2} \tag{2}$$

Of course, the use of Boltzmann statistics is not valid for narrow band gap materials, and a deviation from this approximation is to be expected. The right-hand y-axis of Fig. 3(b) plots calculated values of $\frac{d}{d(1/kT)} ln(n_i)$ for GaSb and InSb, normalised to their respective bandgap energies, using empirically determined relationships of $n_i(T)$.[41,42] As shown, for both GaSb and InSb, this yields an activation energy which is higher than $E_G/2$. The experimentally extracted E_A for $In_{0.3}Ga_{0.7}Sb$ lies in the range between the calculated values of its binary endpoints, illustrating a genuine dependance of G_I on n_i and therefore a genuine minority carrier response.

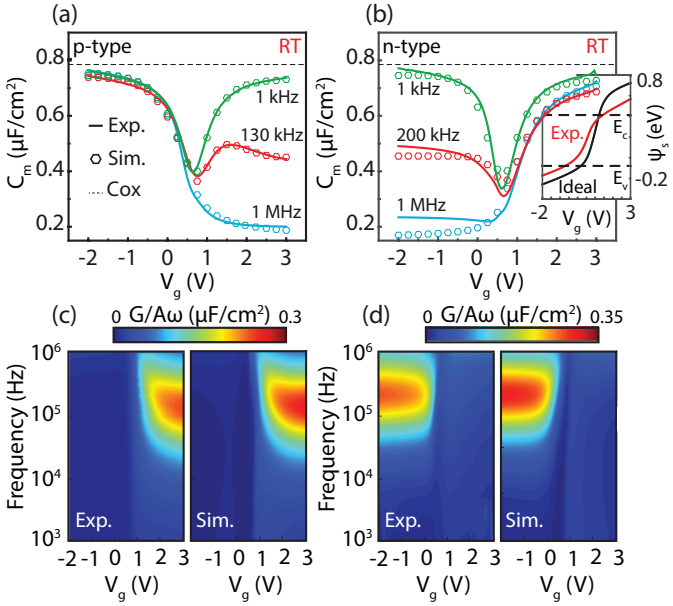

FIG. 4. Comparison between experimental and simulated multifrequency, RT, CV (a,b) and GV (c,d) responses for p-type and n-type Au/Pt/Al_2O_3/$In_{0.3}Ga_{0.7}Sb$ MOSCAPs processed with a H_2 plasma cleaning times of 1 minute.

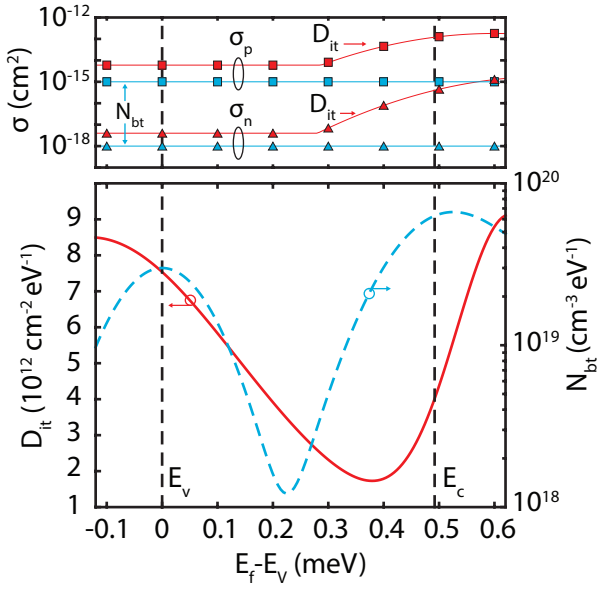

FIG. 5. Input parameters in terms of interface state density, D_{it}, border trap density, N_{bt}, and capture cross section, σ, used for the full interface state model to achieve the simulation results shown in Fig. 4. N_{bt} was input as uniform throughout the oxide thickness.

The preceding analysis unequivocally demonstrates a genuine minority carrier response for both p and n-type MOSCAPs and therefore explicitly evidences that the Fermi level at the $In_{0.3}Ga_{0.7}Sb$-Al_2O_3 interface is unpinned. In order to further quantify this interface, the experimental CV and GV data of both p and n-type MOSCAPs were modelled using the full interface state model,[44–46] including the distributed border trap model of Yuan et al.[45] for both majority and minority carriers. This method circumvents the well documented issues associated with extracting D_{it} on narrow band gap semiconductors.[47,48] Excellent fits to the experimental CV and GV data for both p and n-type samples were achieved, shown in Fig. 4, with D_{it} and N_{bt} distributions common to both (shown in Fig. 5, in addition to the capture cross sections, σ, used to achieve the best fit). For these results, doping concentrations of $N_A = 2.5 \times 10^{17}$ cm^{-3} and $N_D = 1.4 \times 10^{17}$ cm^{-3} were used. Low D_{it} across the band gap was extracted, with a minimum value of 1.73×10^{12} eV^{-1}cm^{-2} located 110 meV below the conduction band edge. The border trap distribution was fitted with two gaussians centred close to the band edges. Border trap densities were extracted with peak magnitudes of 3×10^{19} cm^{-3} near the valence band edge, and 6.5×10^{19} cm^{-3} near the conduction band edge. The Vg-ψ_s relationship is plotted as inset to Fig. 4(b) and shows an unpinned Fermi level that can move into both valence and conduction bands. The similarity between the simulated and experimental CV and GV results with common D_{it} and N_{bt} input parameters is testament to the validity of the extracted parameters.

In summary, it has been shown that by incorporating an in-situ H_2 plasma cleaning process, p and n-type $Pt/Au/Al_2O_3/In_{0.3}Ga_{0.7}Sb$ capacitors can be fabricated where the Fermi level at the $In_{0.3}Ga_{0.7}Sb$-Al_2O_3 interface is unpinned, and a genuine minority carrier response is explicitly discernible for both doping polarities. Consequently, this gate stack process could facilitate the realisation of a common channel InGaSb CMOS device, where both device polarities are fabricated with a common gate stack process. Quantitative parameters of the interface were extracted via the simulation of an equivalent circuit model, which found a minimum D_{it} of 1.73×10^{12} eV^{-1} cm^{-2} located at ~110 meV below the conduction band edge.

See the supplementary material for a comparison between CV measurements of samples processed with H_2 plasma cleaning times of 0 and 30 minutes, with and without an FGA.

This work was funded by the European Union H2020 program INSIGHT (Grant Agreement No. 688784). The authors acknowledge technical support from the James Watt Nanofabrication Center, University of Glasgow.

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