Thick Film Hydrogen Silsesquioxane Planarization for Passive Component Technology Associated with Electronic-Photonic Integrated Circuits

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Migrating Electronic-Photonic Integrated Circuits (EPICs) to higher data rates requires efficient electrical interfaces. This can be achieved with microwave technologies such as coplanar and microstrip transmission lines, but these can be difficult to apply in EPICs because of the complexity of the fabrication processes associated with monolithic integration. In this work, we report a novel method for planarizing a thick, low-κ film based on multiple-spins of layers of Hydrogen Silsesquioxane without a need for thermal curing. Films of total thicknesses of 5 μm and 6 μm were planarized on a heavily doped InP substrate and used to realize coplanar waveguide transmission lines. The film shape is defined as an integral part of the fabrication process without any need for etching. A coplanar waveguide with a characteristic impedance of between 48 Ω and 56 Ω over the frequency range 10 MHz to 67 GHz was demonstrated.

Keywords: electronic-photonic integrated circuits, monolithic integration, low-κ material, low-κ planarization, Hydrogen Silsesquioxane, coplanar waveguide

I. INTRODUCTION

The demand for increased bandwidth in both short and long-haul communications systems is increasing dramatically. Effective solutions are urgently needed, particularly for Passive Optical Networks (PONs) used in local area networks, where cost is a major consideration. The new approach of Electronic-Photonic Integrated Circuits (EPICs), where the electronic and photonic components in EPICs are integrated monolithically, can address this. On-chip monolithic integration can include the light source, optical waveguides, phase shifters, polarization converters, optical amplifiers, contact electrodes, and microwave elements.[1] Integrating the optical components has the advantage of reducing signal losses and increasing the bandwidth capacity, which also makes this technology a promising candidate for microwave signal processing and transmission.[2,3]

Depending on the application, monolithic integration in III-V semiconductors can be achieved with one, or a combination of, selective area growth, etch and regrowth, and quantum well intermixing.[4] Other technologies can be applied to silicon or lithium niobate materials.[1,5,6] For applications where the light source is included in the integration platform, an advanced engineered material is required. An example of such an application is the Electroabsorption Modulated Laser (EML), in which a Distributed Feedback (DFB) laser is monolithically integrated with an Electroabsorption Modulator (EAM).[7,8]

The performance of advanced EPICs is increasingly limited by the efficiency of the Electrical-Optical (E-O) interface, which typically makes use of microwave Transmission Lines (TLs) such as Coplanar Waveguides (CPWs) or microstrips. An additional consideration is the need to minimize the parasitic capacitance of passive components such as tracks and bond pads which means low permittivity insulators are highly desirable.[9]

In order to implement TL technology, surface planarized layers of low-κ material are required. Conventional materials and methods such as BCB (Benzocyclobutene) or polyimide based planarization are difficult to apply in EPICs.[10] BCB is stable up to only 350 °C and is consequently incompatible with many existing backend processes. Other commonly used polymers are stable to 400 °C but are vulnerable to changes in permittivity associated with water absorption. Our processing is based on Electron-Beam Lithography (EBL), while polymer materials make use of photolithography; combining both approaches would make the fabrication complicated, time consuming and introduce alignment issues. Furthermore, it is necessary to open windows for cleaving when using polymer approaches.

As an alternative, Hydrogen Silsesquioxane (HSQ) planarization is commonly used in standard integrated circuits for multilevel metal interconnects.[11] HSQ is a spin-on dielectric material designed for low-κ applications, and is also a negative electron-beam resist, which means it can be patterned directly at high resolution using EBL.[12] Its excellent properties of self-planarization, gap filling and chemical similarity to SiO_2 have identified it as a promising material for forming planarized dielectric films.[11,12] Good HSQ planarity can be achieved with a single spin coating, providing film thicknesses up to 800 nm, depending on the spin speed. Thicker planarized films can be realized with a multiple spin process, however thermal curing is required to prevent the previously deposited HSQ from dissolving.[13,14] Although HSQ planarization has been used as an on-surface coating film, it presents some integration issues such as oxidation, thermal dissociation of Si-H bonds, -OH bond formation, plasma damage, water absorption, copper diffusion into the HSQ films, and metal oxidation during thermal curing.[15,16]

In this work, we report a novel HSQ planarization method based on multiple spin coating and electron beam exposure without the need for thermal curing. A dielectric film with thickness up to 10 μm can be achieved with a simple

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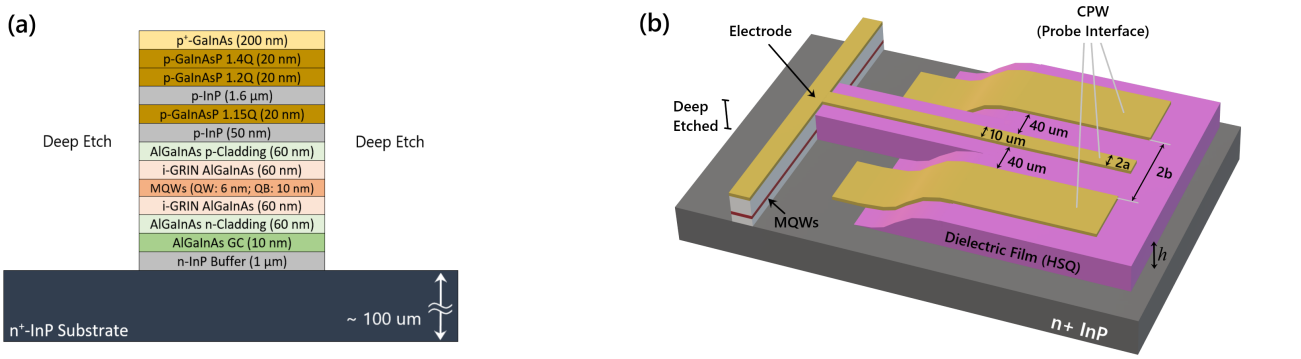

FIG. 1. (a) Cross-section of the sample after deep etch identifying the epitaxial layers in the structure, and (b) the EAM design with a TL configuration.

fabrication process. It has the advantage that the film shape is defined as an integral part of the process without any need for etch-back. The method has been applied to reduce the parasitic capacitance of passive components and to demonstrate TL technology for EPICs.

II. THEORY AND DESIGN

The aim of this work is to establish a platform for making high-speed electrical connections to a ridge waveguide EAM. The material used for the EAM is an AlGaInAs/InP p-i-n structure with a heavily doped n-type InP substrate. The EAM ridge waveguide is deep etched down to the InP substrate, as shown in Fig. 1(a), which also shows the layer structure of the EAM. Figure 1(b) shows the TL configuration used to form the electrical interface with the EAM. This design requires a low-κ film with a suitable thickness to fabricate a TL with a characteristic impedance (Z_0) of 50 Ω.

A self-planarized HSQ film was used as the low-κ dielectric. The required HSQ thickness was first studied analytically for a grounded CPW model with the circuit elements calculated using;[17–19]

$$Z_L = \frac{60\pi}{\sqrt{\varepsilon_{r,eff}}} \times \frac{1}{\frac{K(k)}{K(k')} + \frac{K(k_1)}{K(k_1')}} \tag{1}$$

$$\varepsilon_{r,eff} = \frac{1 + \varepsilon_r \frac{K(k')K(k_1)}{K(k)K(k_1')}}{1 + \frac{K(k')K(k_1)}{K(k)K(k_1')}} \tag{2}$$

where $k = a/b$, $k' = \sqrt{1-k^2}$, $k_1 = \tanh(\frac{\pi a}{2h})/\tanh(\frac{\pi b}{2h})$, $k_1' = \sqrt{1-k_1^2}$, a is half of the signal conductor line width, b is the sum of a plus the gap spacing between the signal conductor line and the ground plane, h is the dielectric thickness, and $K(k)$ is the complete elliptical integral of the first order with modulus k. Furthermore, a simulation based on Finite Element Analysis (FEA) was used to confirm the solution using HFSS simulation software.[20] In general, thicker HSQ films result in a lower parasitic capacitance for lumped elements, however a wider CPW signal stripline will be needed to maintain the required impedance of 50 Ω. The effect of fabrication tolerances was also considered: for an impedance mismatched TL, a wider strip increases the parasitic capacitance. The design was therefore optimized such that the narrowest possible CPW signal line strip could be used, which in turn requires a relatively thin HSQ layer. This minimizes the amount of HSQ required in fabrication, minimizes the number of fabrication steps, reduces the signal losses and offers the lowest possible parasitic capacitance. For this purpose, a CPW with a 10-μm-wide signal conductor line and signal-to-ground gap of 40 μm was used, as illustrated in Fig. 1(b). The results of the analytical calculation and HFSS simulation are closely matched, as shown in Fig. 2. For a CPW design with 50 Ω characteristic impedance, the results indicate a planarized thickness of 4.5 μm of HSQ is required if the dielectric constant of the planarized film is close to 4.

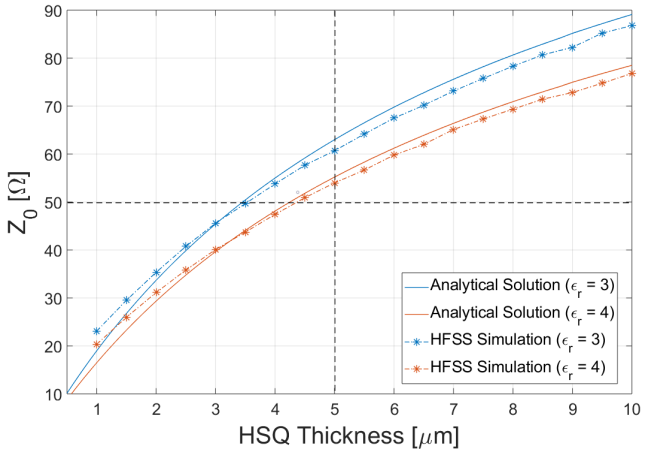

FIG. 2. Impedance as a function of the HSQ film thickness, calculated analytically (solid lines) and using the HFSS FEA simulation (dotted lines/stars).

III. FABRICATION

The HSQ film was created using a multiple spin process. After each spin, the sample underwent Post Application Baking (PAB) followed by exposure to the electron beam then development to leave only the required film shape on the surface. During the PAB stage, the sample was placed on a hotplate at 91 °C for 15 minutes. This simple curing is intended only to remove the HSQ solvent; unlike higher temperature annealing, this process does not cause a fundamental change in the HSQ properties. Before next spin, a 40-nm-thick film of SiO_2 was deposited using Plasma-Enhanced Chemical Vapor Deposition (PECVD). The deposition process along with the electron beam exposure sufficiently protected the previously spun HSQ from dissolving without the need for any additional thermal curing. The process therefore has the advantages that the shape of the planarized film is defined lithographically and thermal curing is not required. Furthermore, a previous study has shown that electron beam exposed HSQ-films contain a higher concentration of Si-H bonds than conventional thermally treated HSQ-films, which in turn results in better dielectric characteristics.[21]

Thicknesses of 5 μm and 6 μm were realized with 4 and 5 spin coatings of HSQ respectively; to implement the TL reported in this paper, the sample with the 5 μm thickness was used. Patterned HSQ features were fabricated at several separations from the ridge guide (30 μm, 40 μm and 50 μm) with no impact on any pre-defined semiconductor elements, such as the EAM. Figure 3 shows a plan view of a planarized HSQ film 30 μm away from a deep-etched EAM ridge, while Fig. 4 shows the corresponding cross-sectional SEM image indicating the HSQ thickness.

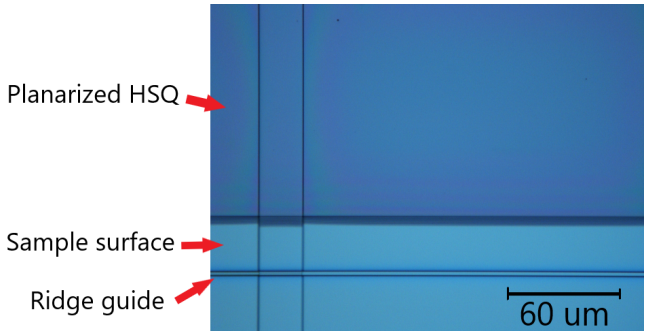

FIG. 3. Surface image of the HSQ structure planarized at 30 μm away from the ridge with 5 μm thickness.

The film-to-ridge separation gap is required to allow windows to be opened to connect the ground of the CPW to the underlying substrate (Fig. 1(b)). The gradual reduction in the HSQ film thickness towards the ridge, shown in Fig. 4, is needed to avoid sharp edges for the CPW metallization. This reduction was controlled by studying the coating uniformity at different spin speeds. The CPW was implemented by depositing 30 nm of Ti followed by 33 nm of Pt and 240 nm of Au. The final fabricated element is shown in Fig. 5.

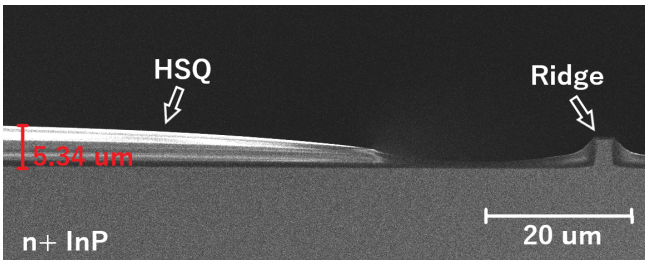

FIG. 4. A cross-section SEM image for the planarized HSQ identifying the achieved thickness.

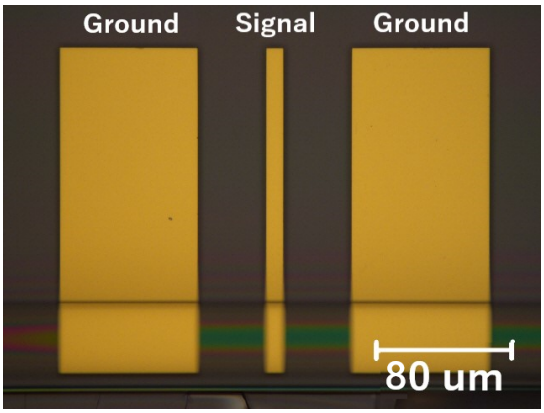

FIG. 5. Fabrication results of the implemented CPW.

IV. MEASUREMENT AND DISCUSSION

The device was tested using a Keysight E8361A Vector Network Analyzer (VNA) with a Cascade SUMMIT200 on-wafer semi-automated probe station. A pair of microprobes manufactured by GGB Industries with a pitch separation of 100 μm was used, and the system was calibrated using the Short-Open-Load-Through (SOLT) method between 10 MHz and 67 GHz. For the fabricated CPW with 10 μm signal stripline width and 40 μm signal-to-ground gap, two port scattering parameters were measured. The S-parameter measurements are shown in Fig. 6. At the input port, the port reflection coefficient was recorded to be lower than -20 dB for frequencies up to 67 GHz, while the insertion loss was close to 0 dB. This indicates that it is possible to maximize the power transfer to the EAM with low loss. The insertion loss per unit length, shown in Fig. 7, was inferred from measurements on a 100-μm-long length of TL.

The corresponding characteristic impedance of the CPW at the input port is shown in Fig. 8 as a function of frequency. An impedance of 48 to 56 Ω is achieved over the entire range of measured frequencies. The simulations in Fig. 2 indicate that an HSQ thickness of 4.5 μm is required to achieve an impedance of 50 Ω, the sample used 5 μm. This apparent discrepancy is due partly to the multiple layer structure of the film which contains PECVD SiO2 separation layers and to the tapered reduction in the HSQ film thickness from 5 μm which is required to connect the TL to the ground.

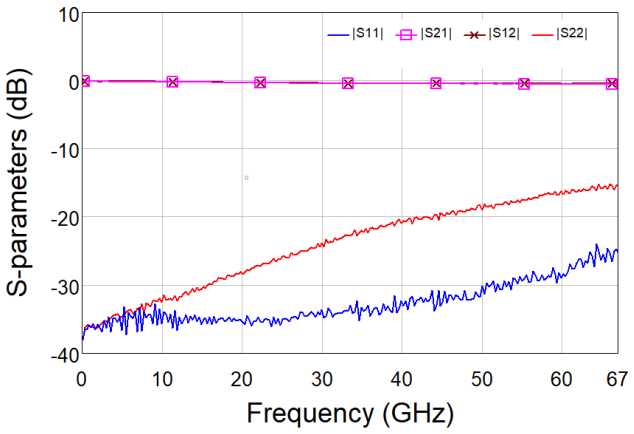

FIG. 6. S-parameter measurements for a 100 μm length of CPW TL.

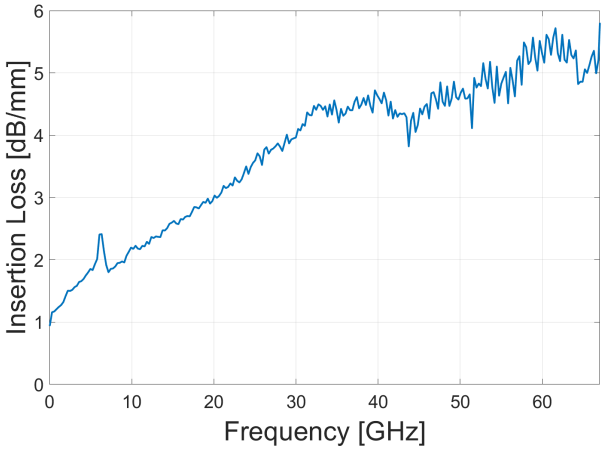

FIG. 7. The insertion loss per unit length for the CPW TL.

V. CONCLUSION

The new approach for HSQ planarization is promising for fabricating low-κ structures for use in applications where a low permittivity, thick insulator and/or low capacitance film is required. It has the advantage of simple fabrication steps with no need for thermal curing nor etch-back processing. The method can be used in EPIC applications where high accuracy and control of the film shape is required. A 5-μm-thick HSQ film was planarized and used as dielectric layer to implement a CPW TL. The RF performance of the final fabricated CPW agreed closely with analytic and FEA models of the initial design.

Compared with conventional BCB or polyimide-based planarization, both of which require many steps and high curing temperatures, this process using spin-coated HSQ self-planarizing layers is straightforward and quick to apply. Furthermore, the shapes of the planarized structures are defined as an integral part of the fabrication process.

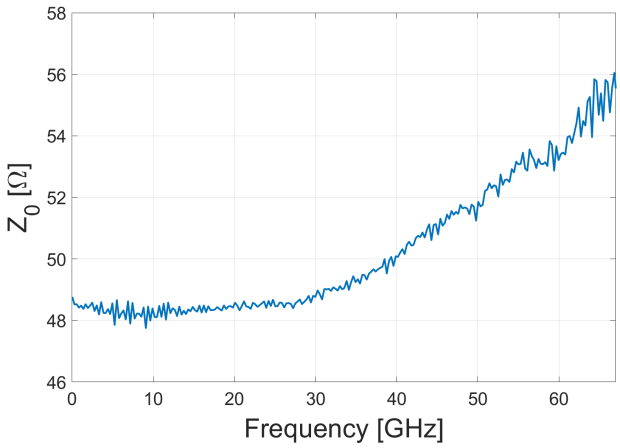

FIG. 8. The characteristic impedance of the CPW at the input port.

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