Integration of Highly Crystalline C8-BTBT Thin-Films into Simple Logic Gates and Circuits

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SUPPORTING INFORMATION

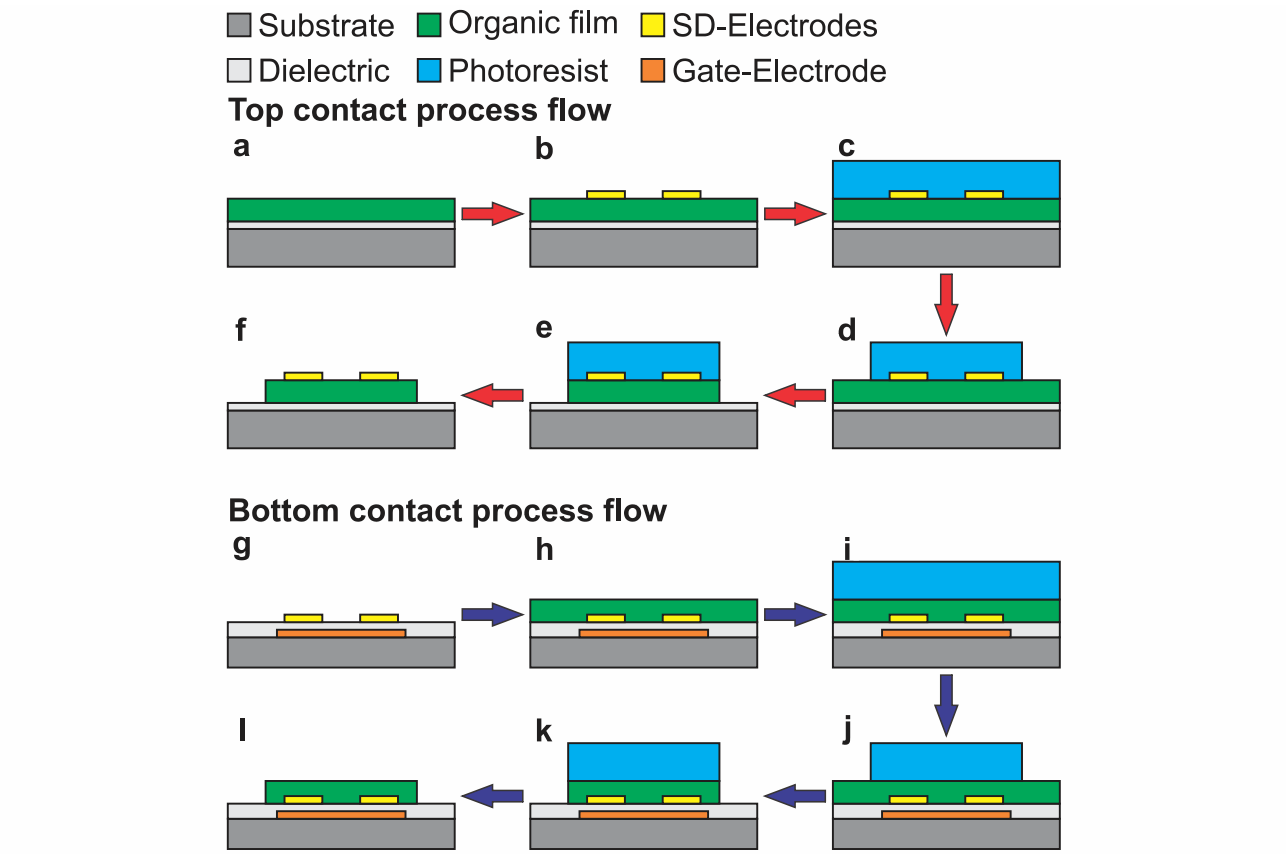

Figure S1. Schematic representation of the patterning process.
Common-bottom-gate/top-contact process flow: Deposition of a) organic semiconductor b) source-drain electrodes. c) Spin-coating and d) exposure and development of the photoresist. e) Etching of the organic thin film and f) stripping of the photoresist.
Patterned-bottom-gate/bottom-contact process flow: g) Patterning of bottom-gate, deposition of dielectric and patterning of bottom source-drain electrodes. h) Deposition of organic semiconductor. i) Spin-coating and j) exposure and development of the photoresist. k) Etching of the organic thin film and l) stripping of the photoresist.

Table S1. Full process flow for patterned, bottom-gate/bottom-contact integration.

1. Cleaning of substrate	
1.1 Soap+DIW	5 min @ 60-70°C with ultrasonication
1.2 DIW	5 min @ 60-70°C with ultrasonication
1.3 Acetone 1	5 min @ 60-70°C with ultrasonication
1.4 Acetone 2	5 min @ 60-70°C with ultrasonication
1.5 IPA 1	5 min @ 60-70°C with ultrasonication
1.6 IPA 2	5 min @ 60-70°C with ultrasonication

2. Gate patterning (Lift-off)	
2.1 Prebake	2 min @ 120°C
2.2 Spincoat photoresist layer 1	LOR-1A @ 2000 rpm, 30 sec
2.3 Bake	5 min @ 150°C
2.4 Spincoat photoresist layer 2	IX845 @ 4000 rpm, 30 sec
2.5 Bake	1 min @ 120°C
2.6 Illumination	MA6 exposure system, 7.2 sec
2.7 Development	OPD5262, 1 min
2.8 Clean	Water bath, drying with compressed N_2
2.9 Sputtering gate stack	2 nm Ti/100 nm Au in a Nimbus 310 PVD system
2.10 Stripping photoresist 2	Acetone with ultrasonication, 3 min
2.11 Stripping photoresist 1	Mircostrip with ultrasonication, 1 hour
2.12 Clean 1	Water bath, drying with compressed N_2
2.13 Clean 2	O_2 plasma for 1 min

3. Gate dielectric deposition	
3.1 Dielectric deposition	Deposit 100 nm Al_2O_3 @ 150 nm in ALD Savannah tool
3.2 Clean 1	Acetone, 5 min @ 50-60°C with ultrasonication
3.3 Clean 2	IPA, 5 min @ 50-60°C with ultrasonication

4. Via patterning and etching	
4.1 Prebake	2 min @ 120°C
4.2 Spincoat photoresist layer	IX845 @ 4000 rpm, 30 sec
4.3 Bake	1min @ 120°C
4.4 Illumination	MA6 exposure system, 7.2 sec
4.5 Development	OPD5262, 1 min
4.6 Clean	Water bath, drying with compressed N_2
4.7 Via etching	30 ml BHF + 500 ml DIW, 3 min 45 sec
4.8 Clean	Water bath, drying with compressed N_2
4.9 Stripping photoresist	Acetone with ultrasonication, 3 min
4.10 Clean 1	Water bath, drying with compressed N_2
4.11 Clean 2	Acetone, 5 min @ 50-60°C with ultrasonication
4.12 Clean 3	IPA, 5 min @ 50-60°C with ultrasonication

5. Source-Drain patterning (Lift-off)	
5.1 Prebake	2 min @ 120°C
5.2 Spincoat photoresist layer 1	LOR-1A @ 2000 rpm, 30 sec
5.3 Bake	5 min @ 150°C
5.4 Spincoat photoresist layer 2	IX845 @ 4000 rpm, 30 sec
5.5 Bake	1 min @ 120°C
5.6 Illumination	MA6 exposure system, 7.2 sec
5.7 Development	OPD5262, 1 min
5.8 Clean	Water bath, drying with compressed N_2
5.9 Deposit MoOx	5 nm by evaporation in Kurt J. Lesker tool
5.10 Deposit Au	30 nm by sputtering in a Kurt J. Lesker LAB 18 PVD system
5.11 Stripping photoresist 2	Acetone with ultrasonication, 3 min
5.12 Stripping photoresist 1	Remover PG (Microchem) @ 70°C with ultrasonication, 10 min
5.13 Clean 1	IPA, 5 min @ 70°C with ultrasonication
5.14 Clean 2	Acetone, 10 min @ 60-70°C with ultrasonication
5.15 Clean 3	IPA, 10 min @ 60-70°C with ultrasonication

6. Surface treatment	
6.1 O2-Plasma clean	5 min @ 100 W
6.2 UV-ozone treatment	15 min
6.3 PFBT treatment	30 ml ethanol + 40 µl PFBT, 30 min @ room temperature
6.4 Clean	Rinse with IPA for 15 sec, drying with compressed N_2
6.5 Phosphonic acid treatment	40 mg phosphonic acid + 25 ml ethanol, 18 hours @ 70°C
6.6 Clean	Rinse with ethanol for 15 sec, drying with compressed N_2
6.7 Bake	10 min @ 70°C

7. Organic layer deposition and patterning	
7.1 Zone-casting	Solution of 0.3 %wt C_8-BTBT in heptane. Casting at 20 µm/s at room temperature. Thickness ~20 nm.
7.2 Vacuum evaporation	50 nm evaporation of C_8-BTBT at rate of 0.2 Å/s and substrate temperature of 22°C in homebuilt UHV system.
7.3 Photoresist processing	Non-fluorinated, chemically amplified, i-line photoresist
7.4 Organic dry etching	Oxygen plasma reactive ion etching

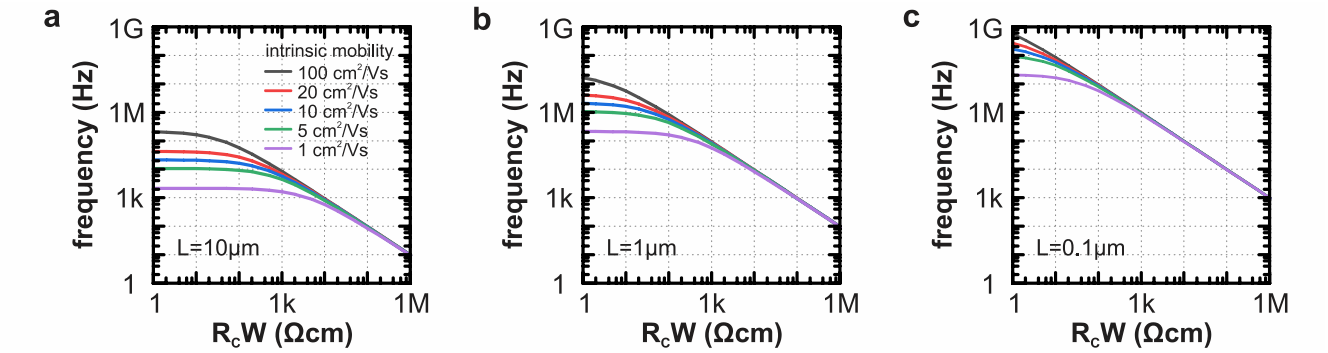

Figure S2. Ring oscillator frequency simulation.

Simulated dependency of the 19-stage ring oscillator frequency on intrinsic charge carrier mobility and contact resistance R_CW for different channel lengths. For very small contact resistances, the frequency follows the theory $f \sim 1/L^2$, while for larger contact resistance, the frequency is only increasing as $f \sim 1/L$. At small contact resistances the total transistor resistance is limited by the channel resistance, therefore the operation speed scales quadradic with the channel length. For large contact resistances, the total transistor resistance is severely limited by the contact resistances, hence variations of the channel resistance have no influence on the operation speed. However, since all dimensions are scaled linearly in this simulation, the parasitic capacitances decrease as much as the channel lengths decrease. Therefore, the operation speed increases due to this decrease of the parasitic capacitances.