A Planar Distributed Channel AlGaN/GaN HEMT Technology

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***Abstract*— This paper presents AlGaN/GaN HEMT devices with improved thermal and DC current-voltage (IV) performance using a novel method of obtaining a distributed channel device, i.e. the total semiconductor area between the Ohmic contacts comprise conducting and non-conducting regions. A novel oxygen (O_2) plasma treatment technique is used to realise the inactive or non-conducting regions. Multi-finger devices with 1 mm gate periphery exhibit extremely low gate leakage currents below 0.2 μA/mm at a gate voltage of -20 V and an increase in the saturated output current by 14 % at 20 V drain voltage. Moreover, performed DC-IV measurements at various ambient temperatures show that the proposed method not only increases the saturated output currents by over 10% for 1×100 μm gate devices but also significantly reduces their knee walk-out voltage from 6 V to 3 V at 300K. These results show that this device design approach can exploit further the potential of the GaN material system for transistor applications.**

***Index Terms*— AlGaN/GaN high electron mobility transistor, gate leakage current, knee-walkout, planar isolation, self-heating.**

I. Introduction

Today's state-of-art technology for efficient high power radio frequency (RF) applications is based on gallium nitride (GaN) high electron mobility transistors (HEMTs) due to the superior properties of GaN: high electron mobility, high dielectric strength, high current density, and ability to work at high temperatures. However, the current GaN HEMT technology is thermally limited by device self-heating constraining the achievable saturated drain current densities, output powers and degrading device reliability. For instance, for an increase in the channel temperature from room temperature to 187 °C, the transconductance (g_m), cut-off frequencies (f_T/f_{max}) and the saturation current (I_{max}) fall by around 35% due to the reduced saturated electron velocity and mobility in the channel at the higher temperature [1]. For improved thermal management of AlGaN/GaN HEMTs, high thermal conductivity silicon carbide (SiC) substrates are widely used in devices for high power density RF applications [2], while diamond substrates, with the highest thermal conductivity of 2000 W/mK, have been actively researched over a number of years now [3],[4]. Additional methods include packaging [5],[6], liquid cooling [7]–[11], high thermal conductivity material incorporation in the device [12] etc. To date, however, thermal management through heat removal through substrate alone has proven to be inadequate for GaN technology, and so to advance the technology we need to think about ways to generate less heat in the first place.

Since the main heat spot in lateral AlGaN/GaN HEMTs is at the gate edge on the drain side [13], it would therefore be most desirable to have the 'cooling system' as close as possible to this region. In this regard, devices employing distributed gates (DG) have been proposed [14]–[16]. They use gate layouts with active and inactive regions along the width of the channel to achieve reduced channel temperatures. This approach was first used by Darwish *et al.* by forming inactive regions along the gate through etching away the active layers [14]. Asubar *et al.*, on the other hand, used narrow (330 nm) etched trenches along the channel to reduce the thermal resistance and improve the DC characteristics [15]. Another technique of fabricating distributed gate devices was proposed by Lin *et al.* where the GaN layers were grown on Si substrate patterned with stripes of SiO_2 to achieve inactive and active regions along the device [16]. Using these approaches, good improvement in the thermal performance of the devices was demonstrated [14]-[16], but due to the dry etching etc. techniques required to realize the inactive gate regions, the gate leakage current was increased from 2.1 μA/mm to 8.2 μA/mm at -10 V gate voltage for conventional and distributed gate designs, respectively [16]. Thus, the overall electrical device performance was degraded offsetting the benefits in the thermal performance.

In this paper, we report new approach to realize AlGaN/GaN HEMTs with distributed regions in which both the thermal and electrical device performances are improved. Specifically, a new planar isolation technique based on O_2 plasma is used to realize the inactive or non-conducting gate regions. Preliminary results using this approach were presented recently by the authors [17] and this paper provides more details and results.

The paper is organized as follows: section II describes the distributed gate and channel design concept including basic simulations. A description of the O_2 planar isolation technique is also provided here. Section III describes the device details and the fabrication processes. Measurement results are given in section IV including a discussion of these, and conclusions to the work are given in section V.

II. Distributed channel design

A. Distributed gate and channel concept

In the proposed distributed channel AlGaN/GaN HEMT technology, the device comprises alternate conducting and non-conducting regions. The non-conducting regions are realized through an oxygen (O_2) plasma treatment technique which is understood to oxidize the nitride layers [18]–[20], and in the work this was done to completely deplete the two-dimensional electron gas (2DEG) channel as illustrated in Fig. 1. As described in earlier work, the distributed gates (DG) or distributed channel improves heat dissipation in the device because current flow through the device is only via the active device areas where heat is generated (indicated as "hot" region) and the inactive device ("colder") regions where the heat can be dissipated leading to an overall reduced channel heating compared to a conventional device. For multi-finger devices, the concept can be further extended so that the active regions corresponding to one finger are aligned with inactive regions of the neighboring fingers.

This work was supported in part by the Engineering and Physical Sciences Research Council (EPSRC) grant EP/K014471/1, and by an EPSRC studentship to Maira Elksne.

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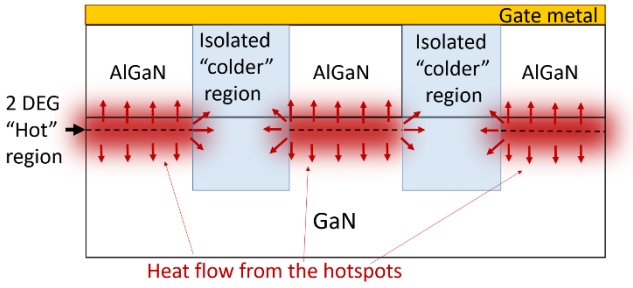


Fig. 1. Schematic illustration of active (hot) and inactive (cold) regions in a distributed gate (DG) and channel device.

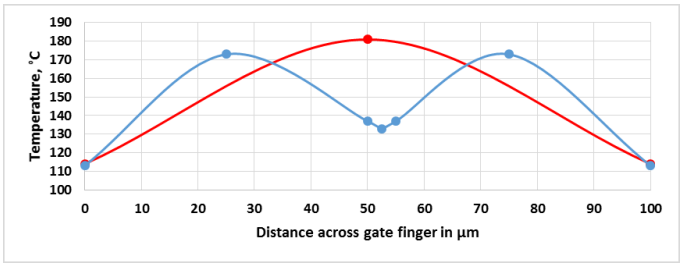
B. *Simulated channel temperatures of distributed gate devices*

For further insight, the channel temperature of device with a DG gate architecture dissipating 2 W was simulated using finite element analysis software COMSOL Multiphysics [21]. The device structure consisted of a 350 µm SiC substrate, a 200 nm AlN nucleation layer, 2 µm GaN channel layer and 20 nm AlGaN barrier layer. The assigned thermal conductivities were 150 W/mK and 30 W/mK for GaN and AlN layers, respectively. Four distributed gate structures with 1, 2, 4 and 10 active sections (or 0, 1, 3 & 9 inactive sections), denoted 1 × 100 µm, 1 × (2×50) µm, 1 × (4×25) µm, and 1 × (10×10) µm, respectively, were simulated. The heat source was located in the 2DEG channel at the GaN and AlGaN interface. The total active gate width in each case was 100 µm wide, while each inactive section was 5 µm wide. Fig. 2a shows a comparison of the temperature profile across the 1×100 µm and 1× (2×50) µm gate geometries. The gate design with one inactive region in the middle of the device width has a lower maximum channel temperature by 10 °C. Also, a low temperature zone in the middle of the active channel is introduced by the inactive region. Further sectioning of the gate finger, e.g. into four 25 µm or and ten 10 µm wide active gate sections (Fig. 2b), reduces the maximum channel temperature even further, by over 30 °C. Clearly, the relative sizing and number of active/inactive sections along the width of the gate determines the device operating temperature.

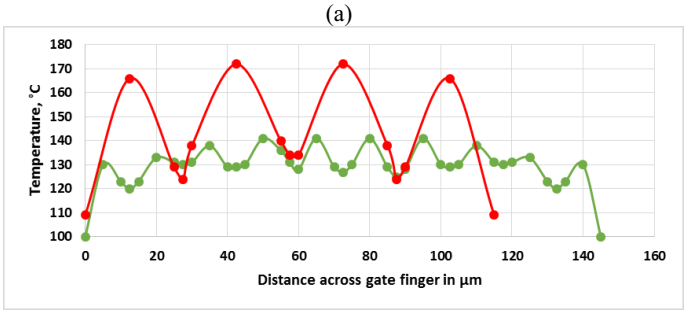
C. *Oxygen plasma isolation technique*

To implement the proposed structure, we employed an oxygen (O_2) planar isolation technique developed in the group for AlGaN/GaN HEMTs to realize the inactive or non-conducting regions [22]. Oxygen plasma ashing is used routinely in semiconductor processing to remove photoresist residues after patterning. We also use it as such in our GaN processing but noticed a drop in current levels between contact pads used to evaluate contact resistances whenever the exposure to the plasma was extended. In the literature, it is known that O_2 plasma can oxidize GaN layers [18] and this has been used to minimize gate leakage currents in AlGaN/GaN HEMTs through oxidation of the barrier layer surface underneath the gate electrode [20]. For our structure (described in sec. III), O_2 plasma treatment at 200 W for 7 minutes can completely deplete the 2DEG underneath making it non-conducting. However, low RF power ashing up to 80 W from 1 to 2 minutes was not seen to have a degrading effect of the 2DEG properties.

To test the effectiveness of the O_2 plasma isolation method scattering parameter (S-parameter) measurements were performed on two 2000 µm long coplanar waveguide (CPW) transmission lines fabricated on AlGaN/GaN samples used for device fabrication. One sample was exposed to O_2 plasma prior CPW metallization and the other was not. Forward transmission coefficient (S21) of these two transmission lines are compared to a third CPW transmission line of identical length on a low-loss alumina substrate that was used for vector network analyzer (VNA) system calibration. The measurements



(a)



(b)

Fig. 2. COMSOL simulation of the temperature profile for a 100 µm wide active finger with and without a 5 µm wide inactive section in the middle (a); and with three and nine 5 µm wide inactive sections (b). Power dissipation was 2 W.

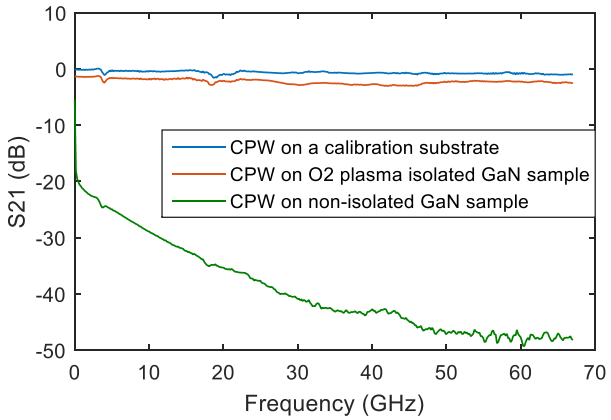


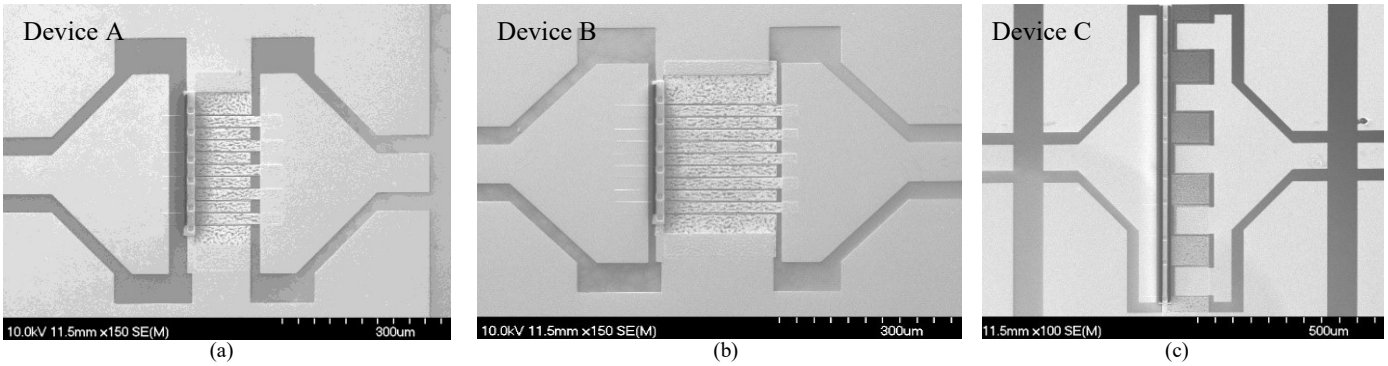
Fig. 3. S-parameter S21 measurements of three CPW transmission lines: CPW on a calibration substrate, CPW on an isolated AlGaN/GaN sample by O_2 plasma treatment and non-isolated AlGaN/GaN sample.

are shown in Fig.3. Here one can see that non-isolated CPW line exhibits high losses across the entire measurement frequency range, reaching -50dB at 67 GHz whereas the O_2 plasma isolated CPW has a loss of only -2dB (which we attribute to characteristic impedance mismatch from the different substrate material, since the three lines had the same geometry) which is comparable to the line on the calibration substrate. This result shows that O_2 plasma treatment is an effective way of achieving non-conducting regions in AlGaN/GaN material.

The O_2 isolation technique for AlGaN/GaN HEMTs is a simple, effective and low-cost process. We note that to employ this technique, the process parameters must be adjusted for each specific wafer depending of the barrier layer thickness and its Al mole fraction. Finally, devices isolated using this technique show the same output characteristics after more than year (when not being in use) showing that this is a stable process.

III. Device Fabrication

AlGaN/GaN HEMTs were fabricated on a high thermal conductivity 4H-SiC substrate grown by metal organic chemical vapor



(a) (b) (c)

Fig. 4. SEM images of fabricated devices with an active area of 10x100 um and gate pith of a) 23.5 µm (device A) b) 23.5 µm and distributed channel (device B) and c) 83.5 µm (device C).

deposition (MOCVD). The epitaxial structure used here was composed of a thin Al nucleation layer followed by 1.8 µm high resistivity GaN, 200 nm of non-intentionally doped GaN, 20 nm of AlGaN with 25% Al content and 2 nm of GaN cap layer. Using Hall measurements, it was determined that this structure had a 2DEG sheet carrier concentration of $1x10^{13}$ cm^{-2} and electron mobility of 1400 $cm^2/V{\cdot}s$. The source and drain Ohmic contacts were obtained by Ti/Al/Ni/Au (30 nm /180 nm/40 nm/100 nm) metal evaporation followed by annealing in a nitrogen atmosphere at 800 °C for 30s. Ohmic contact resistances were measured to be 0.48 Ω·mm. The Schottky gate contact was formed by evaporation of Ni/Au (20 nm/400 nm) metals. Oxygen (O_2) plasma treatment was used to isolate the devices and to achieve a striped patterned isolation for heat dissipation along the device width. The O_2 plasma treatment was performed in the BP80 RIE (reactive ion etching) tool with an RF power of 200 W at a pressure of 20 mT. The devices were passivated (30 nm) SiN_x deposited using plasma enhanced chemical vapor deposition (PECVD).

Distributed gate and standard HEMT devices with source-drain separation of 3.5 µm, gate length of 200 nm, gate pitch of 23.5 and 83.5 µm, an active device area of 10 x 100 µm were fabricated simultaneously. DG device had a stripe pattern of 5 µm wide isolated lines and 5 µm active regions along the device width. The source contacts on all devices were connected through metal bridges with 2 µm thick polyimide layer underneath them for support. Bond pads were fabricated in CPW (coplanar waveguide) technology with pitch of 100 µm. SEM (scanning electron microscope) images of fabricated 10 finger standard and DG HEMTs with gate pitch of 23.5 µm are shown in Figs. 4a & b, respectively. To have a 1 mm wide active region when isolated regions of 5 µm are introduced after each 5µm active region the total contact area of the device becomes almost 2 times larger. Standard HEMTs with gate pitch of 83.5 µm were also

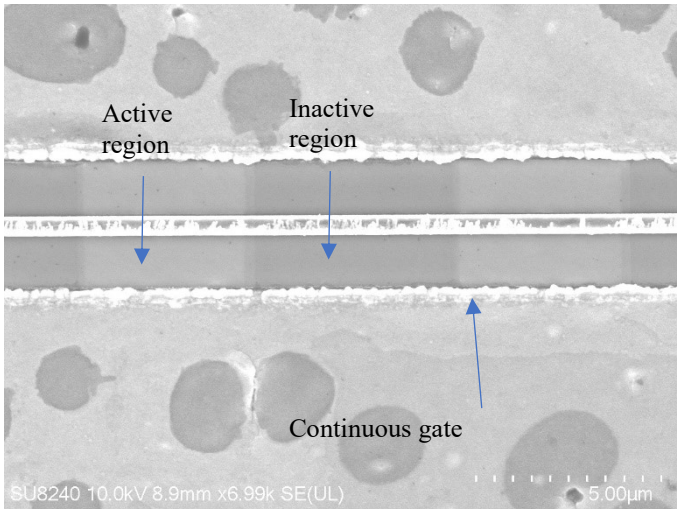


Fig. 5. SEM image of distributed gate region from device B.

fabricated so as to compare the effect of DG devices with other means of reducing self-heating such as increasing gate pitch. An SEM micrograph of this shown in Fig. 4c. Closer SEM image of the isolated DG pattern from the top side is showed in Fig. 5. Here one can see that the device is indeed planar.

IV. Results and Discussion

Standard DC current-voltage (IV) measurements at room temperature were performed on three 10 finger devices A, B and C (fig. 4). Fig 6. shows IV characteristics for DG (device B, gate pitch 23.5µm) and standard devices (A and C, with 23.5 and 83.5 µm gate pitches, respectively) with active area of 10 x 100 µm measured continuously from V_{GS} = 0 V to V_{GS} = -5 V with 1 V decrements. In the large gate periphery devices there is a tradeoff between increasing the total device area and reducing the channel temperature and consequently improving performance. It can be seen that both devices B and C perform better than device A, i.e. have higher saturated current. Here, one can also see that increasing the device width for the 10x100 µm device 2 times by introducing the inactive regions along the channel (device B) reduces the channel temperature more efficiently compared to increasing gate pitch by increasing the length of Ohmic contacts 4 times (devices C), which can be seen as increased saturated current. Note, however, the fact that the saturated output current still reduces with increasing drain bias voltage means that the self-heating is not fully suppressed. Optimization of the active and inactive regions along the gate width is still required to further reduce device self-heating.

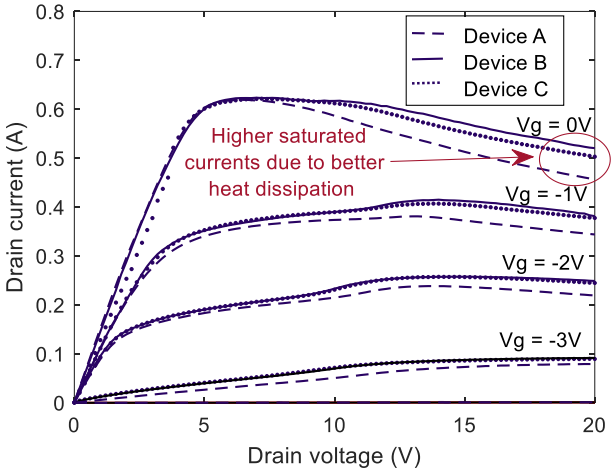


Fig. 6. Output (I_{DS} -V_{DS}) characteristics for devices A, B and C.

All fabricated devices exhibited extremely low gate leakage currents of <0.2 µA/mm at V_{DS} = 0 V and V_{GS} = -20 V as shown in Fig. 7. We attribute this to the use of oxygen plasma treatment for creation of the

non-conducting regions including device isolation. The planar geometry eliminates electrons tunneling into the channel from the gate through the mesa sidewall, for instance. Note also that there is no degradation in the leakage currents for the DG device compared to the standard devices showing the advantage of this planar device geometry over previous attempts to fabricate distributed gate HEMTs using etched isolation [16].

DC-IV measurements were also performed on standard HEMT and DG – HEMT with active area of 1x100 µm in ambient temperatures from 9 K to 300 K and the results are shown in Fig. 8. The measurements at 9 K show the full potential of the device since the heating effects are minimized. At the ambient temperature of 9 K both devices exhibit the same amount of saturated output current as expected since they both have the same active area. In Fig. 8 one can see that as the ambient temperature increases both devices exhibit knee walk-out and the saturated output current decreases due to heating effects. The reduction in the saturated current with increasing ambient temperature is by 6% less for the distributed gate (DG) device. There is also a significant difference in the knee voltages between DG and standard devices as illustrated in Fig 8. DG devices exhibit significantly smaller knee walkout reducing knee voltage 2 times. Knee walk out is generally associated with self-heating and electron trapping in the buffer layer and surface [23]. However, since the devices compared here are made on the same wafer using exactly the same processing steps, and we assume that the electron trapping levels in both devices are nominally the same. Indeed pulsed-IV characterization (not shown here) on the two devices show similar levels of current collapse. We therefore attribute the improved performance to the improved heat dissipation in the channel. We also suspect that due to the thin (30 nm) SiN passivation there is a slight virtual gate formation on the surfaces of both devices but in the DG device it is reduced since the peak of electric field at the gate edge on the drain side is distributed due to the inactive regions along the device. We note here though that the larger 10 finger devices (Fig.6) did not exhibit improved knee voltage. The reasons for this are unclear and under investigation. Last but not least, as reported in our earlier work, the device cut-off frequencies are not degraded for the proposed DG devices [17].

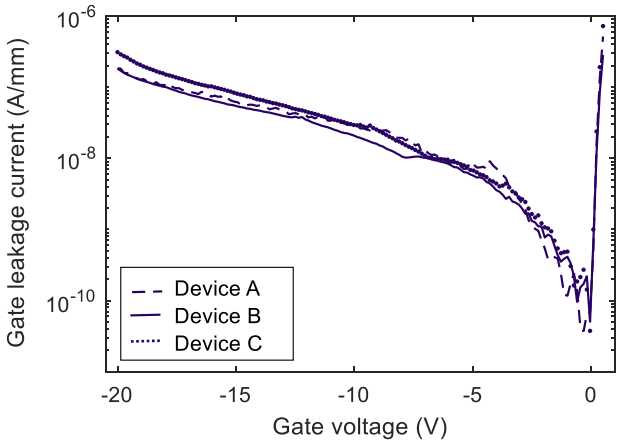


Fig. 7. Gate leakage currents for devices A, B and C at V_D = 0V.

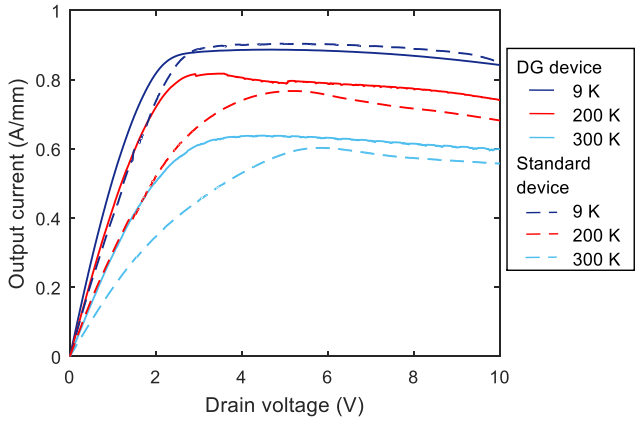


Fig. 8. Output I_{DS} -V_{DS} characteristics at V_G = 0V for devices with active area of 1x100µm at ambient temperatures of 9, 200 and 300 K.

IV. Conclusion

A novel method of planar distributed channel AlGaN/GaN HEMT device technology was described in this paper. It shows good DC-IV performance including by 14% higher saturated output currents, low gate leakage currents of under 0.2 µA/mm and knee walk-out for the single finger device reduced by a half at 300 K. This performance could be increased with optimized designs. We attribute the measured higher saturation current levels and reduced knee-walkout to the improved heat distribution within the device, while the low leakage current comes from the new planar isolation technique. This new device design and realization approach can enable future high performance GaN power amplifiers.

Acknowledgment

The authors would like to thank the staff of James Watt Nanofabrication Centre and Dr. Afesomeh Ofiare for the support and assistance in this work.

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