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# High-efficiency Ge-on-Si SPADs for short-wave infrared

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## ABSTRACT

High efficiency, Ge-on-Si single-photon avalanche diode (SPAD) detectors operating in the short-wave infrared region (1310 nm - 1550 nm) at near room temperature have the potential to be used for numerous emerging applications, including quantum communications, quantum imaging and eye-safe LIDAR applications. In this work, planar geometry Ge-on-Si SPAD designs demonstrate a significant decrease in the dark count rate compared to previous generations of Ge-on-Si detectors. 100  $\mu\text{m}$  diameter microfabricated SPADs demonstrate record low NEPs of  $2.2 \times 10^{-16} \text{ WHz}^{-1/2}$ , and single-photon detection efficiencies of 18% for 1310 nm at 78 K. The devices demonstrate single-photon detection at temperatures up to 175 K.

**Keywords:** SPAD, Single-Photon, Ge-on-Si, planar

## 1. INTRODUCTION

Single-photon avalanche diode (SPAD) detectors are semiconductor-based devices that can absorb a single-photon and create a macroscopic current pulse that can be readily measured when biased above the breakdown voltage.<sup>1</sup> In Geiger mode, an electron-hole pair from a single-photon or, for example, a thermally generated carrier can initiate the impact ionization process which can lead to a self-sustaining avalanche. This avalanche current needs to be quenched by momentarily lowering the bias to below avalanche breakdown, and then returning the bias to the above breakdown before another event can be detected.<sup>2</sup> SPADs have been used for various applications including time-of-flight ranging and LIDAR,<sup>3,4</sup> quantum key distribution,<sup>5</sup> quantum optics, quantum imaging and photonic quantum computing.<sup>6</sup> Commercial Si SPADs are available which operate near, or at, room temperature but are limited to wavelengths below 1000 nm due to the bandgap of Si. Since Ge has a narrower band-gap than Si it is able to absorb light at longer wavelengths, it can allow operation in the short-wave infrared<sup>7</sup> up to  $\sim 1600$  nm if used as an absorber in a SPAD structure.<sup>8</sup> The advantages of short-wave infrared light include the compatibility with standard communications wavelengths of 1310 and 1550 nm as well as an increase in the eye-safe power level at the longer wavelengths. The eye-safe threshold level is approximately 20 times higher for light at 1550 nm wavelength compared to 850 nm,<sup>9</sup> allowing safe operation of much higher laser powers in the SWIR region. In addition, there is a four-fold reduction in solar background which will be the dominating factor in detected background in normal daylight operation. Overall, under normal circumstances, for daylight LIDAR use in eye-safe conditions there are considerable signal-to-noise advantages in operation in the SWIR region. Finally the longer wavelength light will have lower scattering through the atmosphere and obscurants like fog, snow, rain, and haze.<sup>10,11</sup>

In the short-wave infrared region the most widely used single-photon detection technologies are currently InGaAs/InP SPADs,<sup>12</sup> and superconducting nanowire single-photon detectors (SNSPDs).<sup>13</sup> InGaAs/InP detectors have an advantage over SNSPD devices since they can operate at Peltier-cooled temperatures, while the SNSPD devices required cryogenic operating temperatures. InGaAs/InP SPADs are commercially available and provide high performance detection at communications wavelengths, but have much higher cost compared

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to silicon-based photonic technology. The lower silicon production cost could make it commercially viable to extend Si-based SPAD single-photon detection technology using Ge-on-Si to short-wave infrared<sup>14–16</sup> for use in automotive LIDAR<sup>17</sup> where higher laser power and improved signal to noise enable the potential to provide longer range especially through atmospheric obscurants. The lower costs also have significant advantages for quantum communication and quantum imaging applications.

The single-photon detection efficiency (SPDE) of a devices is the product of the following factors: the fraction of photons absorbed in the i-Ge, the fraction of carriers that drift from the absorption region to the avalanche region, and the fraction of carriers that initiate an avalanche current sufficient to provide a detectable output pulse. The dark count rate (DCR) is the rate of false positive detection events which result from non-photogenerated carriers that cause detectable current pulses. The DCR can originate from a number of factors, including thermally generated carriers in the diode structure, from the sidewalls, and band-to-band tunnelling. Again, if these carriers produce a detectable output, then they will contribute to DCR. The challenge is to design structures that reduce the likelihood of dark-generated events and allow the higher bias operation that will enhance SPDE.

Our design improves the SPDE while decreasing the DCR by increasing the fraction of photo-generated carriers reaching the avalanche region while decreasing the generation of dark current and counts. This is accomplished by moving the etched side walls away from the active region, and removing hot spots in the electric field profile close to the active region (Fig. 1). By placing the etched sidewalls further from the high field active region, we will reduce the likelihood of carriers originating at the sidewalls from causing breakdown events. The elimination of hot spots in the electric field of the active part of the devices leads to less likelihood of edge breakdown and decreased tunnelling leading to a lower DCR and potentially higher SPDE.

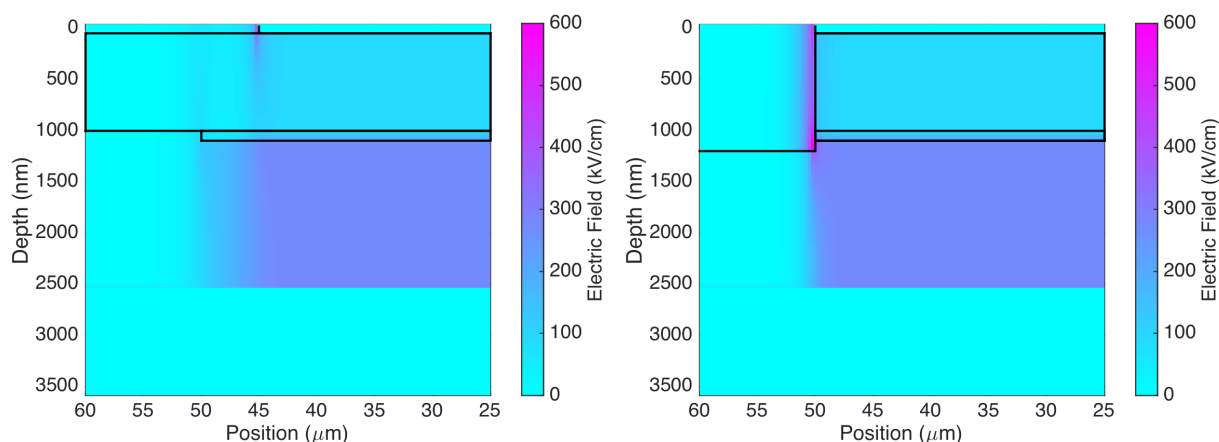


Figure 1. Electric field profile from simulations, left) our planar design, right) previous mesa design. The high field active region is away from the side walls and hotspots are reduced.

## 2. FABRICATION

In order to confirm that the planar design leads to better performance as predicted by simulations, Ge-on-Si SPAD devices were produced using silicon foundry compatible microfabrication processes. The device fabrication used 150 mm wafers n<sup>++</sup> Si (001) wafers. First a 1.5 μm i-Si avalanche region was grown epitaxially using commercial reduced pressure chemical vapour deposition (RPCVD). Next photolithography was used to define a pattern for alignment markers on the wafer. The alignment markers were dry-etched anisotropically by an inductively coupled plasma reactive ion etch (ICP-RIE) using fluorine-based chemistry (SF<sub>6</sub>/C<sub>4</sub>F<sub>8</sub>) to a depth of 1.9 μm.<sup>18</sup> The wafers were cleaned before a 10 nm layer of SiO<sub>2</sub> was deposited to prevent sputtering of the Si surface during implantation. Photolithography was used again to pattern the areas for charge sheet implantation, which will define the size of the devices. Ion implantation of boron at 20 keV was used to implant the charge sheet. Five

wafers were used with implantation doses ranging from  $1 \times 10^{12}$  atoms  $\text{cm}^{-2}$  to  $5 \times 10^{12}$  atoms  $\text{cm}^{-2}$  to allow for variation in dopant activation. Following implantation and wafer cleaning the dopants were activated at  $950^\circ\text{C}$  for 30 seconds. The wafers were cleaned using HF followed by RCA cleans before being sent for Ge epitaxial growth. The  $1 \mu\text{m}$  i-Ge absorption region and  $50 \text{ nm}$  p<sup>++</sup> Ge top contact region were then grown by bulk epitaxy in a commercial RPCVD tool.

After the final epitaxial growth, the top contact regions were defined within the charge sheet areas by photolithography and a shallow  $70 \text{ nm}$  etch using ICP-RIE dry etch<sup>18</sup> followed by an etch through the i-Ge layer with a  $10 \mu\text{m}$  spacing from the charge sheet to isolate the devices. The surfaces were passivated by growing  $\text{GeO}_2$  before an atomic layer deposition (ALD) deposition of  $\text{Al}_2\text{O}_3$ , followed by a plasma enhanced chemical vapor deposition (PECVD) deposition of  $\text{Si}_3\text{N}_4$ . As  $\text{GeO}_2$  is water soluble, the  $\text{Al}_2\text{O}_3$  and  $\text{Si}_3\text{N}_4$  layers are essential to protect the surface of the Ge absorber. Via holes were etched and Ni/Pt top contacts were deposited followed by HSQ planarization and Al bond pad deposition (Fig. 2). Next Ni/Pt was deposited on the back of the sample to form the backside contact. The devices fabricated have a  $100 \mu\text{m}$  diameter charge sheet,  $120 \mu\text{m}$  diameter spacer region, a  $90 \mu\text{m}$  diameter top contact region, with a  $60 \mu\text{m}$  diameter window within the metal contact layer. Figure 3 shows a scanning electron microscope image of a device.



Figure 2. The structure of the device is composed of an n<sup>++</sup> Si substrate, with a  $1.5 \mu\text{m}$  i-Si multiplication region with implanted charge sheet at the top. Followed by an epitaxially grown  $1 \mu\text{m}$  i-Ge absorption layer, and  $50 \text{ nm}$  p<sup>++</sup> Ge top contact layer.

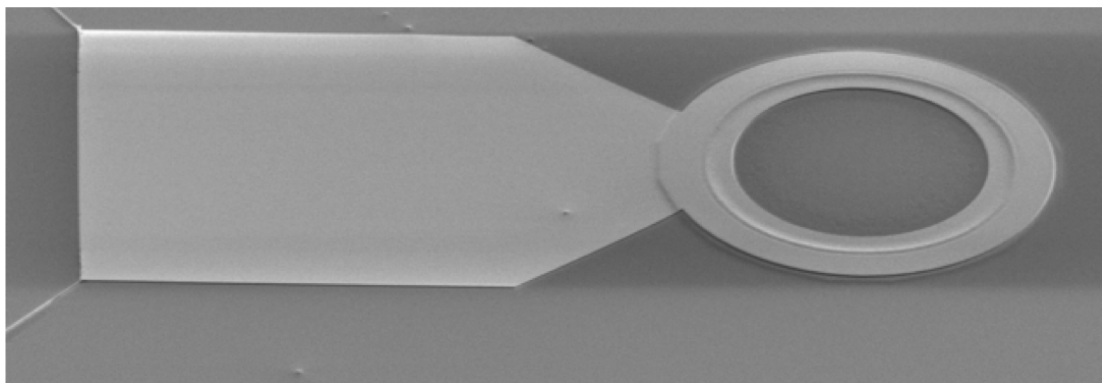


Figure 3. A scanning electron microscope image of a  $100 \mu\text{m}$  device

Initially devices were fabricated from all five wafers to determine which wafer had the optimal charge sheet doping. Initial device were fabricated without an antireflective coating. Current-voltage measurements of detectors fabricated from the five different wafers operating at  $77 \text{ K}$  were taken in the dark and then with short-wave infrared illumination at  $1310 \text{ nm}$  wavelength. The infrared light was only absorbed in the Ge absorption region.

The wafers with the lowest doped sheet charge layer demonstrated early punch-through which means that a high field across the absorption region leads to higher carrier generation from non-photon processes. The wafer doped with the middle sheet charge level demonstrated punch-through around 20 V and good breakdown close to 40 V (Fig. 4). This wafer had the lowest multiplied dark current, being the closest to the original design. This wafer was used for all the measurements reported in this paper. The devices were wire bonded to header packages compatible with measurements in a cryostat with optical access.

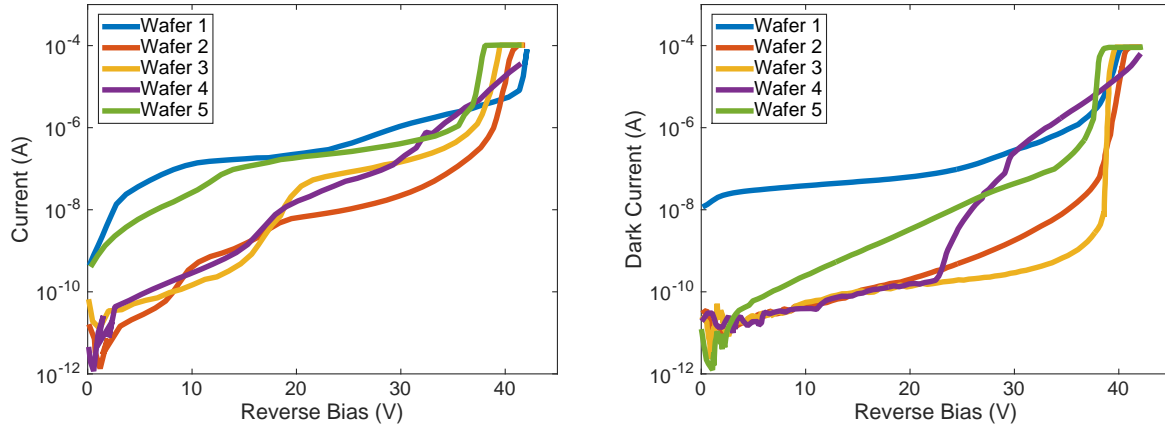


Figure 4. The current-voltage characteristics of typical 100  $\mu\text{m}$  diameter Ge-on-Si SPAD detectors made using different charge sheet doping concentration wafers:  $1 \times 10^{17} \text{ cm}^{-3}$  (blue),  $2 \times 10^{17} \text{ cm}^{-3}$  (red),  $3 \times 10^{17} \text{ cm}^{-3}$  (yellow),  $4 \times 10^{17} \text{ cm}^{-3}$  (purple), and  $5 \times 10^{17} \text{ cm}^{-3}$  (green). All the detectors were operated at 77 K and illuminated with 1310 nm wavelength light (left) or in the dark (right).

### 3. CHARACTERIZATION

Analysis of devices was undertaken using current-voltage measurements at various temperatures. After initial analysis SPDE, DCR and jitter measurements were undertaken using the time-correlated single-photon counting (TCSPC) technique.<sup>16</sup> Measurements were taken from 78 K to 175 K, using 1310 nm light with  $\ll 1$  photon per pulse and 50 ns gate times (Fig. 6). Significant improvements in the DCR and SPDE have been measured compared to previously reported values.<sup>14,15</sup> A record high SPDE of 18% for Ge-on-Si SPADs was measured for a device temperature of 78 K with an excess bias of 4.5 %. The lowest NEP recorded for that temperature was  $2.2 \times 10^{-16} \text{ WHz}^{-1/2}$  was demonstrated at 78 K. Without an anti-reflective coating (ARC) the amount of light reflected from the surface will be around 38 %, when a high quality ARC is used the SPDE should improve by 60 % which would lead to an SPDE of 30 %.

The wavelength dependence of the SPDE was also investigated. The high efficiency region is defined here as the wavelengths where the SPDE drops to 50 % of the maximum value, and for these devices this depends on the direct bandgap of the Ge absorption layer. The increase in measurement temperature allows an increase in the long wavelength edge of the high efficiency region due to band gap narrowing. Measurements were undertaken up to a maximum temperature of 175 K before the DCR became too high to measure SPDE in these devices. The SPDE dependence on temperature can be observed in Fig. 7, the high efficiency edge shifts to longer wavelengths as the temperature increases. Figure 7 shows the results of absorption calculations for a 1  $\mu\text{m}$  Ge layer which has a built in 0.18% tensile strain acquired during growth due to thermal expansion mis-match between Si and Ge. The calculations use a direct band absorption model<sup>19</sup> with strain deformation potentials for Si and Ge,<sup>20</sup> which does not account for indirect absorption which leads to the long wavelength tail in the experimental SPDE curves. Our calculations demonstrate that these devices should have a high SPDE for 1550 nm light with an operating temperature near 250 K. The wavelength of operation could also be expanded by increasing the thickness of the absorption region. An increase of the i-Ge region from 1  $\mu\text{m}$  to 2  $\mu\text{m}$  will increase the absorption of light which would increase the SPDE for all wavelengths and extend the spectral cut-off to

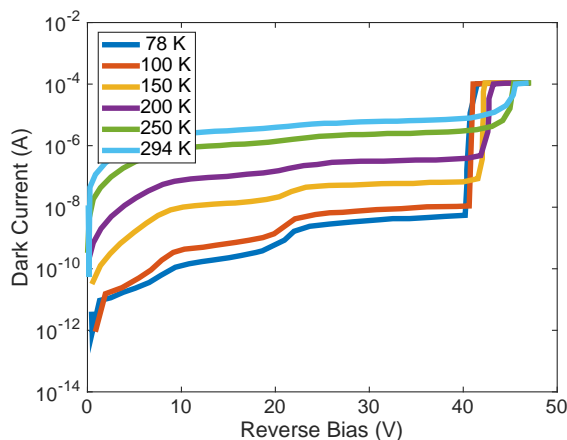


Figure 5. Dark current of a 100  $\mu\text{m}$  diameter Ge-on-Si SPAD operated at different temperatures between 294 K and 78 K as a function of reverse bias

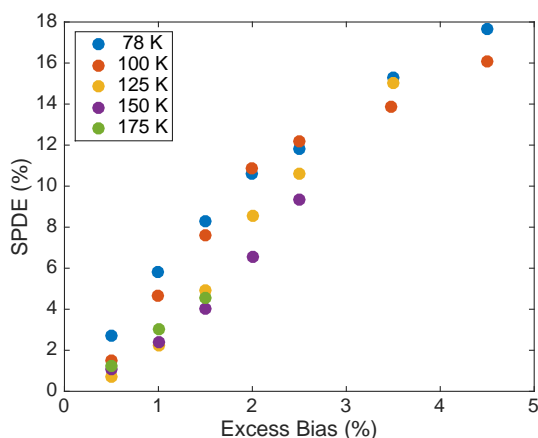


Figure 6. SPDE as a function of excess bias for temperatures from 78 K to 175 K for device without anti-reflective coating. High temperature measurements are limited to lower excess bias due to higher dark count rates.

longer wavelengths. Figure 8 shows the wavelength where the SPDE is equal to 50% of the SPDE at 1450 nm for 1  $\mu\text{m}$  as a function of temperature. As a comparison, the same model is used for a SPAD with a thicker 2  $\mu\text{m}$  Ge absorber layer.

For a SPAD device, the jitter is a measure of the timing error between the photon arrival and detection time of the current pulse. The jitter is calculated from the full-width-half-maximum width (FWHM) of the peak of the timing histogram of the pulse detections. A timing histogram was taken at an excess bias of 5.5% at 78 K device temperature with a laser source of 1310 nm. From the FWHM of the peak our devices demonstrate a jitter of 310 ps. This level of jitter is reasonable for the 1.5  $\mu\text{m}$  avalanche thickness of the device. It is expected that smaller diameter devices will reduce the amount of jitter.

#### 4. CONCLUSIONS

We have reported a novel planar Ge-on-Si SPAD device that was processed using CMOS foundry compatible processes. This 100  $\mu\text{m}$  diameter device has demonstrated a SPDE of 18% at 78 K for 1310 nm wavelength light with a NEP of  $2.2 \times 10^{-16} \text{ WHz}^{-1/2}$  at a temperature of 78 K. These results represent a significant improvement over previously reported Ge-on-Si SPAD devices. These results open up the potential for Ge-on-Si SPAD devices to be used in a range of quantum technology applications that operate at the telecommunications

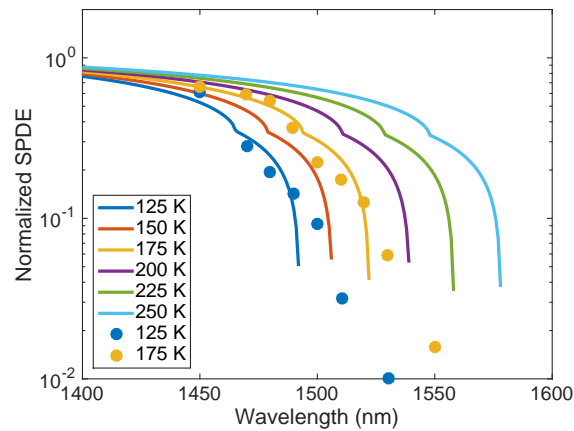


Figure 7. The measured SPDE for device temperatures of 125 and 175 K as a function of wavelength. The calculated absorption for various operating temperatures. The high efficiency region extends to longer wavelengths as the device temperature increases. Calculations demonstrate high efficiency for 1550 nm light at 250 K.

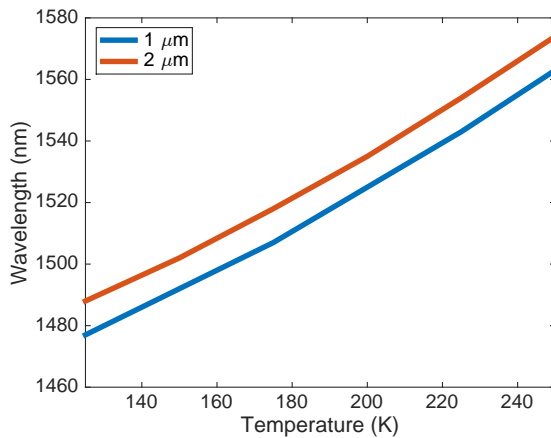


Figure 8. The high efficiency cut-off wavelength from the direct band edge of the Ge absorption region from absorption calculations. The thicker absorption region will shift the high efficiency edge to higher wavelengths for a given device temperature.

wavelengths of 1310 nm and 1550 nm. These results are from a first generation of planar SPAD designs and future optimization of the device design and fabrication has the potential to improve the detection efficiency, reduce the DCR and improve the maximum operating temperature further potentially allowing high SPDE at Peltier cooler temperatures for 1310 nm and 1550 nm operation with silicon foundry compatibility.

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