Energy-Efficient Start-up Power Management for Batteryless Biomedical Implant Devices

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***Abstract*— This paper presents a solar energy harvesting power management using the high-efficiency switched-capacitor DC-DC converter for biomedical implant applications. By employing an on-chip start-up circuit with parallel connected Photovoltaic (PV) cells, a small efficiency improvement can be obtained when compared with the traditional stacked photodiode methodology to boost the harvested voltage while preserving a single-chip solution. The PV cells have been optimised in the PC1D software and the optimal parameters modelled in the Cadence environment. A cross-coupled circuit with level shifter loop is also proposed to improve the overall step up voltage output and hybrid converter increases the start-up speed by 23.5%. The proposed system is implemented in a standard 0.18-µm CMOS technology. Simulation results show that the 4-phase start-up and cross-coupled with level-shifter can achieve a maximum efficiency of 60%.**

Keywords*— *Implantable electronics, Switched Capacitor, Hybrid DC-DC converter, Solar power.

I. INTRODUCTION

Nowadays most biomedical devices are powered by a battery or rechargeable battery. Nevertheless, surgical replacement of the battery is required when it is depleted. In this case, a reliable and power harvester or generator needs to be applied to decrease the risk and cost of operation. Comparing with an alternative energy source, sunlight is omnipresent, reliable and renewable energy, which can also be harvested by the solar cell under the skin. To be specific, when implants with solar cell powered are irradiated, the penetrated light especially invisible and Near-infrared region will be converted into electricity and power the CMOS circuitry embedded in the same chip.

The output of the PV cell is too low to operate for the electronics module on chips. Hence mean of power management or power converter is necessary to supply required power to the loads. The circuit such as [1] which power the peripheral part of the circuits such as clock and digital circuits to make an operation of the converter possible by stacking additional PV cell. This design, however, power manage the whole operation of hybrid converters from a single photovoltaic cell energy source and boosted the high voltage conversion ratio (VCR) for applications on the chip. This is presented in the Fig. 1. In this paper, we will be discussing the how the voltage from the on-chip photovoltaic cell is yield and proposed technique by using a level shifter. Then the implantation of the circuit followed by the result discussion.

One example of power management circuits for a photovoltaic cell can be observed in [2]. In which Dickson charge pump with the fast-transient response is compared with cross-coupled which has high voltage conversion. However, similar concept of high voltage clock for the partial stage of charge pump has presented in [3] in which modified Dickson charge pump NCP-3 which use high voltage clock generator and supply to the MOSFET controlled gate next to output stage to eliminate threshold voltage losses. Assume such high voltage clock are not external and consume primary energy source, and rather than supplying to the gate but to the capacitor instead, it would not have enough power to do so because the current gain is inversely proportional to the voltage gain in Dickson Charge pump. Similarly, level shifting from output to control the gate of crossed couple switches has been presented in [4]. However, this is only to supply the gate of the neighbour transistor pairs to eliminate reversion loss [5].

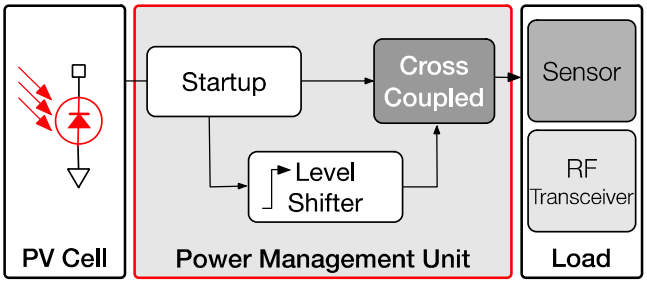


Fig. 1. The PV cell and power management procedure.

In this paper, the 4-phase rotation series-parallel converter is used as the start-up converter due to its fast-transient response and simultaneous dual outputs. This secondary output enables the idea of supplying high voltage clock to the main charge pump, 3-stages cross-coupled circuit [6]. The level shifter proposed in [7] is used to increase the amplitude of the clock signal to the output of the start-up charge pump to gather more VGR at the second main charge pump output.

II. METHODOLOGY AND CIRCUITRY DESCRIPTION

A. On-Chip Photovoltaic Cells

Photovoltaic (PV) cell is a reliable and renewable power supply which performs as a diode in the dark but photo-generated power is produced under the light. The performance of a PV cell highly depends on the doping profile and material. PN homojunction is the most common configuration for photodiode and silicon is the most common material with high efficiency. The structure of the PV cell is shown in Fig. 2, where shows the PV cell can also be equivalent to a diode with series resistance and shunt resistance. Device simulation is applied to test the accuracy

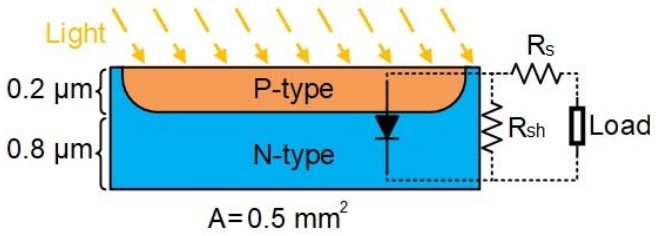


Fig. 2. Schematic and structure of the solar cell, where R_{sh} and R_s are shunt and series stray resistance, A is the area of the active region.

of a schematic model. The PC1D simulator is to make a device analysis, while Cadence is for an equivalent circuit which is embedded with the other power management circuit. The current-voltage (IV) curves provide the performance of the solar cell. The vitals of parameters such as open-circuit voltage (Voc), short-circuit current (Isc), Filling factor (FF) and efficiency (ηeff) can be achieved by Eq. 1 and Eq. 2 from IV curve [8].

$$I(V) = I_{sc} - I_d(V) - \frac{V+I(V)R_s}{R_{sh}} \quad (1)$$

$$\eta_{eff} = \frac{V_{oc}\times I_{sc}\times FF}{G\times A} \quad (2)$$

B. *Start-up Novel 4-phase rotation topology*

The 4-phase rotation series-parallel approach converter is used for the start-up circuit to boost from (V_{PV}) solar cell output to approximately ($2V_{PV}$) by using the Double-Boost mode. This converter is designed to configure two different simultaneous regulated stable dual outputs (V_{o1}, V_{o2}) by using switch-mode regulation. Power stage network is divided into two conceptual internal networks (Net0, Net1) and boost operation will perform in Net0 while another boost output produces at Net1 [9]. Therefore, in every clock cycle, there will be two active corresponding internal outputs at (Out1-Out4). These two active internal outputs will then connect to the external two output (V_{o1}, V_{o2}), Fig. 4. As a result, two outputs of ($2V_{PV}$, $2V_{PV}$) is achieved at (V_{o1}, V_{o2}) from the input from solar cell output (V_{PV}).

C. *Level-shifted Cross-coupled Circuit*

By taking advantage of two outputs, which hold the same voltages from the start-up converter, V_{o1} uses as an input to the 3-stages cross-coupled converter and the second one V_{o2} is used to level shift the amplitude of the clock. The high amplitude clocks is biased to last two stages of the cross-coupled capacitors and achieved the high voltage output as a result. This is only possible thanks to dual outputs a 4-phase rotation design that produce simultaneous second output with the same voltage gain ratios. Despite numerous attempts boosting the clock amplitude with either the output of a

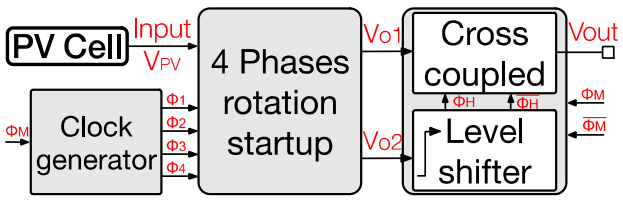


Fig. 3. Simplified schematic showing the proposed single-chip power management crucial blocks.

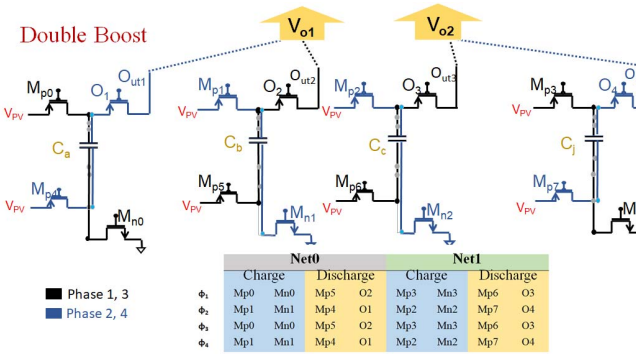


Fig. 4. Schematic circuits of the Novel 4phase rotation topology.

Dickson charge pump or the cross-coupled to supply VDDH of the level shifter, none of them can produce this simultaneously due to redistribution loss and output current is too small to drive the capacitor in main charge pump.

D. *Level-shifting clock*

The main challenge is to raise a supplied clock to the output of the start-up charge pump is V_{o2} cannot directly connect in series with two clocks (ϕM, $\overline{\phi M}$). Therefore, the level shifter [7] is used to level shift the amplitude of the clock from V_{PV}, powered from the PV cell, is pulled up to the higher amplitude (V_{o2}). To achieve that, one output of the previous start-up circuits will act as the V_{DDH} of the level shifter, and thus original amplitude of the clock will raise to new V_{DDH} value. This amplitude shifted clock will then biased in last two stages of the cross-coupled charge pump.

III. Design and Implementation

This work is implemented in a standard 0.18 µm CMOS technology. Now turning point to the scenario of PV cell, AM 1.5G regulates light irradiance (G) as 1000 W/m2 (We assume the light propagates with a 90o incident angle and device is perpendicular to the incident light), and the ambient temperature is 300K. It should be mentioned that the transmittance of skin is set up as 20% according to the

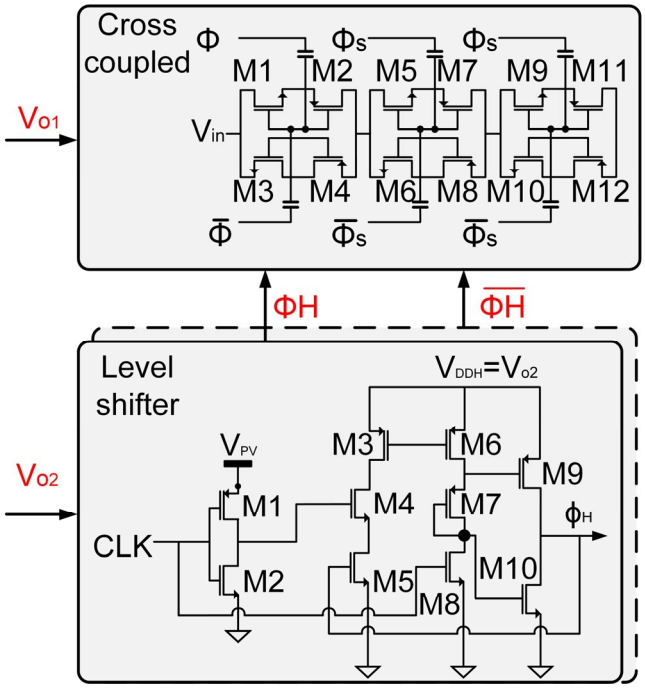
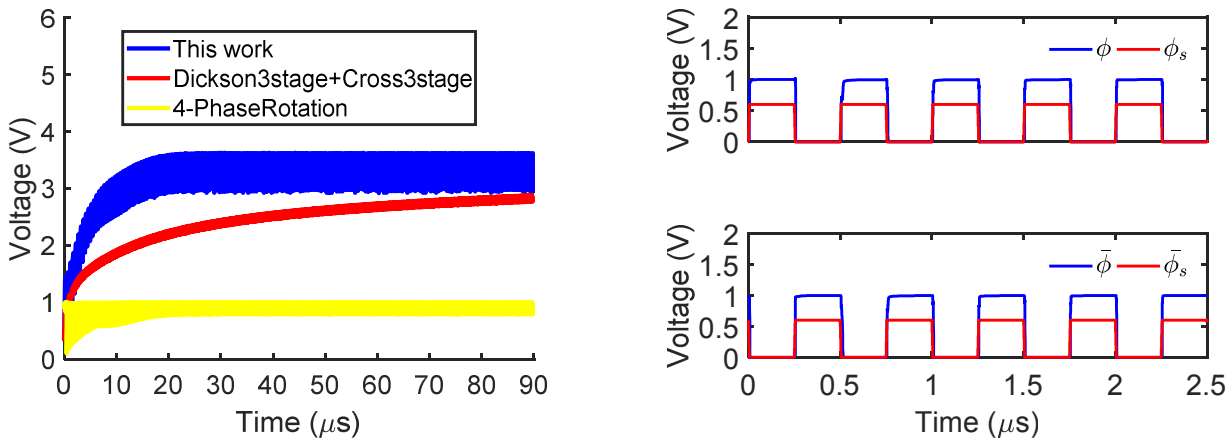


Fig. 5. Schematic circuits of the cross-coupled and level-shifter blocks.



(a) (b)

Fig. 6. (a) Output voltages of the proposed 4-phase rotation series-parallel and cross-coupled hybrid converters in comparison with Dickson and crossed-couple 3stages hybrid converters and (b) the level shifted clock powered by the secondary output of start-up charge pump.

research from Munna Khan et al (2015) [10]. Geometries of the photodiode are defined as follows: area (A) is 0.5 mm^2 and the thickness is 1µm. The thickness for P and N junction are 0.2 µm and 0.8 µm respectively.

The implantation of the start-up series-parallel charge pump has presented in [11], in which the series of D-flip flops are employed to enable four phases and the ring oscillator circuit further enhance the non-overlapping to avoid charge settling and short-circuit loss [12]. These non-overlapping clocks are denoted as (ϕ_1-ϕ_4) in Fig. 3.

In the power stage, there are four 20 pF capacitors and is controlled by 16 switches (8 nMOS, 8 pMOS). the width and length of the pMOS and nMOS are 25µm and 6µm respectively for both charge pumps. However, only half switches are used in every clock phase. Due to 4-phases topology, all the internal outputs which active at the different time in Fig. 4 interleaved between (O_{ut1}, O_{ut2}) and (O_{ut3}, O_{ut4}) to produce constant 1V outputs to both V_{o1} and V_{o2} respectively.

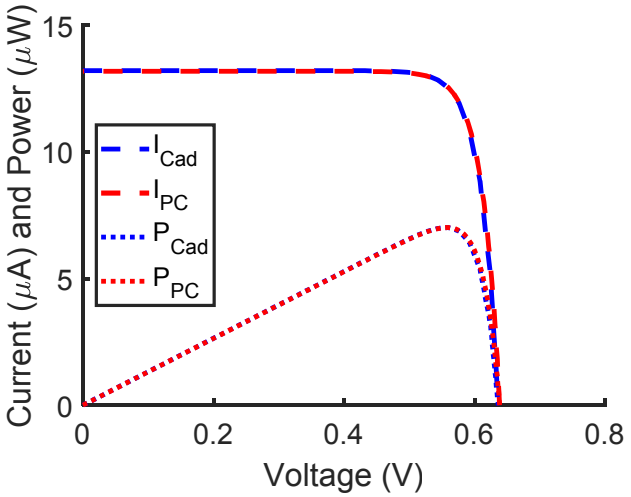


Fig. 7. IV curve comparison between PC1D and Cadence, where I_{Cad} and P_{Cad} are current and power in the Cadence environment, and $I_{PC,}$ as well as $P_{PC,}$ are current and power in PC1D software.

This is then supplied as an input of the main charge pump, the three stages cross-coupled circuit, and V_{DDH} of the level shifter. Only half a size of capacitors (10 pF) is utilised for a cross-coupled circuit. In Fig. 6, there is a comparison result with the hybrid circuit used in [6] is re-simulated with the same operating frequency as this proposed design (2 MHz). The size of the capacitors is 3×20 pF for Dickson and 6×20 pF for a cross-coupled charge pumps are simulated. Therefore, in comparison this proposed hybrid design employ less total capacitance and still provide the better VCR.

IV. RESULTS AND DISCUSSION

The solar cell simulation results of Cadence and PC1D tools are shown in Fig. 7. It provides a V_{oc} of 0.64 V, an I_{sc} of 13.17 µA and a P_{max} of 7.01 µW (From simulation results). Considering the results above, the FF and η_{eff} can be achieved 0.831 and 3.55% respectively.

The proposed hybrid converter is simulated in a Cadence software. The results in Fig. 6(b) show the output of the clock and clock bar which is powered by the PV cell voltage and hold the amplitude of 0.53V (at maximum power point). After the level shift, since the V_{o2} supplies the V_{DDH} of the level shifter, 0.998 (approx.1V) is acquired for new clock amplitude. The operation frequency of 2 MHz is used for all the clocks.

The Fig. 6(a) demonstrate the output condition of first and second converters. As observed, the output voltage of the start-up converter produces 0.998V and its rotation topology interleave the output to regulate at continuous 1V supply. The second stage of the converter produces 3.5-2.9 V peak-to-peak voltage at no load conditions. The total output current is between 4-6 µA. The proposed hybrid converter has the 20 µs transient time to reach the saturation. The overall efficiency of the hybrid boost converter is 40-60%.

Finally, comparison with low powered Dickson [13] and cross-coupled circuit [6] in hybrid connection are simulated as 3-stages each, for which both charge pumps use full 20 pF capacitors. The same operation frequency 2 MHz as the proposed circuit is applied to compare the output condition. As a result, 2.8 V is yield at saturation after a transient time of 85 µs, Fig. 6(a). The overall results are recorded in Table I.

TABLE I. TABLE OF THE SPECIFICATION

Specification	This work
Type	4phase + 3stage Cross
Input (V)	0.531
Output (V)	3.53
Conversion Ratios	6.64
Frequency (MHz)	2
I_{out} (µA)	4 - 6
P_{out_max}(µW)	21
Ripple (mV)	60
Efficiency (%)	40 - 60
$C_{Integrated}$ (pF)	4 × 20 4 × 10

V. CONCLUSION

In this paper, a solar energy harvesting power management using the high-efficiency DC-DC converter for biomedical implant applications is introduced. The proposed system employs a start-up circuit with parallel connected PV cells to derive energy from an integrated photodiode and to produce a high output voltage while maintaining a single substrate procedure. The PV cells have been modelled and simulated in the PC1D and the optimal parameters formed in the Cadence. A cross-coupled circuit with level shifter loop is also proposed to improve the efficiency and increase the startup speed by 23.5%. The proposed system is implemented in a standard 0.18-µm CMOS technology. Our stated solar energy harvesting system produces high efficiency, making it suitable for low-cost ultra-compact robust subdermal implant applications. The future work carries to combine sensors on the system with closed loop maximum power point tracking (MPPT) capability. As to the solar cell, the AM1.5G will be replaced by a different power density produced by near infrared light and tissue loss will be investigated by optic analysis.

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