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# Low noise and high photodetection probability SPAD in 180 nm standard CMOS technology

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**Abstract**—A square shaped, low noise and high photo-response single photon avalanche diode suitable for circuit integration, implemented in a standard CMOS 180 nm high voltage technology, is presented. In this work, a p+ to shallow n-well junction was engineered with a very smooth electric field profile guard ring to attain a photo detection probability peak higher than 50% with a median dark count rate lower than 2 Hz/ $\mu\text{m}^2$  when operated at an excess bias of 4 V. The reported timing jitter full width at half maximum is below 300 ps for 640 nm laser pulses.

**Keywords**—single photon avalanche diode; SPAD; CMOS; low-light (vision); photo detector; image sensor.

## I. INTRODUCTION

The use of CMOS single photon avalanche diodes (SPADs) in biomedical sensing and imaging has increased over time thanks to their performance in terms of fast acquisition, high sensitivity and portability [1]. Typical applications include fluorescence lifetime imaging microscopy (FLIM) [2], fluorescence [3], Raman spectroscopy [4], positron emission tomography (PET) detectors [5], and x-ray sensing [6]. All these applications require high sensitivity and extremely fast resolution on the order of picoseconds [7]. Additionally, SPADs are a suitable technology for portable imaging applications such as fluorescence endoscopic capsules [8], where low power consumption and small size can be achieved. One common method used to minimize power consumption and maximize the sensitivity is to minimize the dark count rate (DCR) while maximizing the photo detection efficiency, which is dependent on the photo detection probability (PDP) and fill factor. SPADs with exceptionally low DCR, high photon detection efficiency, and high dynamic range (DR) have been previously reported using non-standard CMOS process having the disadvantages of increased fabrication complexity and high production cost. The low DCR is obtained by using customized enrichment layers manufactured in non-standard CMOS technologies [9-11]. Very high efficiency CMOS SPADs with extremely complex on chip electronics but with very low fill factors have also been reported [12]. In such cases, microlenses are typically used to recover for the light-capture loss by concentrating light onto the active area, up to a factor of 10 [13]. This method adds complexity to the optics set up, such as misalignment and illumination non-uniformity. Exceptionally high DR values, larger than 100 dB, have been achieved by non-paralyzable devices, using active quenching circuits to

prevent saturation at high count rates, but at the expense of fill factor [14].

In this paper, we report a square shaped photo-carrier diffusion SPAD designed with a narrow depletion region and wide photo collection region. The SPAD was manufactured at Austriamicrosystem (AMS AG) in a standard 180 nm high voltage (HV) CMOS process. It achieves an exceptionally low DCR smaller than 2 Hz/ $\mu\text{m}^2$ , without the need for special implants, with a PDP peak greater than 50% when operated at 4 V of excess bias. The timing jitter performances are higher than state-of-the-art SPADs, yet also achieve sub-nanosecond full width (FW) at 10% for the red wavelength. Being designed in a standard 180 nm technology, this device is expected to be not only low-cost but will allow for easier integration into existing intellectual property cores (IPs) resulting in high resolution arrays particularly suited for portable fluorescence applications.

The following sections are organized as follows: Section II introduces the device design; Section III presents the device characterization and comparison with state-of-the-art SPADs; Section IV concludes the manuscript.

## II. DEVICE DESIGN

The proposed SPAD is composed of a p+ to shallow n-well junction. The cross-section is presented in Fig.1. The shallow n-well layer enhances the electric field (EF) beneath the p+ active area [15] whilst the guard ring, implemented by a shallow p-well (s-pw, blue area in Fig. 1) into a deep p-well, effectively reduces the EF to prevent the active junction from premature breakdown. The shallow p-well acts as cushion preventing an abrupt change of doping profile and EF between the active area and the deep p-well. The width of the guard ring and its distance to the n-well are designed to achieve the smallest possible EF value at the p to n interface whilst

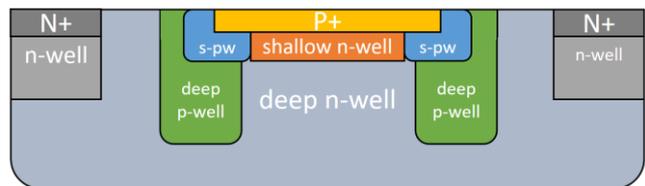


Fig. 1. Cross-section of SPAD layout, shallow p-wells (s-pw) are shown in blue.

minimizing the pixel pitch size. The deep n-well acts as a photocollection region, allowing collected photons to diffuse into the avalanche region.

The fabricated device, shown in Fig. 2, has a squared active area with smooth corners to alleviate early breakdown. The active area side dimension is  $12.08\ \mu\text{m}$  and the cathode-to-cathode distance is  $20.4\ \mu\text{m}$ . This geometry was specifically chosen to maximize the fill factor, as the active area results in a 1.2 % size increase compared to a SPAD with a circular shaped active area, and also to reduce the DCR.

### III. MEASUREMENT

The proposed SPAD was characterized for DCR, PDP, and timing jitter. It was tested with an external passive quenching circuit, comprised of a  $100\ \text{k}\Omega$  resistor with an average dead time of  $1\ \mu\text{s}$ . The measured breakdown voltage is  $16.8\ \text{V}$ .

**DCR** represents the base noise level of a SPAD caused by parasitic avalanches happening in the dark due to thermal noise and band-to-band tunneling effects [19]. DCR measurements were performed on three CMOS dies at room temperature ( $25^\circ\text{C}$ ) using an InfiniiVision MSO-X-3054T oscilloscope with statistical analysis capability, as shown in Fig. 3. For every measurement, the mean DCR value, with an acquisition time of at least 2 min, was recorded; the results are reported in Fig. 4. For an excess bias of 4 V the measured DCR median is 217 Hz and the mean value is 220 Hz. At 1 V of excess bias the obtained DCR mean and median values are both 28 Hz. Fig. 5 shows a more detailed DCR experiment performed in an environmental chamber with temperature ranging from  $10^\circ\text{C}$  to  $40^\circ\text{C}$  at various excess voltage biases. Based on these results the DCR shows a stronger dependence on voltage than temperature, suggesting band-to-band tunneling as the primary noise source. The proposed device favorably compares with state-of-the-art SPADs in [9-10, 15, 17,19-21], as illustrated in Fig. 6. The exceptionally low DCR was obtained by maximizing the breakdown voltage differences between the active area junction and the guard ring junction. The proposed device, used at 4 V (the maximum possible voltage bias), is outperformed by works reported in [11, 18, 22]. However, it must be considered that the work in [11] uses non-standard CMOS technology whilst works in [18, 22] show a higher DCR than the proposed device when they are used at their maximum voltage bias.

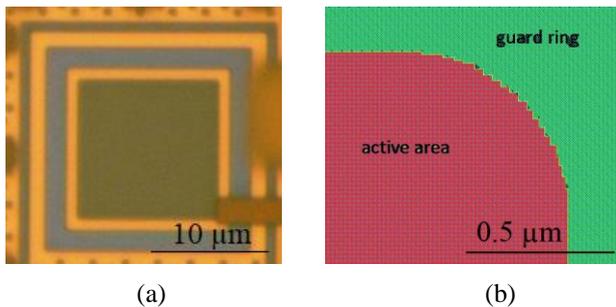


Fig. 2. (a) Micrograph of the manufactured device, and (b) smooth corner layout.

**PDP** is defined as the ratio between the number of incoming photons triggering an avalanche and the total number of photons illuminating the sensor at a selected wavelength in the span of white light spectrum (380-760 nm) [16]. The PDP was measured using a setup, illustrated in Fig. 7, comprising a Hammamatsu L7893 deuterium light source, a Jobin Yvon Horiba H20 monochromator, and a Thorlabs IS200 integrating

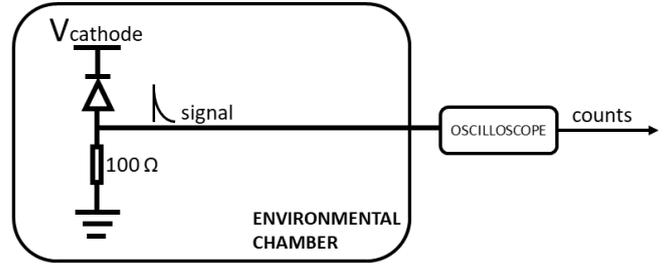


Fig. 3. Block diagram of the experimental setup for DCR measurement.

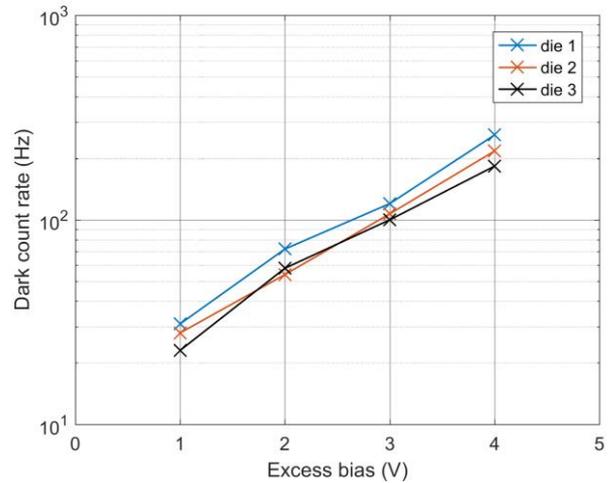


Fig. 4. Dark count rate measured from three different dies.

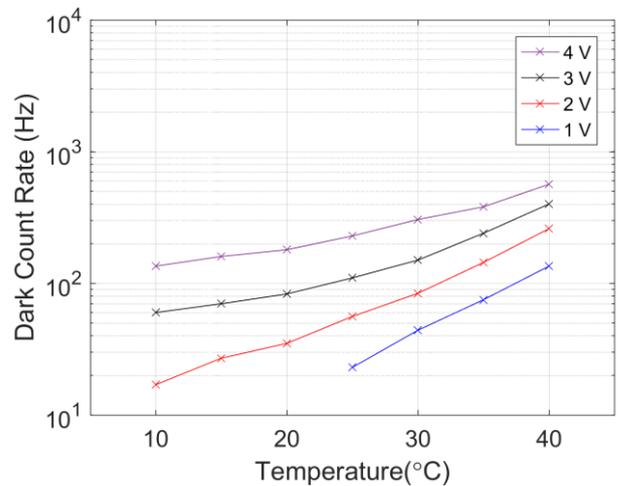


Fig. 5. Dark count rate measurements for several excess voltage biases at different temperatures.

sphere. Two optical fibers, coupling the light beam, were interconnected between the three aforementioned blocks. Two sets of two coated bi-convex lenses, Thorlabs LB1761-A, were used to collimate the light beam to the device under test (DUT) and to a calibrated Hamamtsu S1336 photodiode. The monochromator was operated by tuning the wavelength in 20 nm increments from 380 to 700 nm. The distance between the integrating sphere and the lenses, and the distance from the lenses to the sensors was equal in order to attain a constant attenuation of the light beam. Fig. 8 shows the PDP for different excess bias, it can be noted that when the SPAD is operated at the excess bias voltage of 4 V a PDP greater than 40 % from 420 to 540 nm is obtained with the highest peak achieving 55% at 480 nm. As the main application of the presented work is fluorescence imaging at green wavelength, the PDP drop which occurs towards the red wavelength does not represent an issue. Fig. 9 shows a comparison of the state-of-the-art SPADs with the highest PDP peak versus DCR at the maximum excess voltage biases, confirming the performance of the presented SPAD [9-11, 15, 17-22]. Only the work reported in [9] achieves a higher PDP than the presented device by using non-standard CMOS technology.

**Timing jitter** is the statistical distribution of the period of time between the absorption of a photon and the beginning of the avalanche [19]; the full width at half maximum (FWHM) and the FW at 10 % are provided as statistical distribution markers. Timing jitter measurements were performed with a setup, illustrated in Fig. 10, comprising of a Particulars LA-01-RB red laser (640 nm), including the corresponding filter and collimator, working at 200 kHz with a power rate of 75% (which corresponds to the minimum attainable power). The laser trigger and the SPAD response signal were analyzed using a Keysight DSA91304A Digital Signal Analyzer with histogram analysis capability. The measured FWHM value is 260 ps whilst the maximum FW at 10% is 663 ps. When compared to the state-of-the-art, the FWHM of the present device is the largest value and second best for the full width at 10% as shown in Table I. These results are primarily due to the squared shape of the active area.

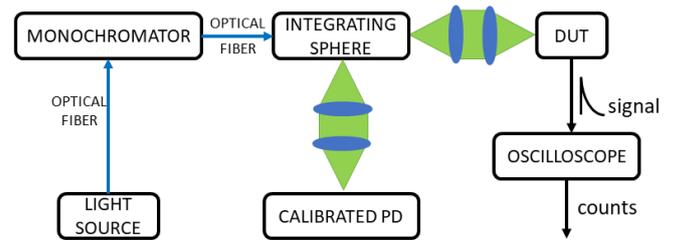


Fig. 7. Block diagram for PDP experimental setup.

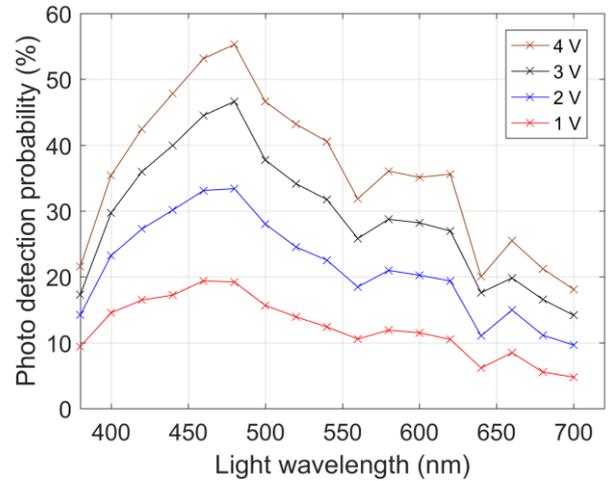


Fig. 8. Photo detection probability at different excess voltage biases.

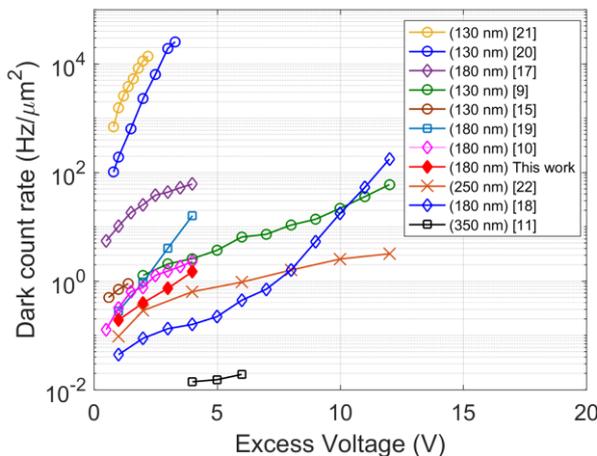


Fig. 6. State-of-the-art comparison for dark count rate. Different technology nodes are represented with different markers: square (350 nm), cross (250 nm), diamond (180 nm), and circle (130 nm).

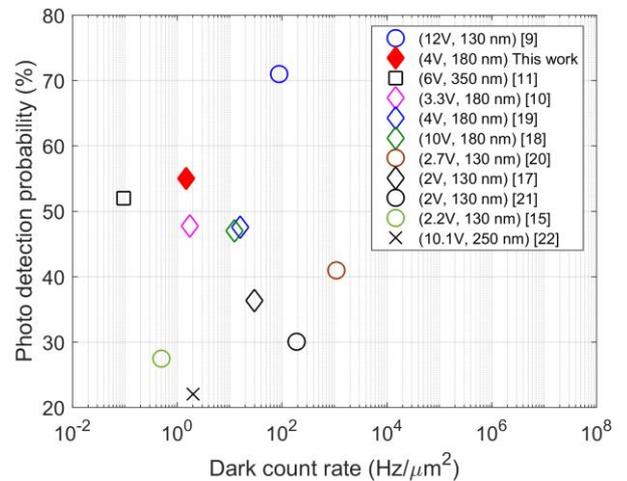


Fig. 9. State-of-the-art comparison for photo detection probability versus dark count rate. Legend reports excess voltage bias and technology node. Different technology nodes are reported with different markers: square (350 nm), cross (250 nm), diamond (180 nm), and circle (130 nm).

#### IV. CONCLUSION

The reported p+ to shallow n-well SPAD achieves the highest PDP with the lowest DCR at 4 V excess voltage from all the 180 nm devices in the state-of-the-art [10, 17-19]. This SPAD, operated at 4 V, with a PDP higher than 50 % from 420 to 540 nm, and DCR less than 1 kHz and sub-ns jitter performance is particularly suited for applications such as portable fluorescence sensors. Moreover, the proposed device shows a good compromise between low DCR and the high PDP peak.

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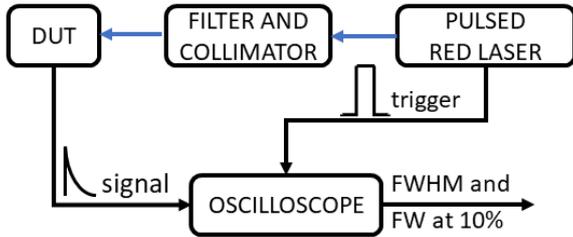


Fig. 10. Block diagram of the timing jitter measurement

TABLE I.  
STATE-OF-THE-ART SPAD COMPARISON FOR FWHM AND FW AT 10% USING RED LASER

	FWHM	FW at 10% maximum
Reference [9] (130 nm)	77 ps (654 nm)	3 ns (654 nm)
Reference [11] (350nm)	119 ps (780 nm)	-
Reference [17] (180 nm)	165 ps (790 nm)	550 ps (790 nm)
Reference [18] (180 nm)	86 ps (673 nm)	244 ps (673 nm)
Reference [19] 180 nm	141 ps (637 nm)	690 ps (637 nm)
<b>This work (180 nm)</b>	<b>260 ps (640 nm)</b>	<b>663 ps (640 nm)</b>

#### PERFORMANCE SUMMARY

Excess bias (V)	1	2	3	4
Median DCR at 25°C (Hz)	28	58	107	217
PDP peak (%) (at 480nm)	18	33	46	55
Timing jitter FWHM (ps)	-	-	-	<b>260</b>
Timing jitter FW at 10 % (ps)	-	-	-	<b>663</b>

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