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Correlation between the Golden Ratio and Nanowire Transistor Performance †

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Abstract: An observation was made in this research regarding the fact that the signatures of isotropic charge distributions in silicon nanowire transistors (NWT) displayed identical characteristics to the golden ratio (Phi). In turn, a simulation was conducted regarding ultra-scaled n-type Si (NWT) with respect to the 5-nm complementary metal-oxide-semiconductor (CMOS) application. The results reveal that the amount of mobile charge in the channel and intrinsic speed of the device are determined by the device geometry and could also be correlated to the golden ratio (Phi). This paper highlights the issue that the optimization of NWT geometry could reduce the impact of the main sources of statistical variability on the Figure of Merit (FoM) of devices. In the context of industrial early successes in fabricating vertically stacked NWT, ensemble Monte Carlo (MC) simulations with quantum correction are used to accurately predict the drive current. This occurs alongside a consideration of the degree to which the carrier transport in the vertically stacked lateral NWTs are complex.

Keywords: silicon nanowire transistors; quantum confinement; golden ratio; technology computer aided design (TCAD); drift diffusion; Poisson-Schrödinger; simulations; 3D-Monte Carlo

1. Introduction

The golden ratio (commonly referred to as the golden section or golden mean, and denoted by the Greek letter Phi) is noteworthy for a variety of reasons: firstly, it can be observed in many naturally occurring patterns, artistic works, and mathematical phenomena; and secondly, in more recent years, the literature has uncovered specific nanoscale symmetry concealed within solid state matter, which reflects aspects of the golden ratio [1].

Despite the availability of numerous studies that have sought to measure natural instances of the golden ratio, a publication has yet to emergence addressing the effect that Phi has on the central parameters and performance of nano transistors, including gate all around (GAA) nanowire transistors (NWTs) [2]. As illuminated in studies such as [3,4], GAA NTWs constitute a promising device architecture that are anticipated to be used for technological advancement in the domain of nodes. In particular, owing to their favorable property of electrostatic integrity, GAA NTWs have been marked as one of the successors of Fin field effect transistor (FinFET) technology in the 5-nm technology node.

It is possible to establish an ideal compromise between leakage currents and GAA NTW performance by engineering device structures. In fact, the literature indicates that the nanowires' cross-sectional shape strongly affects NWTs' gate capacitance and mobile charge [5–7]. As a case in point, for an NWT characterized by <110> channel orientation, as well as an extended elliptical cross-section (where the long diameter is parallel to the surface of the silicon wafer), it is associated with the greatest mobile charge for a certain gate voltage. It is noteworthy that one of the key determinants of device performance has been established as the ratio of the major axis to the minor axis (namely, cross-section aspect ratio or AR). Nevertheless, industrial players have tended to only manufacture NWTs in two different versions: circular cylinder (or elliptical) NWTs [8,9] and nanosheet (or nanoslab) FETs [10]. Each version has its own trade-offs; however, the key difference between these two versions is the cross-sectional AR. Several critical design questions, including the optimal NWT cross-sectional aspect ratio, remain unanswered.

To answer this question, the AR of a GAA NWT is changed while the cross-sectional area is kept constant; surprisingly, the signatures of the isotropic/anisotropic charge distributions are observed as showing the same attributes as the golden ratio.

The immediate aim of the present research is to examine the distinctive structural and dimensional features of the transistors associated with 5-nm Si CMOS technology, thereby illuminating the quantum mobile charge to gate capacitance ratio [5,7], where the indicator of the intrinsic speed of the NWT is the intrinsic delay (τ) [11]. For the purpose of heightening the degree to which the obtained results are realistic, the simulations take into consideration the effect of quantum confinement, non-equilibrium transport, and contact resistance for such ultra-scaled NWTs. An examination of the correlation between the golden ratio and 5 nm NWT performance is also made to take into account the effect of the main sources of statistical variability (SV) [12].

The early successes of fabrication of vertically stacked lateral NWTs may help resolve degradation of the drive current per footprint while shrinking the contacted gate pitch at the 5 nm node [9,10]. The vertically stacked NWTs have also been included in the international technology roadmap for semiconductors (ITRS) roadmap [13]. In an attempt to determine the performance of vertically stacked of NWT with golden AR, the quantum correction achieved by Poison-Schrödinger was used together with non-equilibrium transport to calibrate the drift-diffusion of a single NWT [14,15]. The calibrated drift diffusion (DD) was then used to simulate the vertically stacked lateral NWTs.

The paper is organized as follows: following the introduction, Section 2 offers a device description. Section 3 gives a brief overview of the simulation and the device calibration methodology, while Section 4 discuss the results. Conclusions are provided in Section 5.

2. Device Description

In this study, two NWT structures are used; single lateral NWTs and vertically stacked lateral NWTs. The purpose is to determine the optimal AR, and Figure 1 shows a 3D representation and material details for the initial structure of the NWTs. The Si channel is wrapped in a 0.4 nm SiO_2 interfacial layer and a 0.8 nm HfO_2 (High-k) layer is added at the gate region. The doping concentration in the channel is $10^{14}/cm^3$, in the extensions $10^{20}/cm^3$, and in the source/drain $4 \times 10^{20}/cm^3$. The charge transport's direction is organized along with x-axis, and Table 1 outlines the cross-sectional dimensions for 9 elongated elliptical nanowires (each with the same cross-sectional area amounting to approximately 10π nm^2). In addition, the diameter of the NWT along the y-axis ranges from 4.44 nm to 9.0 nm, whereas the matching diameter along the z-axis ranges from 9.0 nm to 4.44 nm. Resultantly, variance with respect to the matching aspect ratio is from 2.020 to 0.490. It should also be noted that the cross-sectional dimensions include wires with Phi and 1/Phi values. For the estimation of NWTs' performance after determining the optimal AR, state-of-the-art technology keys such as source/drain doping profile, predictive contact resistance, and gate length were utilized for both single NWT and vertically stacked lateral NWT structures.

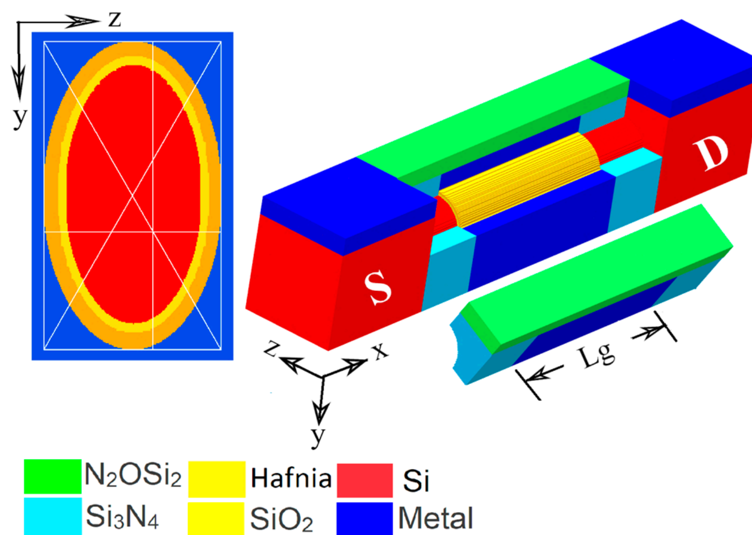

Figure 1. Three-dimensional representation of Si-NWTs (with cross-sectional dimensions of 5 nm × 8.1 nm), as well as chemical constituents. The straight, white lines indicate that golden ratio (Phi) can be observed on the cross-sectional slice with respect to the middle of the nanowire transistors (NWT) channel.

Table 1. Simulated devices' physical cross-section dimensions.

Z (nm) × Y (nm)	Y/Z	Area (nm^2)
4.440 × 9.0	2.020	10π
5 × 8.10 (Phi)	1.620	10π
5.7 × 7.0	0.810	10π
6.0 × 6.66	0.900	10π
6.32 × 6.32	1.000	10π
6.66 × 6.0	1.110	10π
7.0 × 5.7	1.220	10π
8.10 × 5 (1/Phi)	0.620	10π
9.0 × 4.44	0.490	10π

3. Methodology

In conjunction with the three-dimensional Monte-Carlo (MC) and drift-diffusion (DD) simulation techniques [12,16], this paper draws on Poisson-Schrödinger (PS) quantum corrections [17,18]. See Figure 2 for the author's approach to simulation. As will be clear to the reader, the quantum-corrected MC simulations, which valuably reflect the non-equilibrium transport effects [17,19–22], generate predictive simulation results. After conducting the DD simulations and, in turn, calibrating these in view of the MC results, the former can be used to reflect the contact resistance impacts [4]. Furthermore, it is possible to use the calibrated DD simulations to examine relative changes in I_{on}, thus facilitating design optimization and, in addition to this, the creation of efficient statistical variability (SV) and statistical reliability (SR) simulations [12,23,24].

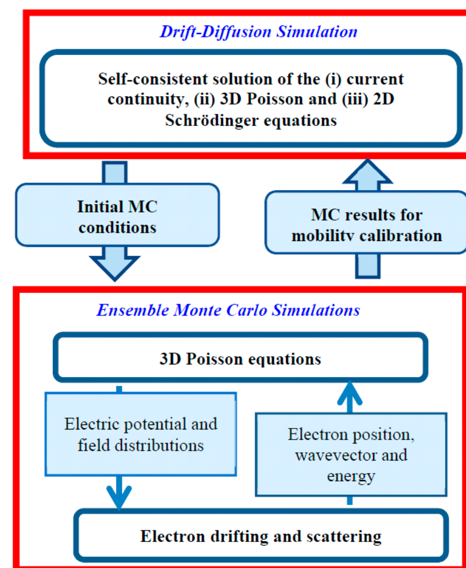

Figure 2. Flowchart for the overall simulation method. MC: Monte-Carlo.

4. Results and Discussions

The PS quantum corrections offer a precise charge distribution within the simulated NWTs' channel [5]. And Figure 3 gives the Phi ovals represented on a two-dimensional cross-section at the center of the gate. It is noteworthy that patterns of isotropic charge distribution derived from the PS simulations are comparable (in terms of their characteristics) to Phi, and despite the voltage-dependent nature of the charge distributions, the Phi ovals' signatures can be identified at every gate voltage.

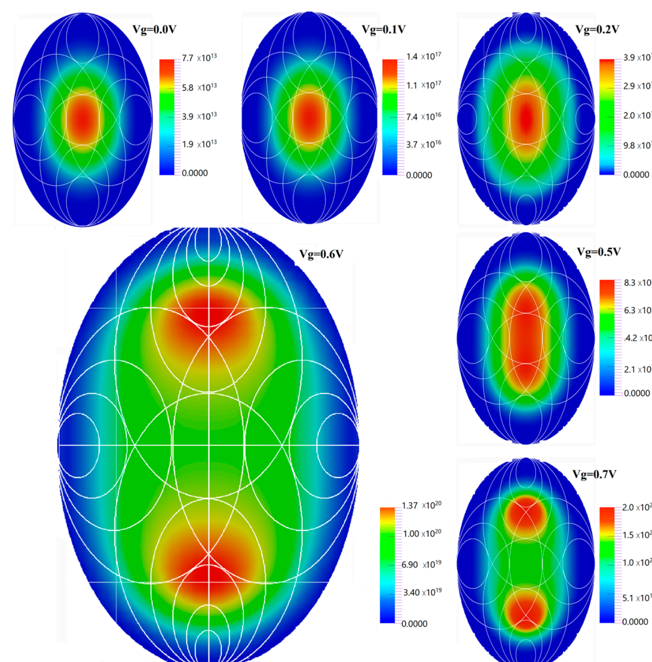

Figure 3. The Poisson-Schrödinger (PS) simulations' charge distribution results. Here, the Phi ovals (marked in white) emphasize the comparability between the golden ratio and the charge distribution within the 5 nm × 8.10 nm NWT cross-section. The slice cut is at the middle of NWT channel at gate bias (0, 0.1, 0.2, 0.5, 0.6, 0.7) Volt at high drain voltage V_D = 0.7 V. The gate length Lg = 12 nm.

For the purpose of evaluating the effect that the NWT cross-section dimension has on device performance in a reasonable manner, Figure 4 gives the gate voltage against the quantum mobile charge within the channel (for the initial 9 NWTs given in Table 1). Here, the alignment of the Q_M-V_G curves takes place by altering the gate work function, and the reader should recognize that the mobile charge is predicted in the middle of the channel. Perhaps the centrally interesting result to arise from our consideration of the Q_M-V_G attributes in Figure 4 relates to the fact that the greatest level of quantum charge is associated with NWTs which have the Phi and 1/Phi dimensional ratios. When comparatively examined against every other elliptical device, the NWT whose cross-section is precisely circular is associated with the lowest level of quantum charge.

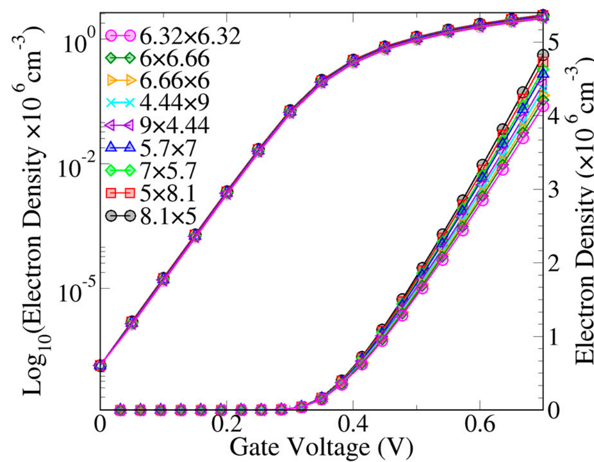

Figure 4. 9 NWT cross-section aspect ratios and the gate voltage dependence of the NWTs' quantum mobile charge. The crystallographic Silicon (Si) channel orientation is <110>. Each NWT has cross-sectional area $\approx 10\pi$ nm^2. The gate length = 12 nm.

In Tables 2 and 3, a certain gate voltage (V_G) is used for the <110> and <100> crystallographic orientations, thus facilitating a comparative examination of the simulated gate capacitance (C_G) and mobile quantum charge in the channel per-unit-length (Q_M). Q_M is in a direct and proportional relationship to the NWT gate capacitance, in view of the following equation:

$$Q_M = C_G(V_G - V_T), \quad (1)$$

where V_T and V_G denote the threshold voltage and gate voltage, respectively.

In view of this, it is reasonable to conclude that the fall in NWT gate capacitance brings about an attendant fall in the channel's mobile charge, thus reducing the overall level of transistor performance. In view of the information given in Tables 2 and 3, it is evidently the case that for the two crystallographic orientations, capacitance is greatest when the wires reflect Phi. As for the wires with the <100> crystallographic orientation, the charges in the Phi and 1/Phi instances are exactly the same, which can be accounted in reference to the m_Y and m_Z effective masses (of electrons).

Hence, it could conceivably be hypothesized that the two recent successful industrial attempts to build NWTs with cross-sectional AR $\approx$ 1 (circular NWT [8,9] and AR $\approx$ 3.5 (sheet NWT) [10] have overlooked the fact that AR contributes to NWT performance (in this study, the term "sheet NWT" refers to any NWT where $0.5 \geq$ AR ≥ 2).

Figure 5 compares the effect of 9 cross-section aspect ratios for Si NWTs on the I_D-V_G curves. Consistent with the data presented so far, the NWTs with cross-sections equal to 1/Phi and Phi own the highest I_{on} at low drain voltage as well as at high drain voltage.

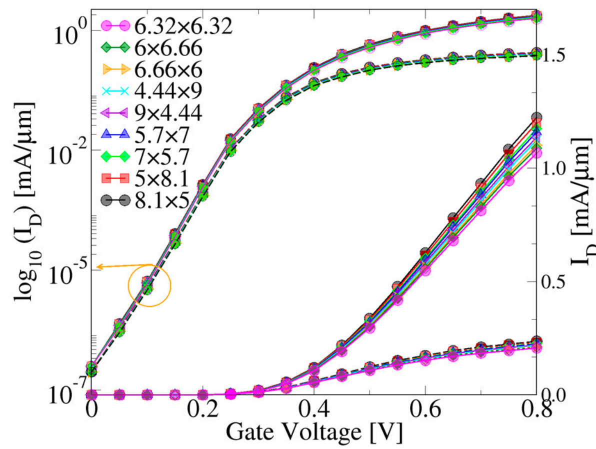

Figure 5. The effect of 9 cross-section aspect ratios for Si NWTs on the I_D-V_G curves. Dotted lines represent a low drain voltage (namely, V_D = 0.05 V), whereas continuous lines represent a high drain voltage (namely, V_D = 0.7 V). <110> is the channel orientation for Si, while the gate length amounts to 12 nm.

Table 2. Quantum charge to the gate capacitance ratio at identical Q_M at zero gate bias (for NWTs with crystallographic Silicon channel orientation <110>.

Z (nm) × Y (nm)	**Q_M (×10^7/cm)**	**C_G (10^{-10} F/cm)**	**Q_M/C_G (10^{17}/F)**	
		<110>		
4.44 × 9.0	2.73300	1.14010	2.3970	Oblate NWT
5 × 8.10 (Phi)	2.84200	1.14740	**2.4760**	
5.7 × 7.0	2.75000	1.12900	2.4350	
6.0 × 6.66	2.58010	1.10930	2.3260	
6.320 × 6.320	2.54800	1.10920	2.2970	Circular
6.660 × 6.0	2.63160	1.11680	2.3560	Prolate NWT
7.0 × 5.70	2.77380	1.13520	2.4400	
8.10 × 5 (1/Phi)	2.89200	1.16020	**2.4910**	
9.0 × 4.44	2.72700	1.13710	2.3980	

Table 3. Quantum charge to the gate capacitance ratio at identical Q_M at zero gate bias (for NWTs with crystallographic Silicon channel orientation <100>.

Z (nm) × Y (nm)	**Q_M (×10^7/cm)**	**C_G (10^{-10} F/cm)**	**Q_M/C_G (10^{17}/F)**	
		<100>		
4.44 × 90	2.73220	1.13500	2.40720	Oblate NWT
5 × 8.10 (Phi)	2.89000	1.15970	**2.49200**	
5.7 × 7.0	2.77940	1.13840	2.44410	
6.0 × 6.66	2.64030	1.11840	2.36070	
6.320 × 6.320	2.61020	1.11600	2.33760	Circular
6.660 × 6.0	2.64020	1.11800	2.36150	Prolate NWT
7.0 × 5.70	2.77930	1.13800	2.44220	
8.10 × 5 (1/Phi)	2.89100	1.15980	**2.49100**	
9.0 × 4.44	2.73210	1.13410	2.40900	

In Figure 6, it is clear that τ constitutes a function of L_G. In particular, τ is correlated in a direct way to the device's speed, where the NWTs' speed with respect to τ can be expressed as follows:

$$\tau = C_G(V_{DD}/I_{off}) \quad (2)$$

where C_G represents the total gate capacitance; $I_{off} = (I_H + I_L)/2$ represents the effective current, where $I_H = I_D$ ($V_G = V_{DD}$, $V_D = V_{DD}/2$), and $I_L = I_D$ ($V_G = V_{DD}/2$, $V_D = V_{DD}$). V_{DD} = 0.6 V, and the leakage current is I_{off} = 0.6 μA/μm. Figure 6 illustrates that NTWs with 8.10 nm × 5 nm and 5 nm × 8.10 nm are associated with the lowest value of τ, and the evaluation of τ is consistent with the Q_M/C_G results (see Table 2).

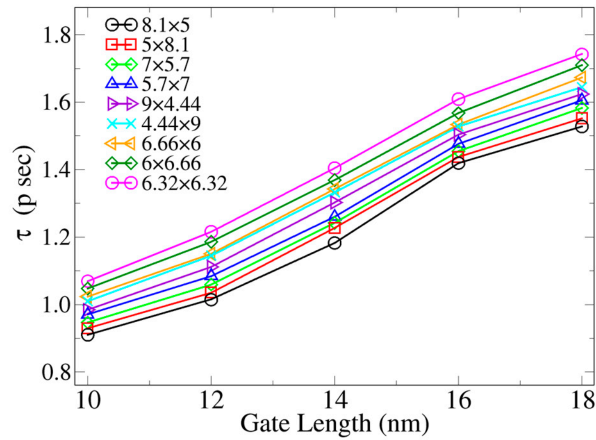

Figure 6. L_G with respect to τ for NWTs with varying cross-section aspect ratios (including Phi and 1/Phi). The Si channel orientation is <110>.

A much more systematic design of experiments would identify how NWTs' FOMs interact with other variables that are correlated to AR. Figure 7 shows a possible design of such experiments, including the effect of gate lengths and oxide thickness, and NWT cross-sectional dimensions on I_{off}, I_{on} and sub-threshold slope (SS). As this study concentrates on 5 nm NWT, three-cross-sectional areas with golden ratios are involved in the design of these experiments: (4 nm × 4.6 nm), (5 nm × 8.1 nm), and (6 nm × 6.9 nm), with corresponding cross-sectional-areas 4.6π, 10.125π, and 10.35π (nm^2). In all cases, only <110> channel orientation is considered.

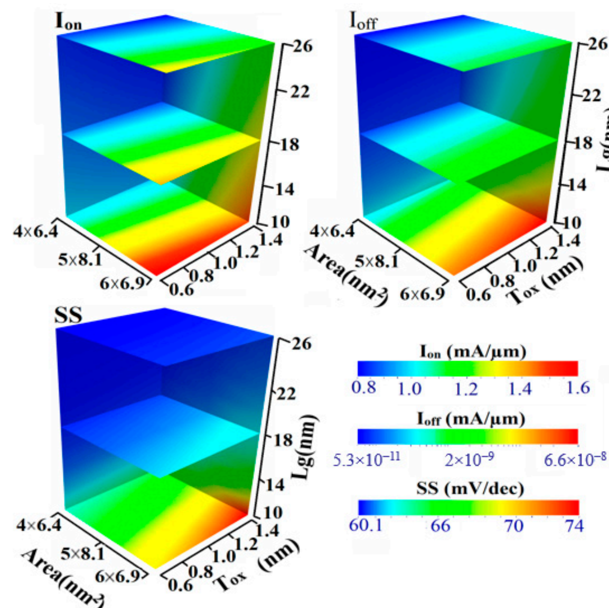

Figure 7. Experimental design for investigation of the impact of NWT size, L_G, and oxide thickness on drain-induced barrier lowering (DIBL), I_{off}, I_{on}, and V_T.

As in a tri gate (FinFETs) the on-current is closely proportional to the fin height of the fin or NWT diameter [25,26] In view of the simulation results, it is possible to conclude that the greatest value of the drive current is associated with the NWT characterized by the shortest gate length and, furthermore, the thinnest oxide. The SS reflects the electrostatic integrity of the transistors. The NWT with a long channel and narrow dimensions has better gate control, resulting in a steeper SS.

The key problem with ultra-scaled NWTs is the challenge of performance degradation, seen as degradation in the I_{on} per lay-out pitch I_{on} A/µm while maintaining low off-state leakage. Paired with altering NWT geometric features, along with crystallographic orientation, it is possible to enhance the electron transport attributes in Si NWTs by establishing a strain in the channel [27–29].

In Figure 8, the results are given for the simulated I_D-V_G characteristics of a NWT (5 nm × 8.10 nm [Phi]) with a crystallographic orientation of <110> at several tensile strain values. Evidently, in the 5% to 30% range, establishing a strain in the channel has a beneficial impact on the saturation current magnitude. Furthermore, establishing a 2 GPa tensile strain has a positive impact on NWT performance (approximately 30%) when considered in relation to the unstrained NWT. Nevertheless, the I_{on} barely reaches the margin of the industrial target for 5 nm node; hence, contact resistance is neglected in this case.

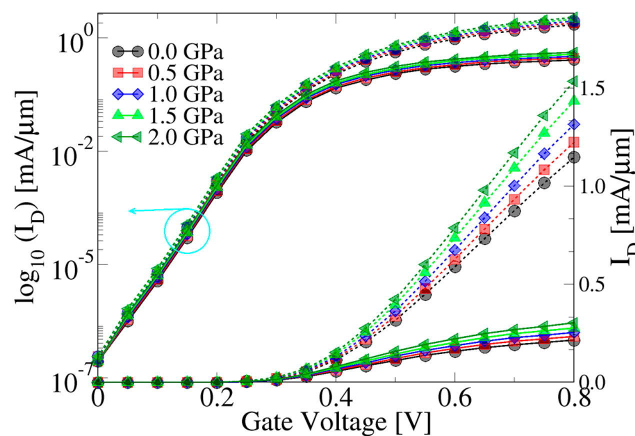

Figure 8. I_D-V_G curve plotted of the 5 nm × 8.10 nm strained silicon NWT at several channel strains. Dotted lines represent V_D = 0.7 V, whereas continuous lines represent V_D = 0.05 V. Crystallographic orientation of the Si channel is <110> and L_G = 12 nm.

Variability in the context of contemporary nanoscale transistor science is an increasingly important context, especially in view of process deviation and the inherent attributes of semiconductor materials and interfaces. Although the NWT with Phi cross-sectional AR has unique attractive features, it is useful to compare, in detail, the impact of the individual and combined local statistical variability sources on such an NWT. Statistical variability (SV) is given rise to by numerous variables, including random discrete dopants (RDD), metal gate granularity (MGG), and wire edge roughness (WER), all of which serve to predominate within NWT behavior.

Figure 9 gives V_T, I_{on}, DIBL, and I_{off} distributions subject to combined SV (RDD, WER, and MGG), all of which are reflective of the gate-first technology of the NWTs listed in Table 2. Comparing the normal distribution of ensembles of 1000 microscopically different transistors simulated for each one of the nine NWTs, it can be seen that the distributions are close to Gaussian. Furthermore, the normal distributions are shifted in consistency with results of I_D-V_G characteristics in Figure 5, hence causing the Phi and 1/Phi ratio NWTs to have better I_{on}, DIBL, V_T, and I_{off} results. This may be explained by the fact that NWTs with Phi and 1/Phi ratios have better electrostatic integrity and more mobile charge and gate capacitance.

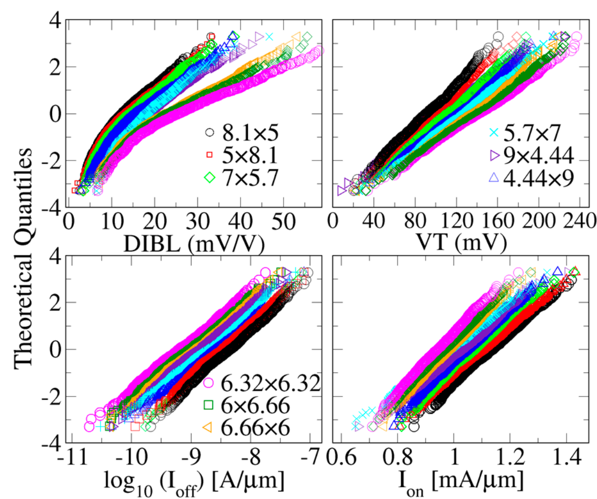

Figure 9. V_T, I_{on}, DIBL, and I_{off} distributions subject to combined SV (RDD, WER, and MGG), all of which are reflective of the gate-first technology of the NWTs listed in Table 2.

One of the most significant findings to emerge from these simulations is that Phi and 1/Phi ratios can thus be suggested as offering the optimal AR. The V_T and I_{on} variability depends on the parameters of the variability sources, and thus further investigations to assess the effects of individual SVs for Phi and 1/Phi NWTs on V_T and I_{on} are required. For each individual source, and for their combinations, ensembles of 1000 microscopically different transistors are thus simulated as shown in Figure 10 and Table 4. The effects of SV sources on I_{on} of Phi NWTs are similar to those of 1/Phi NWTs, with a 0.1 mA/µm shift in Gaussian distribution. This shift has relevance as the mobile charge Q_M in the channel of 1/Phi NWTs is higher than Q_M in the channel of Phi NWTs. Another important implication is that the I_{on} standard deviation of the 1/Phi NWTs is less than in the I_{on} SD of Phi NWTs for <110> channel orientation. Further, MGG is significantly wider in I_{on} variability than other SV sources. These findings are also valid for threshold voltage variability as shown in Figure 11 and Table 5.

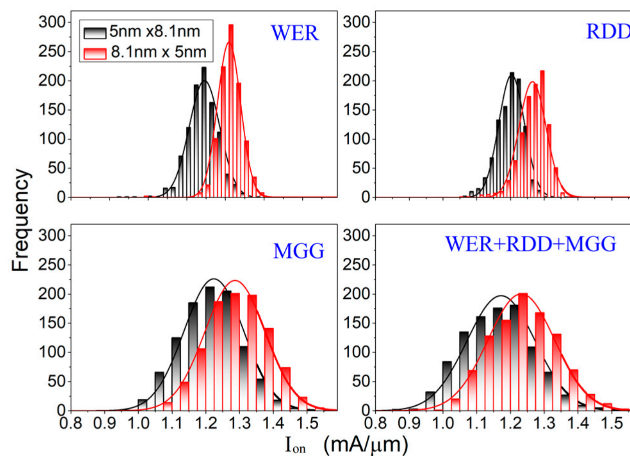

Figure 10. I_{on} distributions subject to combined individual SV and combined SV (RDD, WER, and MGG) which are representative of gate-first technology of Phi and 1/Phi NWTs.

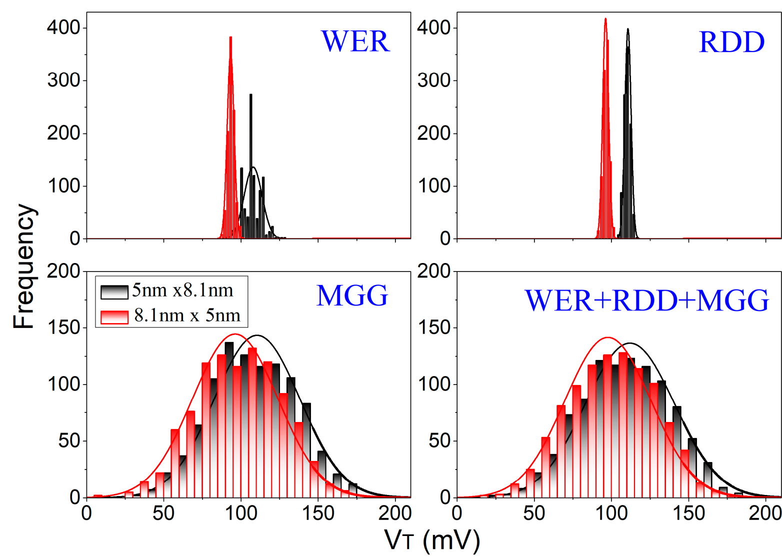

Figure 11. Threshold voltage (V_T) distributions subject to combined individual SV and combined SV (RDD, WER, and MGG) which are representative of gate-first technology of Phi and 1/Phi NWTs.

Table 4. Mean and standard deviation values of I_{on}, subject to combined individual SV and combined SV (RDD, WER, and MGG) which are representative of gate-first technology of Phi and 1/Phi NWTs.

I_{on} mA/µm	5 nm × 8.1 nm		8.1 nm × 5 nm	
	SD	**Mean**	**SD**	**Mean**
WER	0.0380	1.246	0.0276	1.310
RDD	0.0379	1.203	0.0401	1.265
MGG	0.0882	1.223	0.0893	1.286
SV	0.1031	1.171	0.0998	1.232

Table 5. Mean deviations and standard deviations values of V_T subject to combined individual SV and combined SV (RDD, WER, and MGG) which are representative of gate-first technology of Phi and 1/Phi NWTs.

V_T mV	5 nm × 8.1 nm		8.1 nm × 5 nm	
	SD	**Mean**	**SD**	**Mean**
WER	5.807	107.85	2.247	93.29
RDD	2.001	110.66	1.91	96.18
MGG	27.82	110.41	27.59	96.24
SV	28.52	111.9	27.74	97.65

Presented in Figure 12 are the distribution and correlations between extracted figures of merit (FoM), derived from the TCAD simulations conducted with respect to the degraded NWT with a trap sheet density amounting to 1×10^{12} /cm^2 when variability sources (RDD, WER, MGG) are considered. Both figures show a correlation between the V_T, I_{off}, and I_{on}. However, nevertheless, the correlation between DIBL and the remaining FoM is weak.

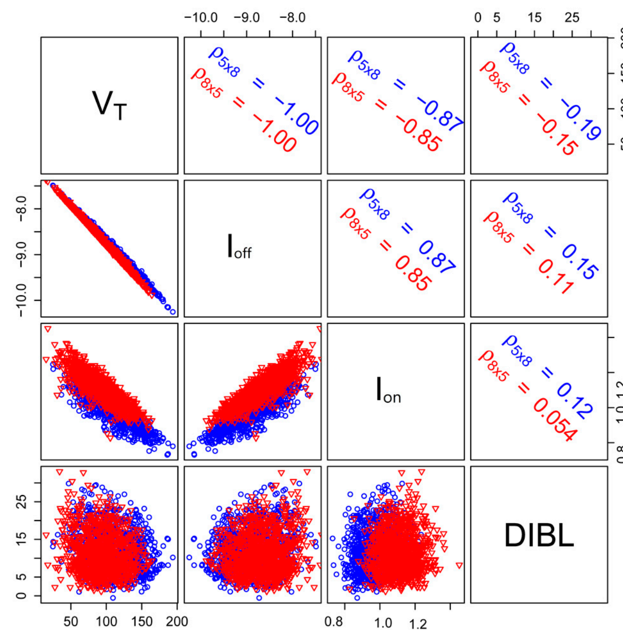

Figure 12. V_T, I_{on}, DIBL, and I_{off} distributions subject to combined SV (RDD, WER, and MGG), all of which are reflective of the gate-first technology of the NWTs given in Table 2.

The most obvious finding to emerge from the comparison of phi and 1/Phi NWTs is that the 1/Phi NWT has better I_{on} and therefore could be faster; however, the most important limitation lies in the fact that its footprint is wider than the Phi NWT, which has a negative effect on CMOS device density.

Recent developments in doping technology have exceeded 10^{21} cm [30], and such heavy S/D doping could also enhance the drive current. Nevertheless, contact resistance remains one of the greatest challenges for 5 nm technology. Figure 13 compares the I_{on} of Phi NWTs with S/D doping up to 1.2×10^{21} cm^{-3}, with contact resistance in the range (500–2500) Ω, and gate length (10–22) nm. At the predictive Lg = 12 nm and R = 2314 Ω of the 5 nm node [26,31,32], Figure 13 shows the I_{on} as 1.4 mA/µm.

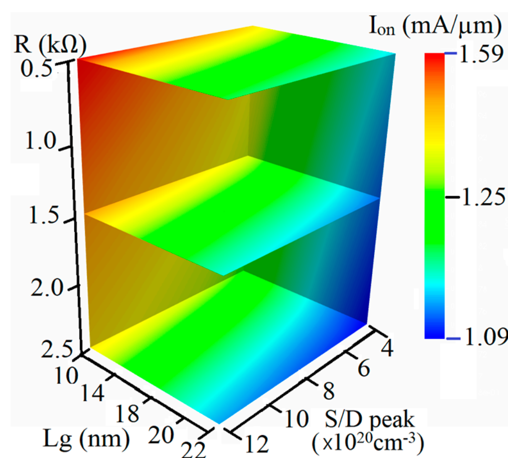

Figure 13. Correlation between NWT performance and source/drain peak doping, gate length, and S/D contact resistance. NWT cross-section is Phi (5 nm × 8.1 nm) and channel orientation is <110>. I_{on} extracted at high drain voltage V_D = 0.7 V.

Vertically stacked lateral NWT nanowires are included in the ITRS roadmap to reduce the contacted gate pitch and to enhance the current per footprint. Figure 14 compares both Phi and

1/Phi NWTs in vertically stacked structures. The I_D-V_G characteristics of both NWTs are shown in Figure 15.

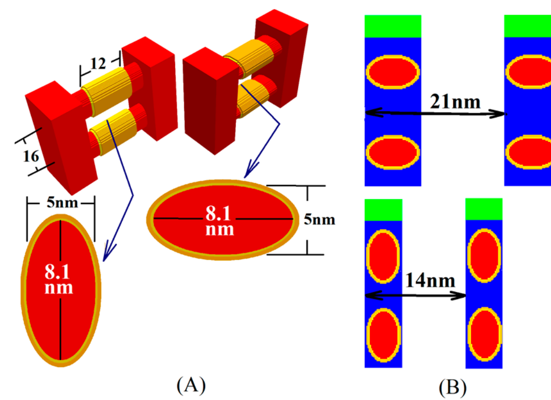

Figure 14. (**A**) Vertically stacked lateral NWT of both phi and 1/Phi; (**B**) The gate pitch layout for Phi and 1/Phi NWTs.

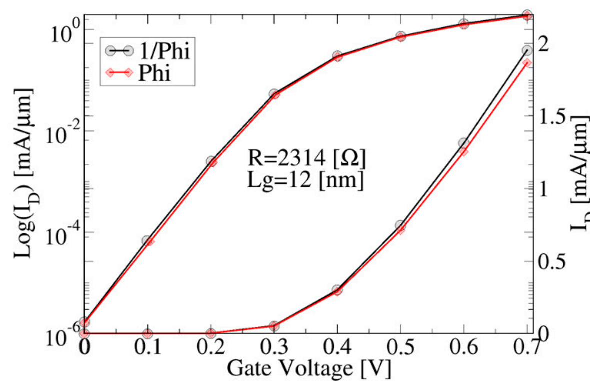

Figure 15. I_D-V_G characteristics of vertically stacked of two lateral Phi (5 nm × 8.1 nm) (red) and (8.1 nm × 5 nm) 1/Phi (black) NWTs at high drain voltage V_D = 0.7 V. The gate length is 12 nm. <110> is the channel orientation.

5. Conclusions

The present paper represents a valuable contribution to the literature, since it is the first publication to deal with a simulation of the effect that Phi has on the electrostatics and device performance of n-type silicon nanowire transistors for 5-nm CMOS applications. Regarding the main findings, it is reasonable to conclude that the usage of NWT shapes with aspect ratios equivalent (or approximate) to Phi has the potential to serve as a way to enhance gate capacitance, along with the mobile charge in the channel. In view of this, significant potential exists to heighten the intrinsic speed of the device. Noteworthy findings are also enclosed regarding the relationship between gate length and time delay, along with the main FoM, including V_T, I_{off} and I_{on}, and DIBL.

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