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Vertically Stacked Lateral Nanowire Transistors: Optimisation for 5nm CMOS Technology

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Abstract— **In this work, for the first time we employ ensemble Monte Carlo /2D-Poisson-Schrödinger to study the impact of golden ratio Phi on the performance of the vertically stacked lateral silicon nanowire transistor. The design of experiment and solution for the uniformity of the current density are also discussed.**

I. Introduction

Gate all around nanowire transistors is the most promising architecture to extend the scalability of the gate pitch future technology nodes to beyond the FinFET limit [1]. The novel structure of vertically stacked lateral nanowires VSL has been included in the ITRS roadmap to tackle the challenge of degradation of the drive current per footprint of NWT and to achieve higher density beyond scaling. In this context, we previously demonstrated the performance of VSL NWT and concepts of engineering the electron transport properties in NWTs such as strain [2], channel orientation, cross-sectional shape [3], and channel materials. We also demonstrated for the first time the uniformity of the current density in each stacked lateral NWT [4]. In this work, we performed simulation study focused on improvement of S/D contacts as a possible solution for the uniformity of the current density, further we have for the first time present the impact of golden ratio Phi on VSL NWT performance. The design of experiment for golden ratio VSL NWT and the effects of size, gate lengths and effective oxide thickness on DIBL, Ioff, and Ion has been investigated.

II. Methodology

A. Simulation

In this work we used ensemble Monte Carlo (EMC) simulations with 2D-Poisson-Schrödinger (PS) for quantum corrections [3]; The quantum corrected EMC simulations accurately captured the nonequilibrium charge transport [4].

B. Device Optimization

The trade-off between performance and leakage currents can be achieved by engineering the device structures. The VSL NWT in [1] is selected as a reference device. Firstly, the cross-sectional shape of the reference device is approximately a circular shape with a diameter 8nm, and cross-sectional area A=16π nm^2. The improved device has elliptical 5nm x 8nm cross-section (A=10π^2) with aspect ratio AR equivalent to the golden ratio φ= (1+√5)/2=1.618. We have observed that an elongated elliptical nanowire delivers the highest mobile charge for a given gate overdrive with the aspect ratio equivalent or close to the golden ratio thereby maximises the drive current while minimising the channel footprint from 8nm to 5nm.

Secondly, for the VSL NWT, the current density degrades through the identically sized lateral NWTs in the vertical stack. The upper lateral nanowires, closer to the source/drain, contacts carry more current than the ones that are farther away (bottom) due to is due to series resistance related voltage drop, and it may become weak point suffering extensive ageing. Solutions including the idea of increasing the diameter of lower nanowires with respect to the upper nanowires in the stack are demonstrated in [5]. However, although the drain current is increasing with the increase of the NWT cross-sectional area, the voltage drop will increase across the highly doped S/D regions. Furthermore, the possibility of decreasing the doping concentrations near the top lateral NWT and increasing it gradually near the middle and the bottom lateral NWTs, would decrease the total drain current (Ion). Therefore, it is desirable to optimise S/D contacting by the deformation of S/D contacts.

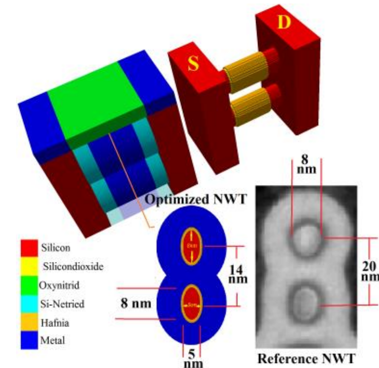

Fig. 1 3D schematic view of simulated Si nanowire transistor (NTW) and material information, comparable to reference device [1]

III. Results and Discussion

. Fig 2 (left-hand-side) compares the current density of VSL NWT with the identical cross-sectional area (10π nm^2). The current density is anisotropic, top lateral NWT carries more current than the middle lateral NWT, and the middle NWT carries more current than the bottom NWT. Figure 2 (right-hand-side) compares the current density of VSL NWT with three lateral NWTs with of 5nm x(b)nm where b=8nm, 8.8nm and, 9.6nm for the (top, middle, bottom) lateral NWTs. Increasing the size of the middle NWT and the bottom NWT is the leading cause of anisotropic current distribution due to voltage drop correlated with series resistance in highly doped S/D region. Slicing the S/D contacts from the top to the middle of the stack could balance

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the current density. Fig. 4 shows an efficient solution to optimise the anisotropic current density by slicing up from the top of contact and the second slice up to the middle of the stack.

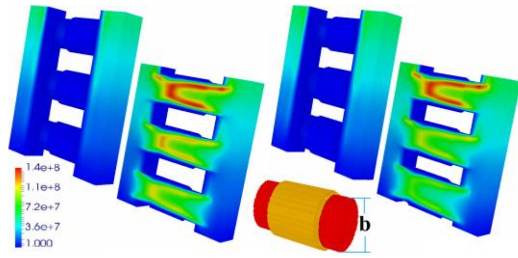

Fig 3 (left) 3D view of the current density for NWTs with (identical) cross-sectional (5nmx8nm), (right) current density for NWTs with (5nmxb), b= 8nm, 8.8nm, 9.6nm for top, bottom, and down laterals NWTs. L_G=12nm. V_D=0.7V.

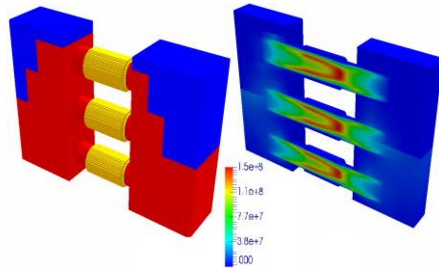

Fig 4 Slicing the S/D contact, the up slice is from the top of contact and the second slice up to the middle of the stack. (right) The current density of longitudinal cross section. (Identical) cross-sectional (5nmx8nm), current density for L_G=12nm V_D=0.7V and solid lines V_D=0.7V.

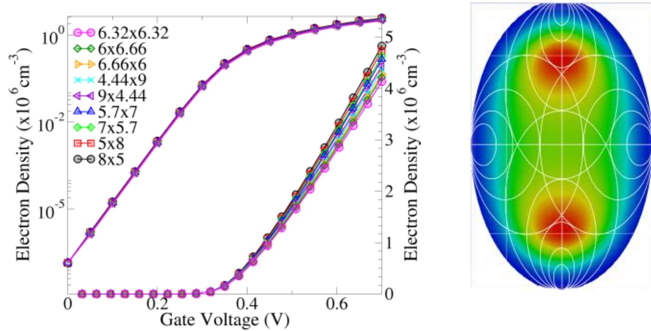

Fig 5 (right) Comparison of the Phi ovals with the charge distribution in the (5nmx8.1nm) nanowire cross-section obtained from the Poisson-Schrödinger simulations. (left) Gate voltage dependence of the mobile charge in the channel for the NWT with different cross sections.

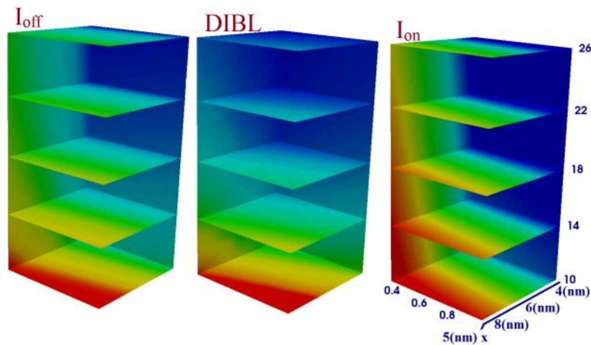

Fig. 6 Design of experiment for golden ratio NWT and the effects of size, gate lengths and effective oxide thickness on DIBL, I_{off}, and I_{on}.

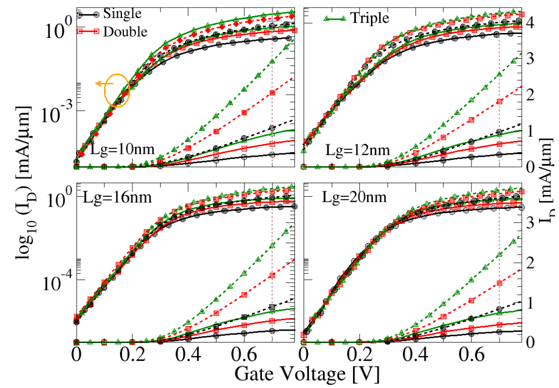

Fig. 6 I_D-V_G curves based on calibrated DD methods of a single, double and triple channel Si NWT at four different gate lengths at low (5mV) and high (0.7V) drain bias. Dashed lines represent 0.7V drain bias, and the solid line is for 5mV drain bias.

Fig 5 (right-hand side) shows the phi ovals with the charge distribution in the (5nmx8.1nm) nanowire cross-section obtained from the Poisson-Schrödinger simulations. The signatures of isotropic charge distributions showing the same attributes as the golden ratio (Phi).

Fig 5 (left-hand side) shows gate voltage dependence of the mobile charge in the channel for the NWT with different AR at the same cross-sectional area. The NWT with Phi and 1/Phi has more quantum charge compares to the others NWTs .

Fig 6 shows the design of experiment for VSH NWT and the effects of size, gate lengths and effective oxide thickness on DIBL, Ioff and Ion. The figure shows that for the nanowire with the shortest gate length has the most device the change of all three above parameters is the most significant. Fig. 6 compares the I_D-V_G characteristics based on simulations of a single, double and triple channel Si NWT at four different gate lengths at low (5mV) and high (0.7V) drain bias. Those I_D-V_G characteristics show that in all case the device with three nanowires performs better than the single and double NWT. Also, the drive current increases with decreasing of the gate length.

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